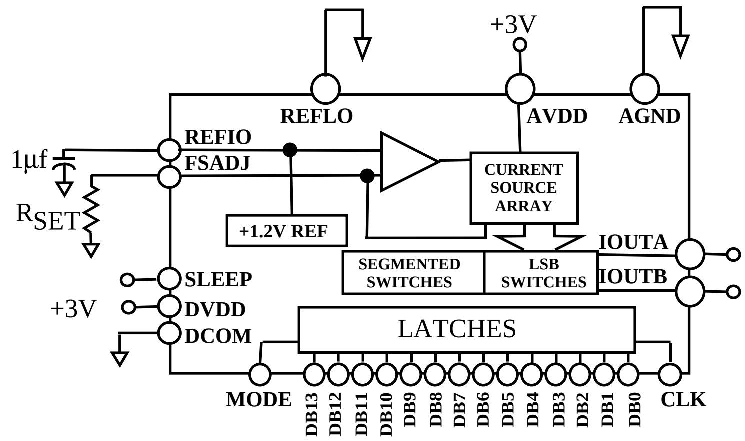
ANALOG DEVICES

14-Bit, 165 MSPS TxDAC® D/A Converter

Preliminary Technical Data AD9744

FEATURES
14-Bit Resolution
165 MSPS Conversion Rate
2's Complement or Straight Binary data format
SFDR @ 2 to 40MHz: ~80dBc
Single Ended Clock Input
+3V Compatible CMOS Inputs
Single +3V Supply Operation
Power Dissipation: 115 mW @ +3V
Power Down Mode: 12 mW @ +3V
On-chip 1.2 V Reference
28 pin SOIC/TSSOP packages



BLOCK DIAGRAM

APPLICATIONS
Wideband Communications TX:
Digital Quadrature Modulation Architectures
W-CDMA, Multi-Carrier GSM, TDMA, CDMA Systems
Instrumentation:
ATE, Signal Synthesis

PRODUCT DESCRIPTION
The AD9744 is a high precision 14-bit 3rd generation TxDAC with state of the art distortion and noise performance. The AD9744 is the 14-bit member of a pin compatible family consisting of 12 and 10-bit TxDACs developed to meet the demanding performance requirements of the most stringent multi-carrier and 3G basestations. The clock interface can accept a single ended CMOS input.

The DAC utilizes a segmented current-source architecture combined with a proprietary switching technique to reduce glitch energy and to maximize dynamic accuracy. The DAC provides differential current outputs thus supporting single-ended or differential applications. The AD9744 differential current output is identical to that of the entire TxDAC and TxDAC+ family and provides a nominal full-scale current from 2 to 20mA. The AD9744 is manufactured on an advanced low cost 0.35 micron CMOS process. It operates from a single supply of 2.7V to 3.6 V and consumes 115 mW of power.

Targeted at ultra-wide dynamic range, multi-carrier and multi-standard systems, desiring unmatched distortion and noise performance.

REV.PrA 04/16/01

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PRODUCT HIGHLIGHTS
1. The AD9744 is a 14 bit member of a pin compatible 10 and 12-bit TxDAC family offering excellent INL and DNL performance..

2. Data input supports 2's complement or straight binary data coding.

3. High speed, single-ended CMOS clock input can support 165 MSPS conversion rate.

4. Low Power: Complete CMOS DAC function operates on ~105mW from a 2.7V to 3.6V single supply. The DAC full-scale current can be reduced for lower power operation, and a sleep mode is provided for low-power idle periods.

5. On-chip Voltage Reference: The AD9744 includes a 1.2V temperature-compensated bandgap voltage reference.

6. Small 28 pin SOIC/TSSOP packages.

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AD9744-SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +3V, DVDD = +3V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	14			Bits
DC ACCURACY [1]				
Integral Linearity Error (INL)				
TA = +25°C	TBD	±1.5	TBD	LSB
Differential Nonlinearity (DNL)				
TA = +25°C	TBD	±1.0	TBD	LSB
ANALOG OUTPUT				
Offset Error	–0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)		±0.5		% of FSR
Gain Error (With Internal Reference)		±1		% of FSR
Gain Match		0.25		% of FSR
Full-Scale Output Current [2]	2.0		20.0	mA
Output Compliance Range	–1.0		1.25	V
Output Resistance		100		KΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.25	1.26	V
Reference Output Current [3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance			1	MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
VDD	2.7	3.3	3.6	V
DVDD	2.7	3.3	3.6	V
Analog Supply Current (IAVDD)		33	TBD	mA
Digital Supply Current (IDVDD)[4]		2	TBD	mA
Supply Current Sleep Mode (IAVDD)		4	TBD	mA
Power Dissipation [4] (3 V, IOUTFS = 20 mA)		115	TBD	mW
Power Dissipation [5] (3 V, IOUTFS = 20 mA)		TBD		mW
Power Supply Rejection Ratio [6] —AVDD	–0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio [6] —DVDD	–0.025		+0.025	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES

1 Measured at IOUTA, driving a virtual ground.

2 Nominal full-scale current, I_{OUTFS}, is 32 times the I_{REF} current.

3 An external buffer amplifier with input bias current <100na should be used to drive any external load.

4 Measured at F_{CLOCK} = 25 MSPS and F_{OUT} = 1.0 MHz.

5 Measured as unbuffered voltage output with I_{OUTFS} = 20 mA and 50 Ω R_{LOAD} at IOUTA and IOUTB, F_{CLOCK} = 100 MSPS and F_{OUT} = 40 MHz.

6 ±5% Power supply variation.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (T_MIN to T_MAX, AVDD = +3V, DVDD = +3V, I_OUTFS = 20 mA, Differential Transformer Coupled Output, 50Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (F_{CLOCK})	165			MSPS
Output Settling Time (t_{st}) (to 0.1%)[8]		11		ns
Output Propagation Delay (t_{pd})		TBD		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[8]		2.5		ns
Output Fall Time (10% to 90%)[8]		2.5		ns
Output Noise (IOUTFS = 20 mA)		50		pA/√Hz
Output Noise (IOUTFS = 2 mA)		30		pA/√Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
F_{CLOCK} = 25 MSPS; F_{OUT} = 1.00 MHz				
0 dBFS Output				
TA = +25°C		TBD		dBc
–6 dBFS Output				dBc
–12 dBFS Output				dBc
–18 dBFS Output				dBc
F_{CLOCK} = 65 MSPS; F_{OUT} = 1.00 MHz		84		dBc
F_{CLOCK} = 65 MSPS; F_{OUT} = 2.51 MHz		83		dBc
F_{CLOCK} = 65 MSPS; F_{OUT} = 10 MHz		78		dBc
F_{CLOCK} = 65 MSPS; F_{OUT} = 15 MHz		77		dBc
F_{CLOCK} = 65 MSPS; F_{OUT} = 25 MHz		70		dBc
F_{CLOCK} = 125 MSPS; F_{OUT} = 21 MHz		68		dBc
F_{CLOCK} = 125 MSPS; F_{OUT} = 41 MHz		60		dBc
Spurious-Free Dynamic Range within a Window				
F_{CLOCK} = 25 MSPS; F_{OUT} =1.00 MHz; 2 MHz Span		TBD		
F_{CLOCK} = 50 MSPS; F_{OUT} = 5.02 MHz; 2 MHz Span				dBc
F_{CLOCK} = 65 MSPS; F_{OUT} = 5.03 MHz; 2.5 MHz Span				dBc
F_{CLOCK} = 125 MSPS; F_{OUT} = 5.04 MHz; 4 MHz Span				dBc
Total Harmonic Distortion				
F_{CLOCK} = 25 MSPS; F_{OUT} = 1.00 MHz		-83		
TA = +25°C				dBc
F_{CLOCK} = 50 MHz; F_{OUT} = 2.00 MHz				dBc
F_{CLOCK} = 65 MHz; F_{OUT} = 2.00 MHz				dBc
F_{CLOCK} = 125 MHz; F_{OUT} = 2.00 MHz				dBc
Multitone Power Ratio (8 Tones at 110 kHz Spacing)				
F_{CLOCK} = 65 MSPS; FOUT = 2.00 MHz to 2.99 MHz				
0 dBFS Output		TBD		dBc
–6 dBFS Output				dBc
–12 dBFS Output				dBc
–18 dBFS Output				dBc

NOTES
8 Measured single-ended into 50Ω load.
Specifications subject to change without notice.

AD9744-SPECIFICATIONS

DIGITAL SPECIFICATIONS (T$_{MIN}$ to T$_{MAX}$, AVDD = +3V, DVDD = +3V, I$_{OUTFS}$ = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS[1]				
Logic “1” @ DVDD = 3	2.1	3		V
Logic “0” @ DVDD = 3		0	0.9	V
Logic “1” Current	-10		+10	µA
Logic “0” Current	-10		+10	µA
Input Capacitance		5		pF
Input Setup Time (t_s)	2			ns
Input Hold Time (t_h)	1.5			ns
Latch Pulse Width (t_{lpw})	TBD			ns

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	ACOM	-0.3	+3.9	V
DVDD	DCOM	-0.3	+3.9	V
ACOM	DCOM	-0.3	+0.3	V
AVDD	DVDD	-3.9	+3.9	V
CLOCK, SLEEP	DCOM	-0.3	DVDD + 0.3	V
Digital Inputs	DCOM	-0.3	DVDD + 0.3	V
IOUTA, IOUTB	ACOM	-1.0	AVDD + 0.3	V
REFIO, REFLO, FSADJ	ACOM	-0.3	AVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		-65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD9744-AR	–40°C to +85°C	28 pin SOIC	R-28
AD9744-ARU	–40°C to +85°C	28 pin TSSOP	RU-28
AD9744-EB		Evaluation Board	

* R = Small Outline IC; RU = Thin Shrink Small Outline Pacakge

THERMAL CHARACTERISTICS

Thermal Resistance

28 Lead 300-Mil SOIC

θ_{JA}= 71.4 °C/W

θ_{JC}= 23.0 °C/W

28 Lead TSSOP

θ_{JA}= 97.9 °C/W

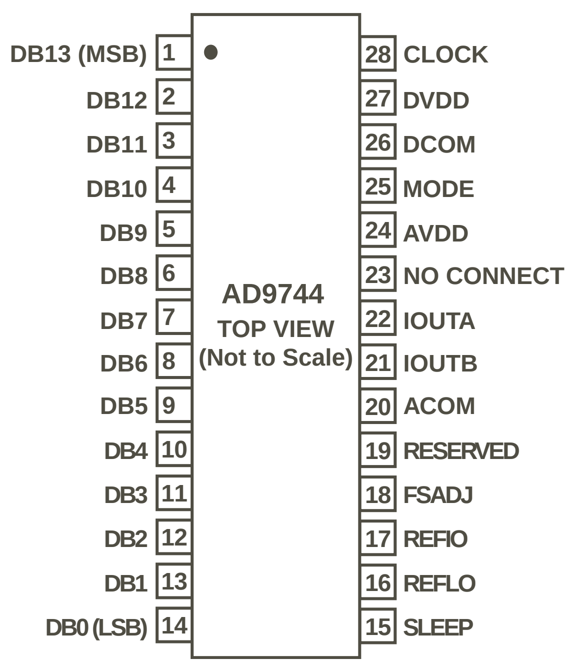
θ_{JC}= 14.0 °C/W

TBD

Figure 1. Timing Diagram

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1-14	DB13 - DB0	Data bits. DB13 is most significant bit and DB0 is least significant bit.
15	SLEEP	Power-down control input
16	REFLO	Reference AGND when using internal 1.2 reference. Reference AVDD to disable internal reference.
17	REFIO	Reference input/output
18	FSADJ	Full-scale current output adjust.
19	RESERVED	Reserved
20	ACOM	Analog Common
21,22	IOUTA, IOUTB	Differential DAC current outputs
23	NC	No connect
24	AVDD	Analog Supply Voltage (3V)
25	MODE	Mode selects between straight binary (0) and two's compliment (1) input.
26	DCOM	Digital Common
27	DVDD	Digital Supply Voltage (3V)
28	CLOCK	Clock input. Data latches on positive edge of clock.



DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree C. For reference drift, the drift is reported in ppm per degree C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Multitone Power Ratio
The spurious free dynamic range containing multiple carrier tones of equal amplitude. It is measures as the difference between the rms amplitude of a carrier tone to the peak spurious signal in the region of a removed tone.

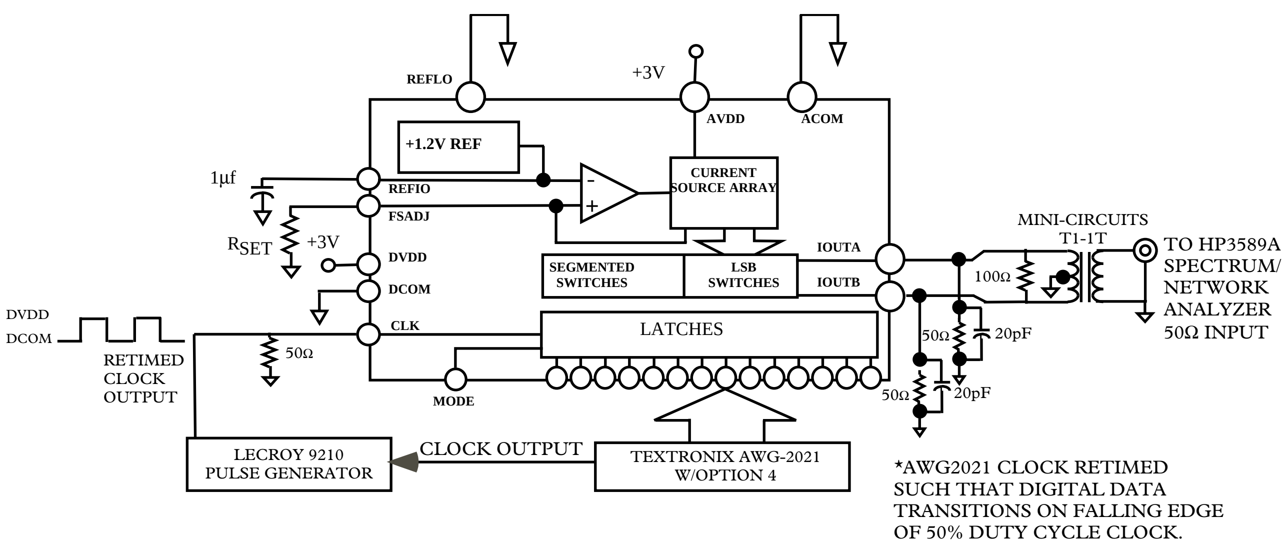


Figure 2. Basic AC Characterization Test Set-Up For AD9744

TPC 1. SFDR vs. f_{OUT}@ 0dBFS

TPC 2. SFDR vs. f_{OUT}@ 5MSPS

TPC 3. SFDR vs. f_{OUT} @25MSPS

TPC 4. SFDR vs. f_{OUT}@ 65MSPS

TPC 5. SFDR vs. f_{OUT}@ 165MSPS

TPC 6. SFDR vs. f_{OUT} and I_{OUTFS} @65MSPS and 0dBFS

TPC 7. Single-Tone SFDR vs. A_{OUT} @f_{OUT}=f_{CLOCK}/11

TPC 8. Single-Tone SFDR vs. A_{OUT} @f_{OUT}=f_{CLOCK}/5

TPC 9. Dual-Tone SFDR vs. A_{OUT} @f_{OUT}=f_{CLOCK}/7

TPC 10. SINAD vs. F_{CLOCK} and I_{OUTFS} @ F_{OUT} = 5MHz and 0dBFS

TPC 11. Typical INL

TPC 12. Typical DNL

TPC 13. SFDR vs. Temperature @ 165MSPS, 0dBFS

TPC 14. Gain and Offset Matching vs Temperature

TPC 15. Single Tone SFDR

TPC 16. Dual Tone SFDR

TPC 17. Four tone SFDR

FUNCTIONAL DESCRIPTION

Figure 3 shows a simplified block diagram of the AD9744. The AD9744 consists of a DAC, digital control logic and fullscale output current control. The DAC contains a PMOS current source array capable of providing up to 20mA of full-scale current (I_{OUTFS}). The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSBs are binary weighted fractions of the middle bits current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >100KΩ).

TBD

Figure 3. Simplified Block Diagram of AD9744

All of these current sources are switched to one or the other of the two output nodes (i.e., IOUTA or IOUTB) via PMOS differential current switches. The switches are based on a new architecture that improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9744 have separate power supply inputs (i.e., AVDD and DVDD) that can operate independently over a 2.7V to 3.6V Volt range. The digital section, which is capable of operating up to a 150 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.2V bandgap voltage reference and a reference control amplifier.

The DAC full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}, connected to the Full Scale Adjust (FSADJ) pin. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is $32 \times I_{REF}$.

REFERENCE OPERATION

The AD9744 contains an internal 1.2V bandgap reference. The internal reference can be disabled by raising REFLO to AVDD. It can also be easily overridden by an external reference with no effect on performance. REFIO serves as either an *input* or *output* depending on whether the internal or an external reference is used. To use the internal reference, simply decouple the REFIO pin to ACOM with a 0.1µF capacitor and connect REFLO to ACOM via a resistance less than 5 ohms. The internal reference voltage will be present at REFIO. If the voltage at REFIO is to be used anywhere else

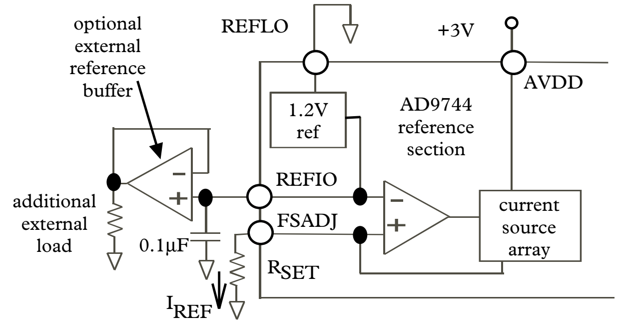


Figure 4. Internal Reference Configuration

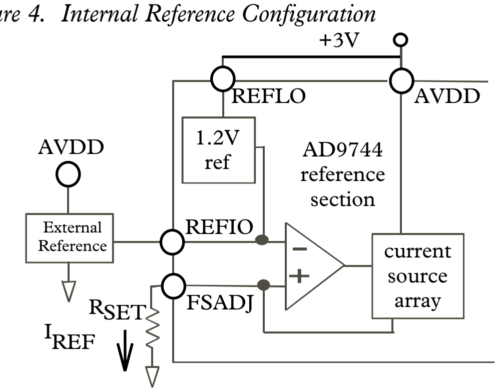


Figure 5. External Reference Configuration

in the circuit, an external buffer amplifier with an input bias current of less than 100nA should be used. An example of the use of the internal reference is given in Figure 4.

An external reference can be applied to REFIO as shown in Figure 5. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1µF compensation capacitor is not required since the internal reference is overridden, and the relatively high input impedance of REFIO minimizes any loading of the external reference.

REFERENCE CONTROL AMPLIFIER

The AD9744 contains a control amplifier that is used to regulate the full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter as shown in Figure 4, so that its current output, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is copied to the segmented current sources with the proper scale factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting IREF between 62.5 µA and 625 µA. The wide adjustment span of I_{OUTFS} provides several benefits. The first relates directly to the power dissipation of the AD9744, which is proportional to I_{OUTFS} (refer to the POWER DISSIPATION section). The second relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 500 KHz and can be used for low frequency small signal multiplying applications.

DAC TRANSFER FUNCTION

Both DACs in the AD9744 provide complementary current outputs, IOUTA and IOUTB. IOUTA will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 16383) while IOUTB, the complementary output, provides no current. The current output appearing at IOUTA and IOUTB is a function of both the input code and I_{OUTFS} and can be expressed as:

$$I_{OUTA} = (DAC\ CODE/16384) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (16383 - DAC\ CODE)/16384 \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to 16383 (i.e., Decimal Representation).

As mentioned previously, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage, V_{REFIO} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, IOUTA and IOUTB should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. Note, R_{LOAD} may represent the equivalent load resistance seen by IOUTA or IOUTB as would be the case in a doubly terminated 50Ω or 75Ω cable. The single-ended voltage output appearing at the IOUTA and IOUTB nodes is simply :

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA}, I_{OUTB} and I_{REF}; V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2\times DAC\ CODE - 16383)/16384\} \times (32\times R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

These last two equations highlight some of the advantages of operating the AD9744 differentially. First, the differential operation will help cancel common-mode error sources associated with I_{OUTA} and I_{OUTB} such as noise, distortion and dc offsets. Second, the differential code dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note, the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9744 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

ANALOG OUTPUTS

The complementary current outputs in each DAC, I_{OUTA} and I_{OUTB}, may be configured for single-ended or differential operation. I_{OUTA} and I_{OUTB} can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC TRANSFER FUNCTION section by Equations 5 through 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB} can also be converted to a single-ended voltage via a transformer or differential amplifier configuration. The ac performance of the AD9744 is optimum and specified using a differential transformer coupled output in which the voltage swing at IOUTA and IOUTB is limited to ±0.5 V. If a single-ended unipolar output is desirable, IOUTA should be selected.

The distortion and noise performance of the AD9744 can be enhanced when it is configured for differential operation. The common-mode error sources of both I_{OUTA} and I_{OUTB} can be significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases. This is due to the first order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough and noise.

Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load (i.e., assuming no source termination). Since the output currents of IOUTA and IOUTB are complementary, they become additive when processed differentially. A properly selected transformer will allow the AD9744 to provide the required power and voltage levels to different loads.

The output impedance of IOUTA and IOUTB is determined by the equivalent parallel combination of the PMOS switches associated with the current sources and is typically 100 KΩ in parallel with 5 pF. It is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) due to the nature of a PMOS device. As a result, maintaining IOUTA and/or IOUTB at a virtual ground via an I-V op amp configuration will result in the optimum dc linearity. Note the INL/DNL specifications for the AD9744 are measured with IOUTA maintained at a virtual ground via an op amp.

IOUTA and IOUTB also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The negative output compliance range of –1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the AD9744.

The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.2 V for an I_{OUTFS} = 20 mA to 1.00 V for an I_{OUTFS} = 2 mA. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUTA and IOUTB does not exceed 0.5 V. Applications requiring the

AD9744's output (i.e., V_{OUTA} and/or V_{OUTB}) to extend its output compliance range should size R_{LOAD} accordingly. Operation beyond this compliance range will adversely affect the AD9744's linearity performance and subsequently degrade its distortion performance.

DIGITAL INPUTS

The AD9744's digital inputs consists of a 14 bit channel and a clock. The 14-bit parallel data inputs follow standard

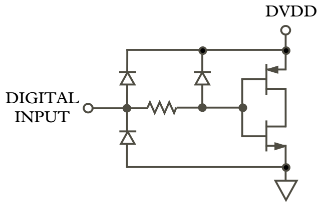


Figure 6. Equivalent Digital Input

positive binary coding where DB13 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). IOUTA produces a full-scale output current when all data bits are at logic 1. IOUTB produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master/slave latch. The DAC output updates on the rising edge of the clock and is designed to support a clock rate as high as 165 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulse width. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met, although the location of these transition edges may affect digital feedthrough and distortion performance. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

DAC TIMING

INPUT CLOCK AND DATA TIMING RELATIONSHIP

It is important to know that the DAC has a full clock cycle latency between latching the data and the output of the associated analog value. Also, SNR in a DAC is dependent on the relationship between the position of the clock edges and the point in time at which the input data changes. The AD9744 is rising edge triggered, and so exhibits SNR sensitivity when the data transition is close to this edge. In general, the goal when applying the AD9744 is to make the data transition close to the falling clock edge. This becomes more important as the sample rate increases. Figure 7 shows the relationship of SNR to clock placement with different sample rates. Note that at the lower sample rates, much more tolerance is allowed in clock placement, while at higher rates, much more care must be taken.

TBD

Figure 7. SNR vs. Clock Placement @ f_{OUT} = 10MHz

SLEEP MODE OPERATION

The AD9744 has a power down function that turns off the output current and reduces the supply current to less than 4ma over the specified supply range of 2.7V to 3.6V and temperature range. This mode can be activated by applying a logic level "1" to the SLEEP pin. The SLEEP pin logic threshold is equal to 0.5×AVDD. This digital input also contains an active pull-down circuit that ensures the AD9744 remains enabled if this input is left disconnected. The AD9744 takes less than 50ns to power down and approximately 5µs to power back up.

POWER DISSIPATION

The power dissipation, P_D, of the AD9744 is dependent on several factors that include: (1) The power supply voltages (AVDD and DVDD), (2) the full-scale current output I_{OUTFS}, (3) the update rate f_{CLOCK}, (4) and the reconstructed digital input waveform. The power dissipation is

TBD

Figure 8. I_{AVDD} vs I_{OUTFS}

TBD

Figure 9. I_{DVDD} vs Ratio @DVDD=3V

directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS} as shown in Figure 8 and is insensitive to f_{CLOCK}. Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and digital supply DVDD. Figures 9 show I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with DVDD = 3 V.

APPLYING THE AD9744

Output Configurations

The following sections illustrate some typical output configurations for the AD9744. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain and/or level shifting, within the bandwidth of the chosen op-amp.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if IOUTA and/or IOUTB is connected to an appropriately sized load resistor, R_{LOAD}, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity since IOUTA or IOUTB is maintained at a virtual ground. Note that IOUTA provides slightly better performance than IOUTB.

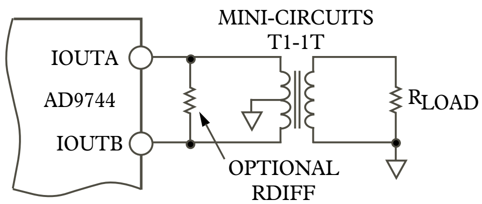


Figure 10. Differential Output Using a Transformer

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion as shown in Figure 6. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's passband. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at IOUTA and IOUTB (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9744. A differential resistor, R_{DIFF}, may be inserted in applications where the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR. Note that approximately half the signal power will be dissipated across R_{DIFF}.

DIFFERENTIAL COUPLING USING AN OP AMP

An op amp can also be used to perform a differential to single-ended conversion as shown in Figure 11. The AD9744 is configured with two equal load resistors, R_{LOAD}, of 25 W. The differential voltage developed across IOUTA and IOUTB is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across IOUTA and IOUTB, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amps distortion performance by preventing the DACs high slewing output from overloading the op amp's input.

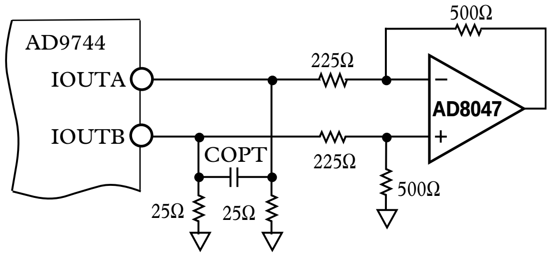


Figure 11. DC Differential Coupling Using an Op-Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8047 is configured to provide some additional signal gain. The op amp must operate off of a dual supply since its output is approximately ±1.0 V. A high speed amplifier capable of preserving the differential performance of the AD9744 while meeting other system level objectives (i.e., cost, power) should be selected. The op-amp's differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

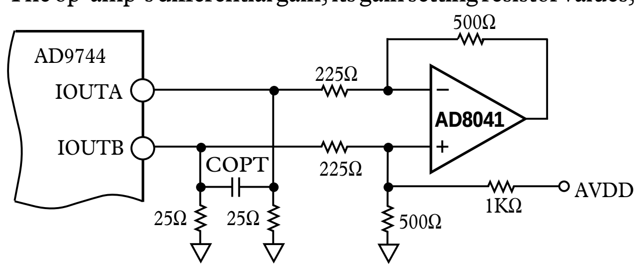


Figure 12. Single Supply DC Differential Coupled Circuit

The differential circuit shown in Figure 12 provides the necessary level-shifting required in a single supply system. In this case, AVDD which is the positive analog supply for both the AD9744 and the op-amp is also used to level-shift the differential output of the AD9744 to midsupply (i.e., AVDD/2). The AD8041 is a suitable op amp for this application.

SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT

Figure 13 shows the AD9744 configured to provide a unipolar output range of approximately 0 V to +0.5 V for a doubly terminated 50 W cable since the nominal full-scale current, I_{OUTFS}, of 20 mA flows through the equivalent R_{LOAD} of 25 W. In this case, R_{LOAD} represents the equiva-

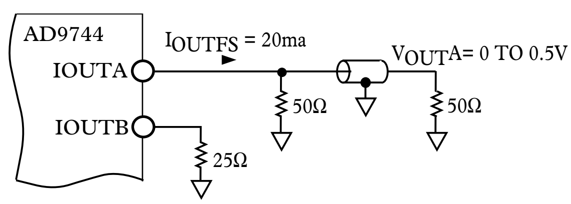


Figure 13. 0V to 0.5V Unbuffered Voltage Output

lent load resistance seen by IOUTA or IOUTB. The unused output (IOUTA or IOUTB) can be connected to ACOM directly or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL) as discussed in the ANALOG OUTPUT section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

SINGLE-ENDED, BUFFERED VOLTAGE OUTPUT CONFIGURATION

Figure 14 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the AD9744 output current. U1 maintains IOUTA (or IOUTB) at a virtual ground, thus minimizing the nonlinear output

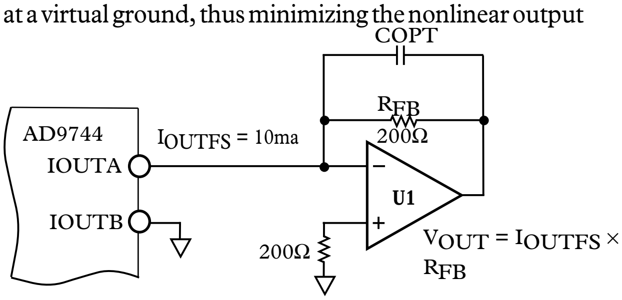


Figure 14. Unipolar Buffered Voltage Output

impedance effect on the DAC's INL performance as discussed in the ANALOG OUTPUT section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by U1's slewing capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current U1 will be required to sink will be subsequently reduced.

POWER AND GROUNDING CONSIDERATIONS, POWER SUPPLY REJECTION

Many applications seek high speed and high performance under less than ideal operating conditions. In these application circuits, the implementation and construction of the printed circuit board is as important as the circuit design. Proper RF techniques must be used for device selection , placement and routing as well as power supply bypassing and grounding to ensure optimum performance. Figures 20 to 25 illustrate the recommended printed circuit board ground, power and signal plane layouts which are implemented on the AD9744 evaluation board.

One factor that can measurably affect system performance is the ability of the DAC output to reject dc variations or ac noise superimposed on the analog or digital dc power distribution. This is referred to as the Power Supply Rejection Ratio. For dc variations of the power supply, the resulting performance of the DAC directly corresponds to a gain error associated with the DAC's full scale current, I_{OUTFS}. AC noise on the DC supplies is common in applications where the power distribution is generated by a switching power supply. Typically, switching power supply noise will occur over the spectrum from tens of KHz to several MHz. The PSRR vs frequency of the AD9744 AVDD supply over this frequency range is shown in Figure 15.

TBD

Figure 15. Power Supply Rejection Ratio of AD9744

Note that the units in Figure 15 are given in units of (amps out/volts in). Noise on the analog power supply has the effect of modulating the internal switches, and therefore the output current. The voltage noise on AVDD, therefore, will be added in a non-linear manner to the desired I_{OUT}.Due to the relative different size of these switches, PSRR is very code dependent. This can produce a mixing effect which can modulate low frequency power supply noise to higher frequencies. Worst case PSRR for either one of the differential DAC outputs will occur when the full-scale current is directed towards that output. As a result, the PSRR measurement in Figure 15 represents a worst case condition in which the digital inputs remain static and the full scale output current of 20ma is directed to the DAC output being measured.

An example serves to illustrate the effect of supply noise on the analog supply. Suppose a switching regulator with a switching frequency of 250KHz produces 10mV of noise and for simplicity sake (i.e. ignore harmonics), all of this noise is concentrated at 250KHz. To calculate how much of this undesired noise will appear as current noise superimposed on the DAC's full scale current, I_{OUTFS}, one must determine the PSRR in dB using Figure 15 at 250 KHz. To calculate the PSRR for a given R_{LOAD}, such that the units of PSRR are converted from A/V to V/V, adjust the curve in Figure 15 by the scaling factor $20\times Log(R_{LOAD})$. For instance, if R_{LOAD} is 50Ω, the PSRR is reduced by 34 dB (i.e., PSRR of the DAC at 250KHz which is 85dB in Figure 15 becomes 51dB Vout/Vin).

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9744 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close to the chip as physically possible.

For those applications that require a single +3 V supply for both the analog and digital supplies, a clean analog supply may be generated using the circuit shown in Figure 16. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained by using low ESR type electrolytic and tantalum capacitors

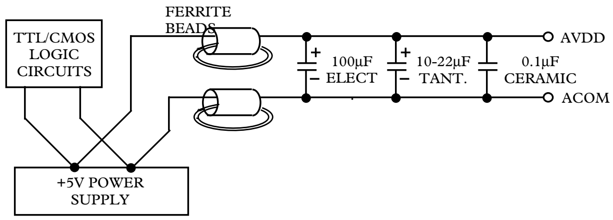


Figure 16. Differential LC Filter for Single +3 V Applications

APPLICATION

VDSL Applications Using the AD9744

Very High Frequency Digital Subscriber Line (VDSL) technology is growing rapidly in applications requiring data transfer over relatively short distances. By using QAM modulation and transmitting the data in discrete multiple tones (DMT), high data rates can be achieved.

As with other multitone applications, each VDSL tone is capable of transmitting a given number of bits, depending on the signal-to-noise ratio (SNR) in a narrow band around that tone. For a typical VDSL application, the tones are evenly spaced over the range of several KHZ to 10MHz. At the high frequency end of this range, performance is generally limited by cable characteristics and environmental factors, such as external interferers. Performance at the lower frequencies is much more dependent on the performance of the components in the signal chain. In addition to in-band noise, intermodulation from other tones can also potentially interfere with the data recovery for a given tone. The two graphs in Figure 13 represent a 500 tone missing bin test vector, with frequencies evenly spaced from 400Hz to 10MHz. This test is very commonly done to determine if distortion will limit the number of bits which can be transmitted in a tone. The test vector has a series of missing tones around 750KHz, which is represented in Figure 17a, and a series of missing tones around 5MHz, which is represented in Figure 17b. In both cases, the spurious free dynamic range (SFDR) between the transmitted tones and the empty bins is greater than 60dB.

CDMA

Carrier Division Multiple Access, or CDMA, is an air transmit/receive scheme where the signal in the transmit path is modulated with a pseudorandom digital code (sometimes referred to as the spreading code). The effect of this is to spread the transmitted signal across a wide spectrum. Similar to a DMT waveform, a CDMA waveform containing multiple subscribers can be characterized as having a high peak to average ratio (i.e., crest factor), thus demanding highly linear components in the transmit signal path. The bandwidth of the spectrum is defined by the CDMA standard being used, and in operation is implemented by using a spreading code with particular characteristics.

Distortion in the transmit path can lead to power being transmitted out of the defined band. The ratio of power transmitted in-band to out-of-band is often referred to as Adjacent Channel Power (ACP). This is a regulatory issue due to the possibility of interference with other signals being transmitted by air. Regulatory bodies define a spectral mask outside of the transmit band, and the ACP must fall under this mask. If distortion in the transmit path causes the ACP to be above the spectral mask, then filtering, or different component selection is needed to meet the mask requirements.

Figure 18 shows the AD9744 reconstructing a wideband, or W-CDMA test vector with a bandwidth of 5MHz, centered at 15.625MHz, and being sampled at 62.5MHz. ACP for the given test vector is measured at 70dB.

Figure 19 shows an example of the AD9744 used in a W-CDMA transmitter application using the AD6122 CDMA 3V IF subsystem. The AD6122 has functions, such as external gain control and low distortion characteristics, needed for the superior Adjacent Channel Power (ACP) requirements of W-CDMA.

TBD

Figure 17a. Notch in Missing Bin at 750KHz is Down >60dB. (Peak Amplitude = 0dBm)

TBD

Figure 17b. Notch in Missing Bin at 5MHz is Down >60dB. (Peak Amplitude = 0dBm)

TBD

Figure 18. CDMA Signal, Sampled at 62.5MSPS, Adjacent Channel Power > 70dBm

AD9744 EVALUATION BOARD

General Description

The AD9744-EB is an evaluation board for the AD9744 14 bit D/A converter. Careful attention to layout and circuit design combined with a prototyping area allow the user to easily and effectively evaluate the AD9744 in any application where high resolution, high speed conversion is required.

This board allows the user the flexibility to operate the AD9744 in various configurations. Possible output configurations include transformer coupled, resistor terminated, and single and differential outputs. The digital inputs can be used in dual port or interleaved mode, and are designed to be driven from various word generators, with the on board option to add a resistor network for proper load termination.

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Figure 19. CDMA Transmit Application Using AD9744 and AD6122

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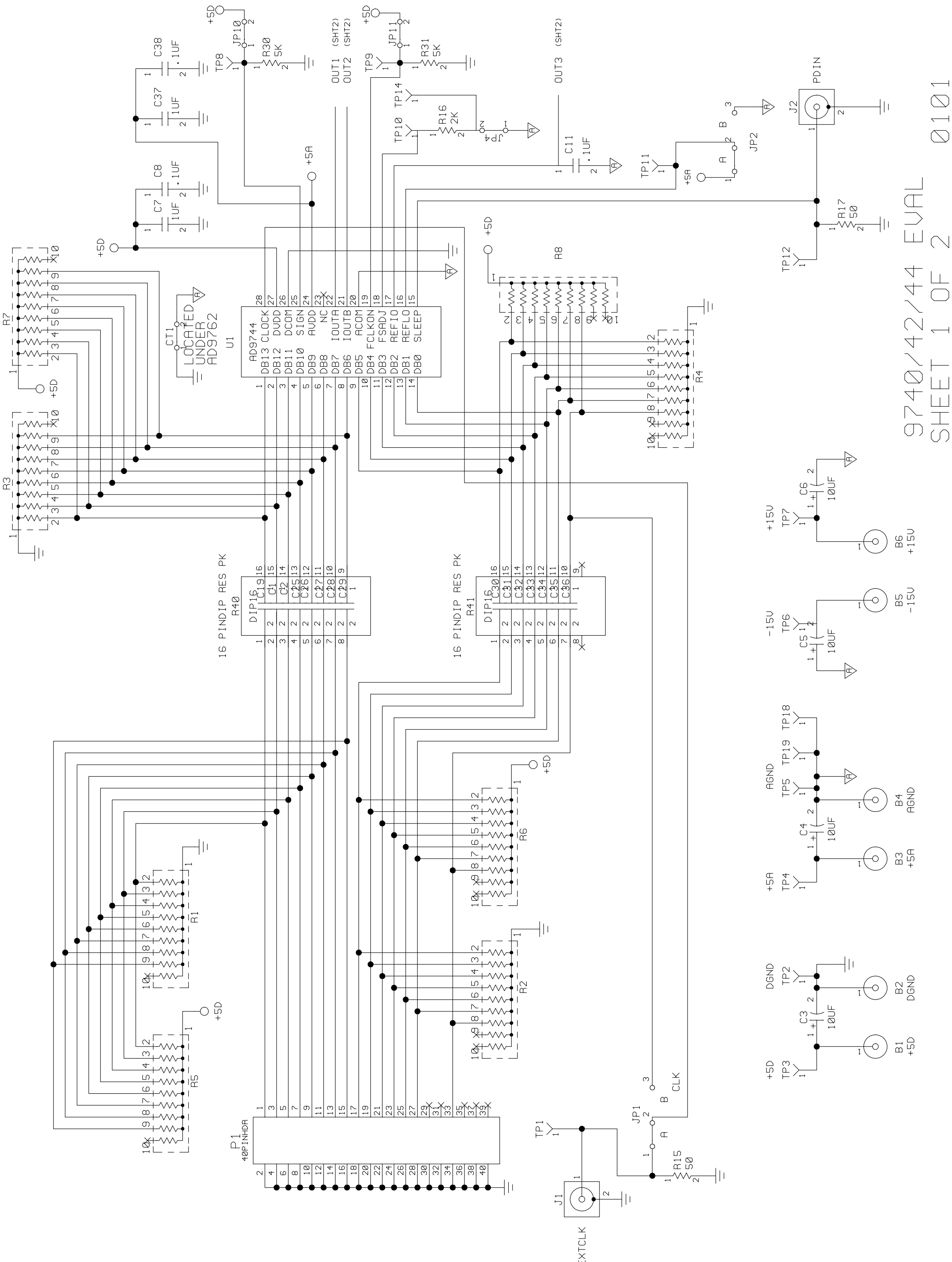
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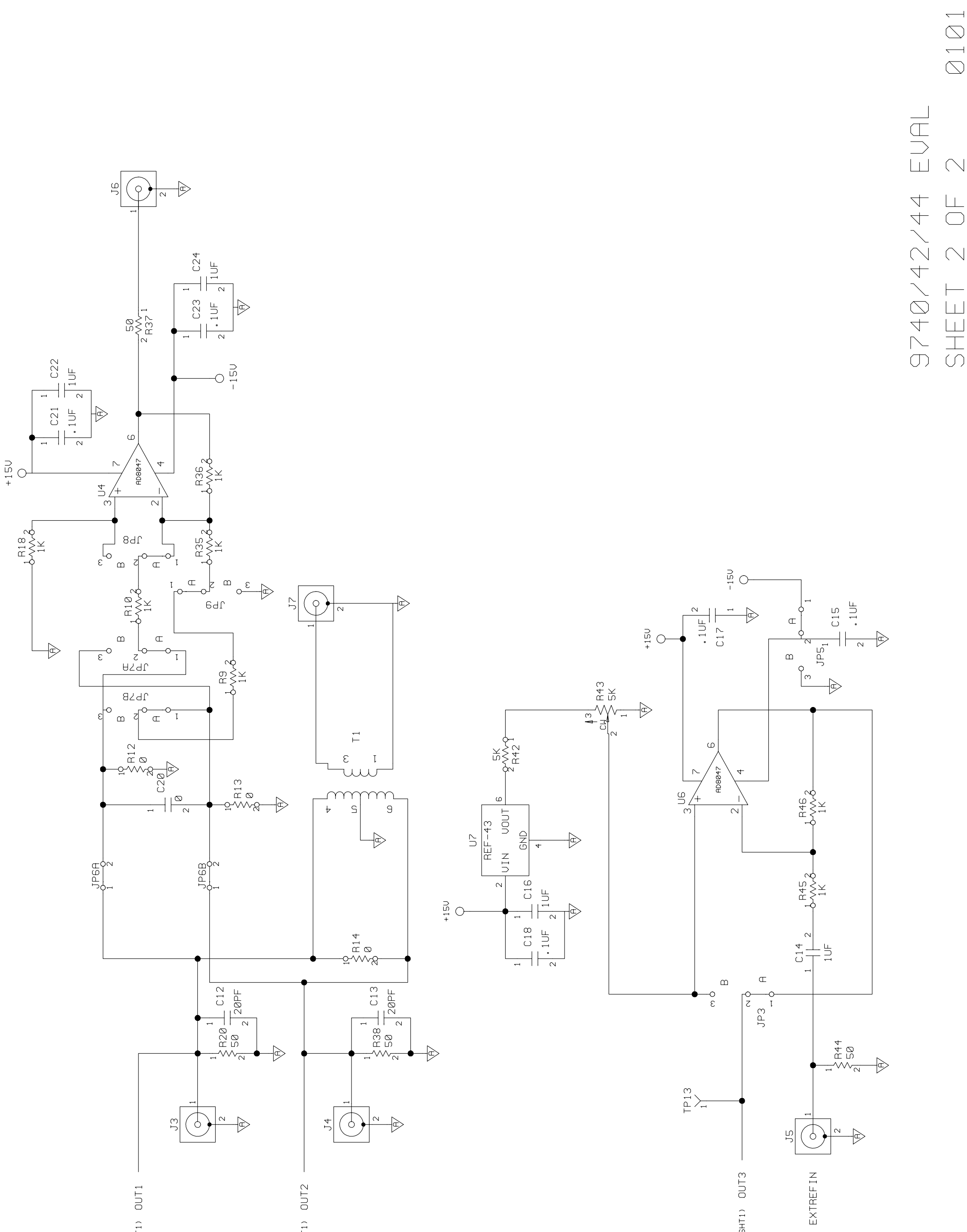
SHEET 1 OF 2
0101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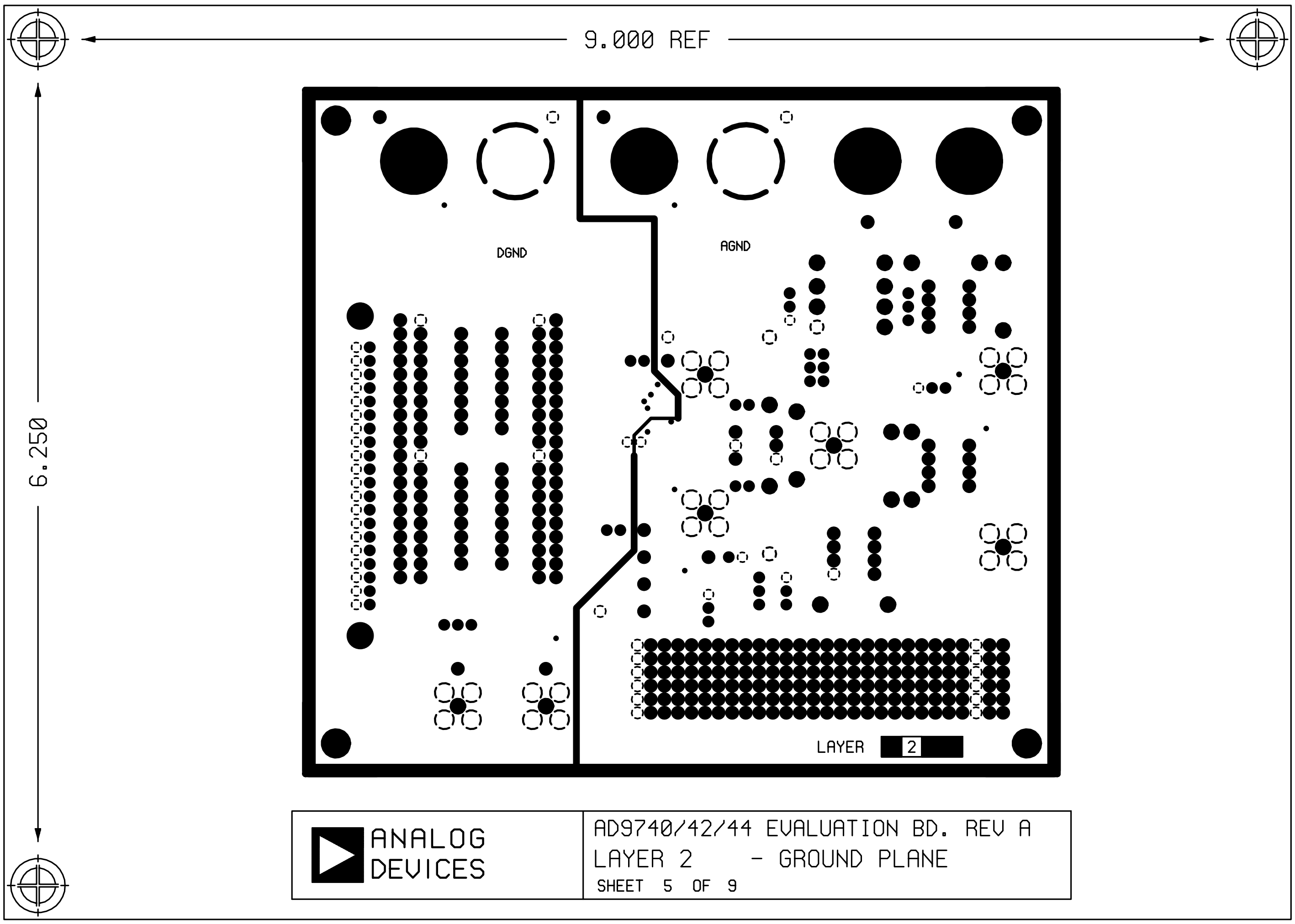
9.000 REF
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DGND
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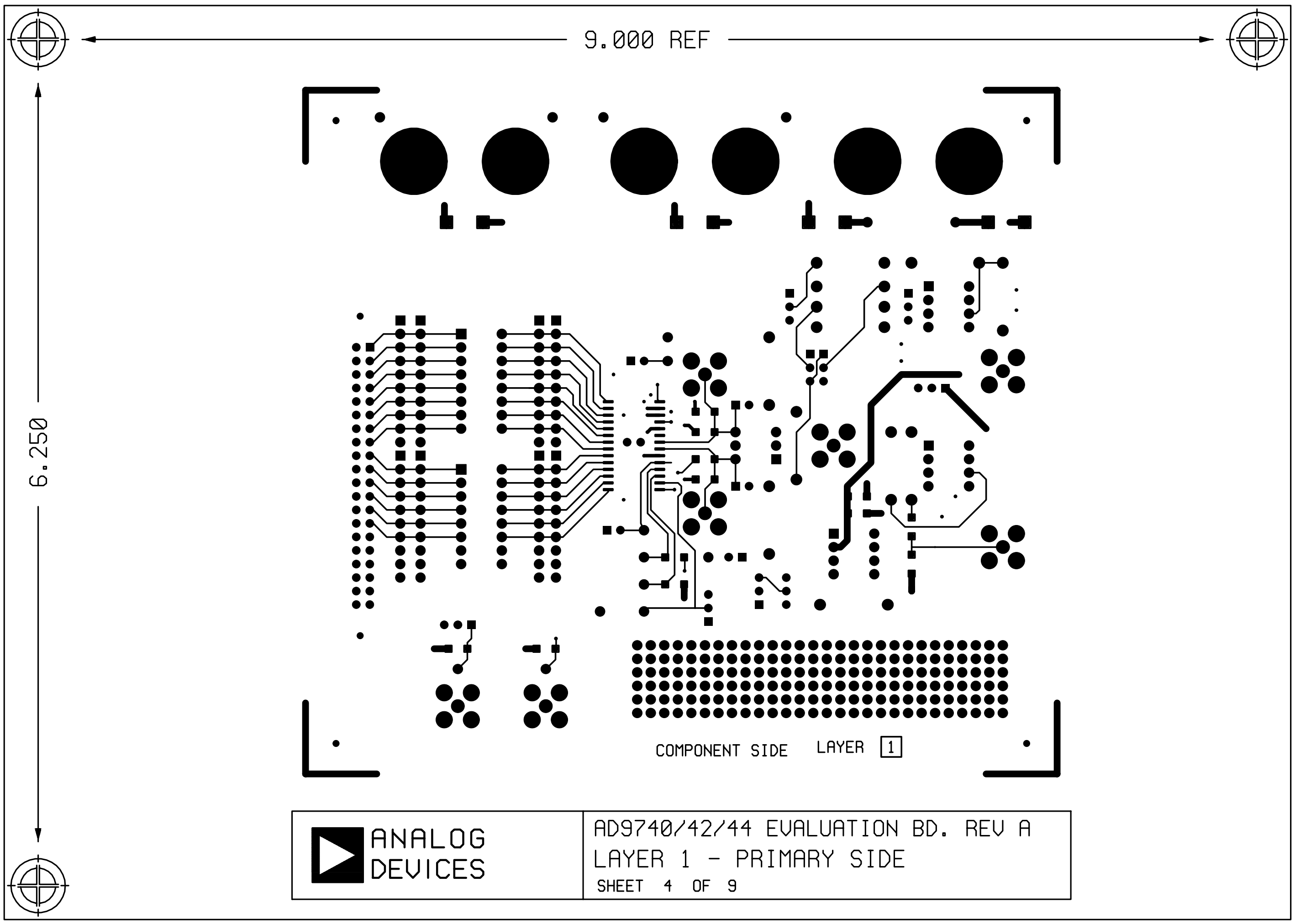
LAYER 2
ANALOG DEVICES
AD9740/42/44 EVALUATION BD. REV A
LAYER 2 - GROUND PLANE
SHEET 5 OF 9


9.000 REF
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COMPONENT SIDE
LAYER 1
ANALOG DEVICES
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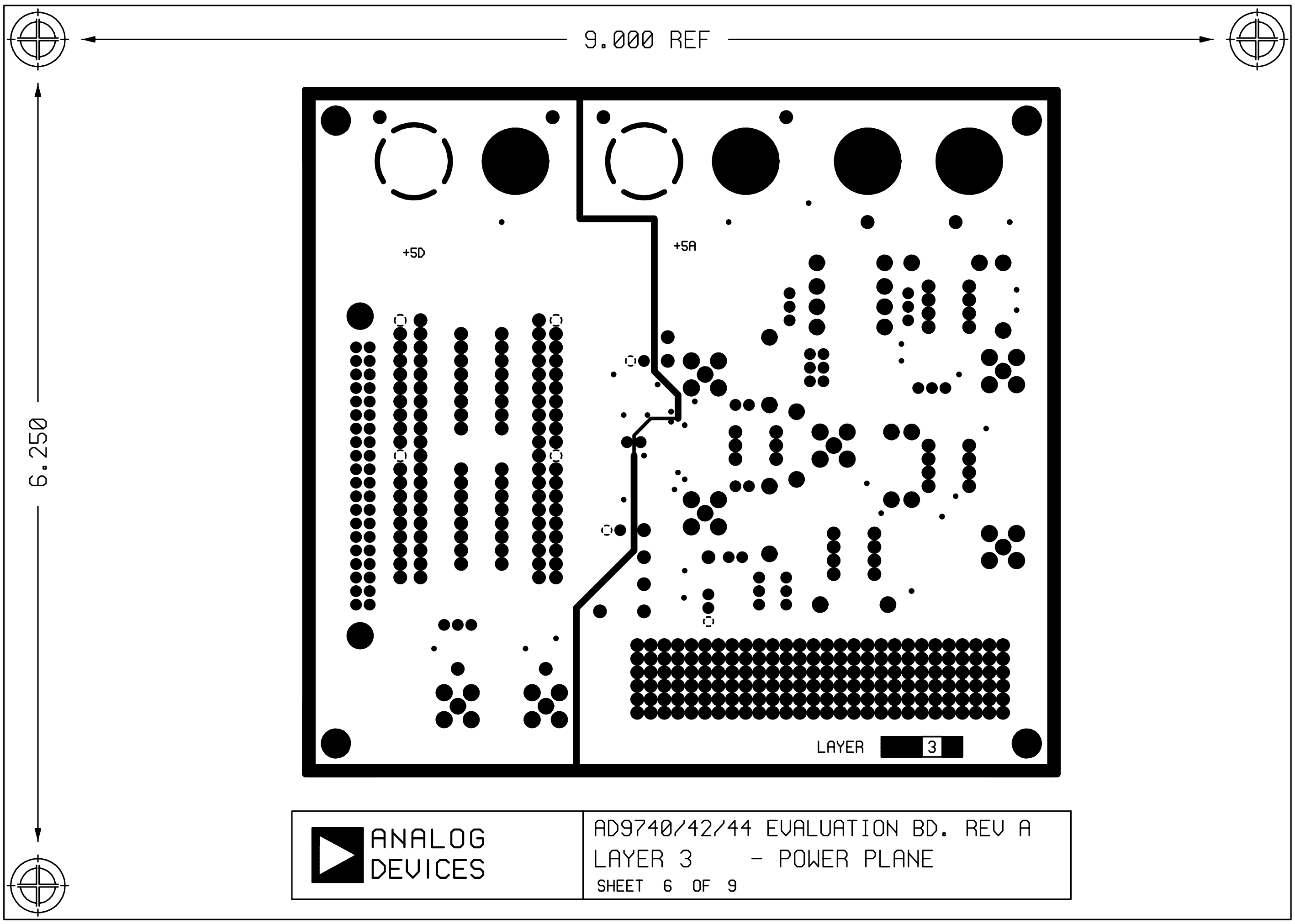
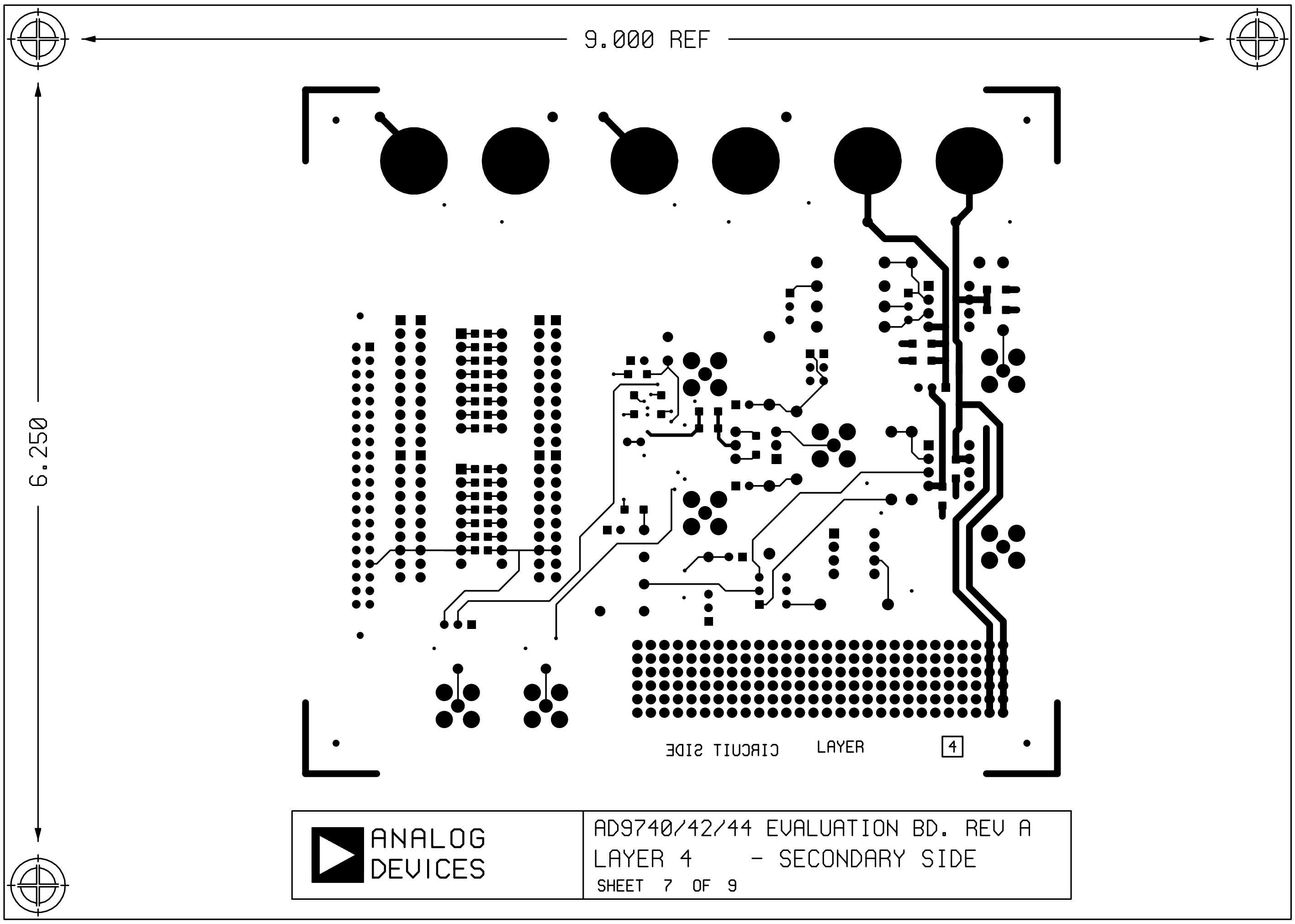
LAYER 1 - PRIMARY SIDE
SHEET 4 OF 9


9.000 REF
6.250
+5D
+5A
LAYER 3
ANALOG DEVICES
AD9740/42/44 EVALUATION BD. REV A
LAYER 3 - POWER PLANE
SHEET 6 OF 9


9.000 REF
6.250
CIRCUIT SIDE
LAYER
4
ANALOG
DEVICES
AD9740/42/44 EVALUATION BD. REV A
LAYER 4 - SECONDARY SIDE
SHEET 7 OF 9