



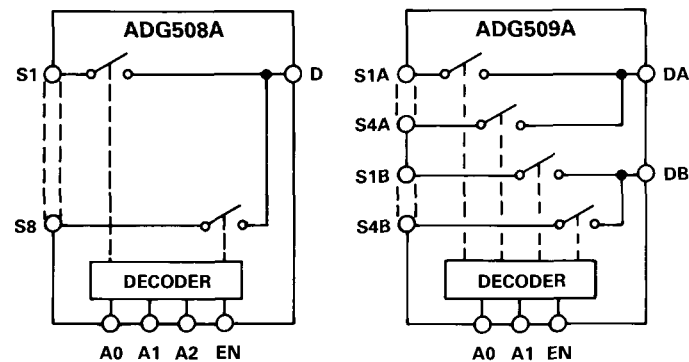
# CMOS 4/8 Channel Analog Multiplexers

## ADG508A/ADG509A

### FEATURES

- 44V Supply Maximum Rating
- $V_{SS}$  to  $V_{DD}$  Analog Signal Range
- Single/Dual Supply Specifications
- Wide Supply Ranges (10.8V to 16.5V)
- Extended Plastic Temperature Range  
( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
- Low Power Dissipation (28mW max)
- Low Leakage (20pA typ)
- Available in 16-Lead DIP/SOIC and  
20-Lead PLCC/LCCC Packages
- Superior Alternative to:  
DG508A, HI-508  
DG509A, HI-509

### FUNCTIONAL BLOCK DIAGRAMS



### GENERAL DESCRIPTION

The ADG508A and ADG509A are CMOS monolithic analog multiplexers with 8 channels and dual 4 channels respectively. The ADG508A switches one of 8 inputs to a common output depending on the state of three binary addresses and an enable input. The ADG509A switches one of 4 differential inputs to a common differential output depending on the state of two binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG508A and ADG509A are designed on an enhanced LC<sup>2</sup>MOS process which gives an increased signal capability of  $V_{SS}$  to  $V_{DD}$  and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low  $R_{ON}$ .

### PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:  
The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Extended Signal Range:  
The enhanced LC<sup>2</sup>MOS processing results in a high breakdown and an increased analog signal range of  $V_{SS}$  to  $V_{DD}$ .
3. Break-Before-Make Switching:  
Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
4. Low Leakage:  
Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

### ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Option <sup>2</sup>
ADG508AKN	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	N-16
ADG508AKR	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	R-16A
ADG508AKP	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	P-20A
ADG508ABQ	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Q-16
ADG508ATQ	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Q-16
ADG508ATE	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	E-20A
ADG509AKN	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	N-16
ADG509AKR	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	R-16A
ADG509AKP	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	P-20A
ADG509ABQ	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Q-16
ADG509ATQ	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Q-16
ADG509ATE	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	E-20A

### NOTES

- <sup>1</sup>To order MIL-STD-883, Class B processed parts, add /883B to part number. See Analog Devices Military Products Databook (1990) for military data sheet.  
<sup>2</sup>E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = 0.15" Small Outline IC (SOIC).

### REV. B

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# ADG508A/ADG509A—SPECIFICATIONS

**DUAL SUPPLY** ( $V_{DD} = +10.8V$  to  $+16.5V$ ,  $V_{SS} = -10.8V$  to  $-16.5V$  unless otherwise specified)

Parameter	ADG508A ADG509A K Version		ADG508A ADG509A B Version		ADG508A ADG509A T Version		Units	Comments
	+25°C	-40°C to +85°C	25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
<b>ANALOG SWITCH</b>								
Analog Signal Range	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	V min V max	
$R_{ON}$	280 450 300	600 400	280 450 300	600 400	280 450 300	600 400	$\Omega$ typ $\Omega$ max $\Omega$ max $\Omega$ max	-10V $\leq$ $V_S$ $\leq$ +10V, $I_{DS} = 1mA$ ; Test Circuit 1  $V_{DD} = 15V(\pm 10\%)$ , $V_{SS} = -15V(\pm 10\%)$ $V_{DD} = 15V(\pm 5\%)$ , $V_{SS} = -15V(\pm 5\%)$
$R_{ON}$ Drift	0.6		0.6		0.6		%/°C typ	$V_S = 0$ , $I_{DS} = 1mA$
$R_{ON}$ Match	5		5		5		% typ	-10V $\leq$ $V_S$ $\leq$ +10V, $I_{DS} = 1mA$
$I_S$ (OFF), Off Input Leakage	0.02 1	50	0.02 1	50	0.02 1	50	nA typ nA max	$V_1 = \pm 10V$ , $V_2 = \mp 10V$ ; Test Circuit 2
$I_D$ (OFF), Off Output Leakage	0.04 1	100	0.04 1	100	0.04 1	100	nA typ nA max	$V_1 = +10V$ , $V_2 = \mp 10V$ ; Test Circuit 3
ADG509A	1	50	1	50	1	50	nA max	
$I_D$ (ON), On Channel Leakage	0.04 1	100	0.04 1	100	0.04 1	100	nA typ nA max	$V_1 = V_2 = \pm 10V$ ; Test Circuit 4
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
$I_{DIFF}$ , Differential Off Output Leakage (ADG509A only)		25		25		25	nA max	$V_1 = \pm 10V$ , $V_2 = \mp 10V$ ; Test Circuit 5
<b>DIGITAL CONTROL</b>								
$V_{INH}$ , Input High Voltage		2.4		2.4		2.4	V min	
$V_{INL}$ , Input Low Voltage		0.8		0.8		0.8	V max	
$I_{INL}$ or $I_{INH}$		1		1		1	$\mu A$ max	$V_{IN} = 0$ to $V_{DD}$
$C_{IN}$ Digital Input Capacitance	8		8		8		pF max	
<b>DYNAMIC CHARACTERISTICS</b>								
$t_{TRANSITION}^1$	200 300	400	200 300	400	200 300	400	ns typ ns max	$V_1 = \pm 10V$ , $V_2 = \mp 10V$ ; Test Circuit 6
$t_{OPEN}^1$	50 25	10	50 25	10	50 25	10	ns typ ns min	Test Circuit 7
$t_{ON}(EN)^1$	200 300	400	200 300	400	200 300	400	ns typ ns max	Test Circuit 8
$t_{OFF}(EN)^1$	200 300	400	200 300	400	200 300	400	ns typ ns max	Test Circuit 8
OFF Isolation	68 50		68 50		68 50		dB typ dB min	$V_{EN} = 0.8V$ , $R_L = 1k\Omega$ , $C_L = 15pF$ , $V_S = 7V$ rms, $f = 100kHz$
$C_S$ (OFF)	5		5		5		pF typ	$V_{EN} = 0.8V$
$C_D$ (OFF)								
ADG508A	22		22		22		pF typ	$V_{EN} = 0.8V$
ADG509A	11		11		11		pF typ	
$Q_{INJ}$ , Charge Injection	4		4		4		pC typ	$R_S = 0\Omega$ , $V_S = 0$ ; Test Circuit 9
<b>POWER SUPPLY</b>								
$I_{DD}$	0.6	1.5	0.6	1.5	0.6	1.5	mA typ mA max	$V_{IN} = V_{INL}$ or $V_{INH}$
$I_{SS}$	20	0.2	20	0.2	20	0.2	$\mu A$ typ mA max	$V_{IN} = V_{INL}$ or $V_{INH}$
Power Dissipation	10	28	10	28	10	28	mW typ mW max	

NOTE  
<sup>1</sup>Sample tested at 25°C to ensure compliance.  
 Specifications subject to change without notice.

## ADG508A/ADG509A

### SINGLE SUPPLY ( $V_{DD} = +10.8V$ to $+16.5V$ , $V_{SS} = GND = 0V$ unless otherwise noted.)

Parameter	ADG508A ADG509A K Version		ADG508A ADG509A B Version		ADG508A ADG509A T Version		Units	Comments	
	-40°C to +25°C +85°C		-40°C to +25°C +85°C		-55°C to +25°C +125°C				
<b>ANALOG SWITCH</b>									
Analog Signal Range	GND	GND	GND	GND	GND	GND	V min V max	$GND \leq V_S \leq +10V$ , $I_{DS} = 0.5mA$ Test; Circuit 1  $V_S = 0$ , $I_{DS} = 0.5mA$ $GND \leq V_S \leq +10V$ , $I_{DS} = 0.5mA$  $V_1 = +10V/GND$ , $V_2 = GND/+10V$ , Test Circuit 2  $V_1 = +10V/GND$ , $V_2 = GND/+10V$ ; Test Circuit 3  $V_1 = V_2 = +10V/GND$ ; Test Circuit 4  $V_1 = +10V/GND$ , $V_2 = GND/+10V$ ; Test Circuit 5  $V_{IN} = 0$ to $V_{DD}$  $V_1 = +10V/GND$ , $V_2 = GND/+10V$ ; Test Circuit 6  $V_{EN} = 0.8V$ , $R_L = 1k\Omega$ , $C_L = 15pF$ , $V_S = 3.5V$ rms, $f = 100kHz$  $V_{EN} = 0.8V$  $V_{EN} = 0.8V$  $R_S = 0\Omega$ , $V_S = 0V$ ; Test Circuit 9	
$R_{ON}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$\Omega$ typ $\Omega$ max		
$R_{ON}$ Drift	500	1000	500	1000	500	1000	%/°C typ		
$R_{ON}$ Match	0.6		0.6		0.6		% typ		
$I_S$ (OFF), Off Input Leakage	5		5		5		nA typ nA max		
$I_D$ (OFF), Off Output Leakage	0.02		0.02		0.02		nA typ nA max		
ADG508A	1	100	1	100	1	100	nA max		
ADG509A	1	50	1	50	1	50	nA max		
$I_D$ (ON), On Channel Leakage	0.04		0.04		0.04		nA typ nA max nA max		
ADG508A	1	100	1	100	1	100	nA max		
ADG509A	1	50	1	50	1	50	nA max		
$I_{DIFF}$ , Differential Off Output Leakage (ADG509A only)		25		25		25	nA max		
<b>DIGITAL CONTROL</b>									
$V_{INH}$ , Input High Voltage		2.4		2.4		2.4	V min		
$V_{INL}$ , Input Low Voltage		0.8		0.8		0.8	V max		
$I_{INL}$ or $I_{INH}$		1		1		1	$\mu A$ max		
$C_{IN}$ Digital Input Capacitance	8		8		8		pF max		
<b>DYNAMIC CHARACTERISTICS</b>									
$t_{TRANSITION}^1$	300		300		300		ns typ ns max		
$t_{OPEN}^1$	450	600	450	600	450	600	ns typ ns min		
$t_{ON}(EN)^1$	50		50		50		ns typ ns max		
$t_{OFF}(EN)^1$	25	10	25	10	25	10	ns typ ns max		
OFF Isolation	250		250		250		dB typ dB min		
$C_S$ (OFF)	450	600	450	600	450	600	pF typ		
$C_D$ (OFF)	250		250		250		pF typ		
ADG508A	450	600	450	600	450	600	pF typ		
ADG509A	250		250		250		pF typ		
$Q_{INJ}$ , Charge Injection	450	600	450	600	450	600	pC typ		
<b>POWER SUPPLY</b>									
$I_{DD}$	0.6		0.6		0.6		mA typ mA max		
Power Dissipation		1.5		1.5		1.5	mW typ mW max		

NOTE  
<sup>1</sup>Sample tested at 25°C to ensure compliance.  
 Specifications subject to change without notice.

#### TERMINOLOGY

$R_{ON}$  Ohmic resistance between terminals D and S  
 $R_{ON}$  Match Difference between the  $R_{ON}$  of any two channels  
 $R_{ON}$  Drift Change in  $R_{ON}$  versus temperature  
 $I_S$  (OFF) Source terminal leakage current when the switch is off  
 $I_D$  (OFF) Drain terminal leakage current when the switch is off  
 $I_D$  (ON) Leakage current that flows from the closed switch into the body  
 $V_S$  ( $V_D$ ) Analog voltage on terminal S or D  
 $C_S$  (OFF) Channel input capacitance for "OFF" condition  
 $C_D$  (OFF) Channel output capacitance for "OFF" condition

$C_{IN}$  Digital input capacitance  
 $t_{OFF}(EN)$  Delay time between the 50% and 10% points of the digital input and switch "OFF" condition  
 $t_{TRANSITION}$  Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another  
 $t_{OPEN}$  "OFF" time measured between 50% points of both switches when switching from one address state to another  
 $V_{INL}$  Maximum input voltage for Logic "0"  
 $V_{INH}$  Minimum input voltage for Logic "1"  
 $I_{INL}$  ( $I_{INH}$ ) Input current of the digital input  
 $V_{DD}$  Most positive voltage supply  
 $V_{SS}$  Most negative voltage supply  
 $I_{DD}$  Positive supply current  
 $I_{SS}$  Negative supply current

# ADG508A/ADG509A

## ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = 25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> . . . . .	44V
V <sub>DD</sub> to GND . . . . .	25V
V <sub>SS</sub> to GND . . . . .	-25V
Analog Inputs <sup>1</sup>	
Voltage at S, D . . . . .	V <sub>SS</sub> - 2V to V <sub>DD</sub> + 2V or 20mA, Whichever Occurs First
Continuous Current, S or D . . . . .	20mA
Pulsed Current S or D . . . . .	40mA
I <sub>ms</sub> Duration, 10% Duty Cycle . . . . .	40mA
Digital Inputs <sup>1</sup>	
Voltage at A, EN . . . . .	V <sub>SS</sub> - 4V to V <sub>DD</sub> + 4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C . . . . .	470mW
Derates above +75°C by . . . . .	6mW/°C
Operating Temperature	
Commercial (K Version) . . . . .	-40°C to +85°C
Industrial (B Version) . . . . .	-40°C to +85°C
Extended (T Version) . . . . .	-55°C to +125°C
Storage Temperature Range . . . . .	-65°C to +150°C

### NOTE

<sup>1</sup>Overvoltage at A, EN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

## TRUTH TABLES

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

### ADG508A

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

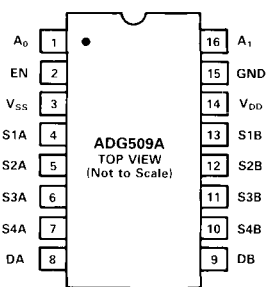
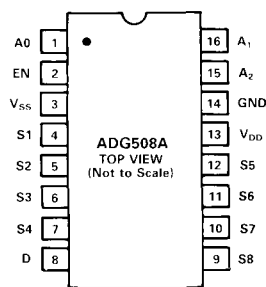
X = Don't Care

### ADG509A

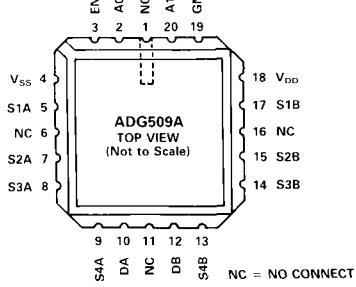
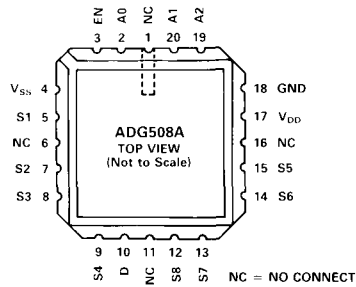


## PIN CONFIGURATIONS

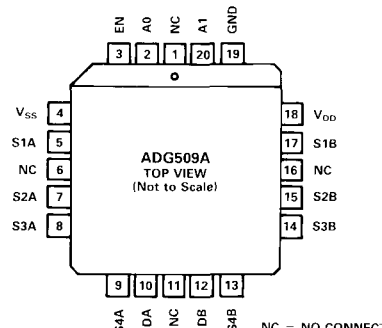
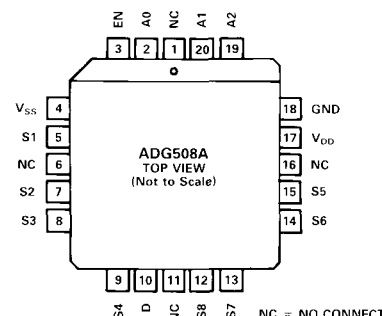
### DIP, SOIC



### LCCC

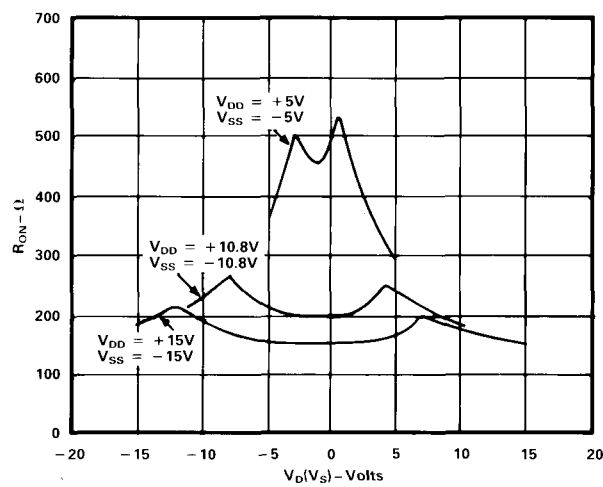


### PLCC

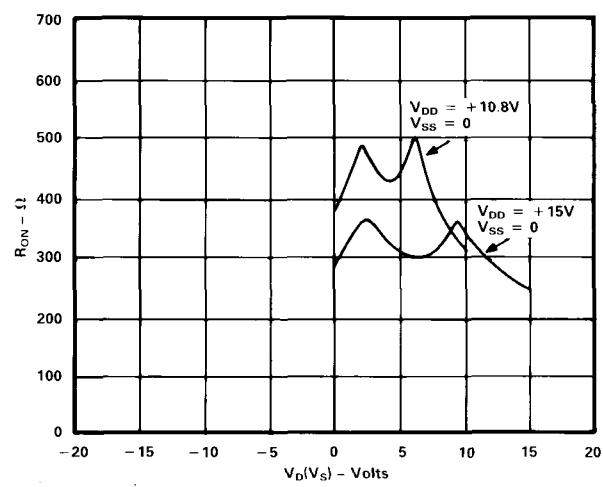


## Typical Performance Characteristics—ADG508A/ADG509A

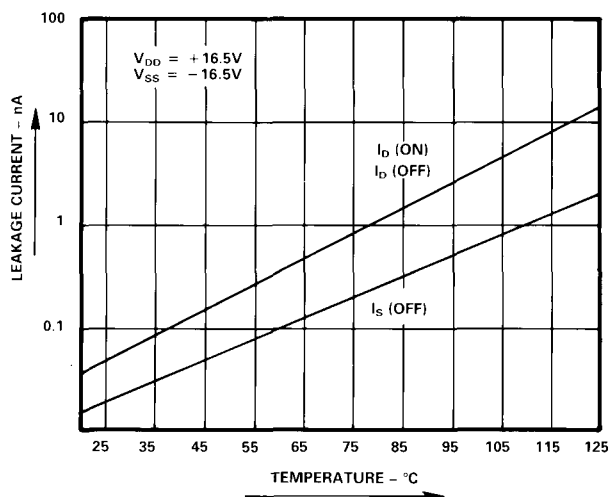
The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5V.



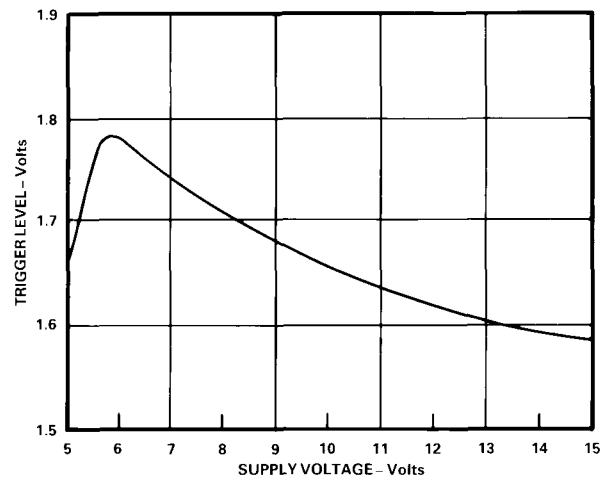
$R_{ON}$  as a Function of  $V_D(V_S)$ : Dual Supply Voltage,  $T_A = +25^\circ\text{C}$



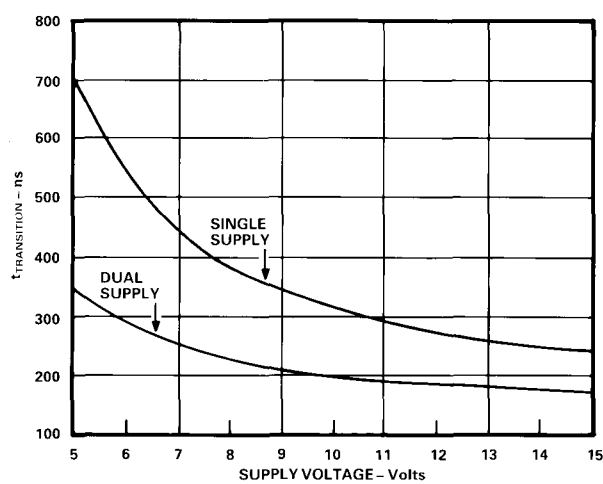
$R_{ON}$  as a Function of  $V_D(V_S)$ : Single Supply Voltage,  $T_A = +25^\circ\text{C}$



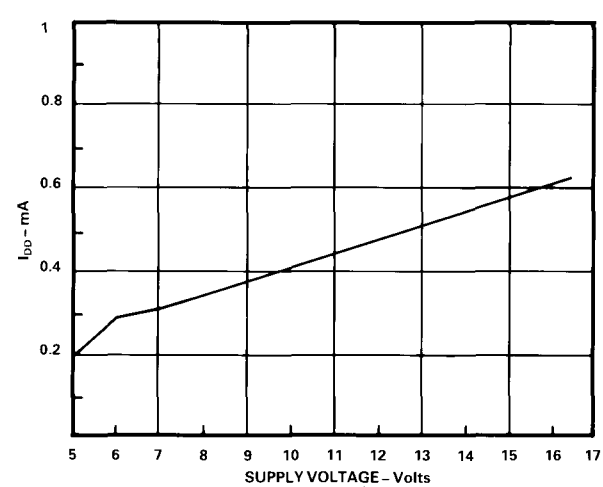
Leakage Current as a Function of Temperature  
(Note: Leakage Currents Reduce as the Supply Voltages Reduce)



Trigger Levels vs. Power Supply Voltage, Dual or Single Supply,  $T_A = +25^\circ\text{C}$



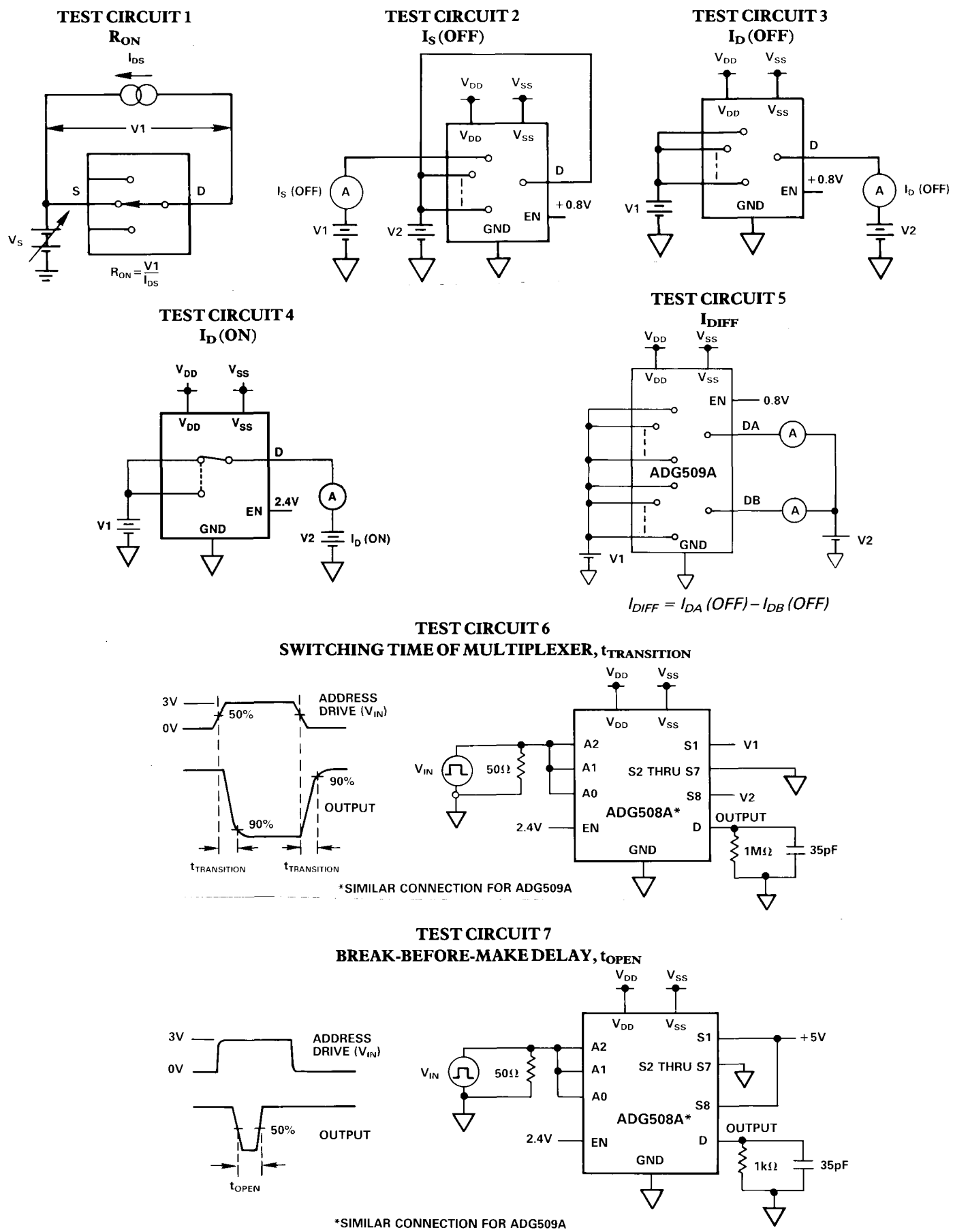
$t_{TRANSITION}$  vs. Supply Voltage: Dual and Single Supplies,  $T_A = +25^\circ\text{C}$   
(Note: For  $V_{DD}$  and  $|V_{SS}| < 10\text{V}$ ;  $V1 = V_{DD}/V_{SS}$ ,  $V2 = V_{SS}/V_{DD}$ . See Test Circuit 6)



$I_{DD}$  vs. Supply Voltage: Dual or Single Supply,  $T_A = +25^\circ\text{C}$

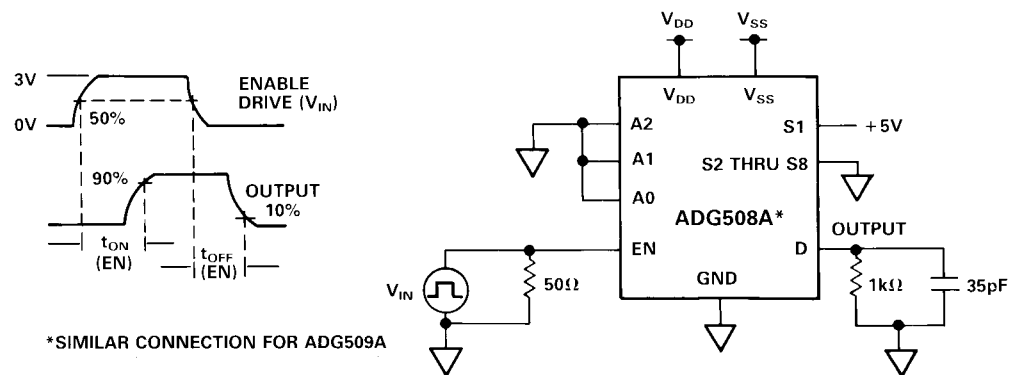
## ADG508A/ADG509A — Test Circuits

Note: All Digital Input Signal Rise and Fall Times Measured from 10% to 90% of 3V.  $t_R = t_F = 20\text{ns}$ .

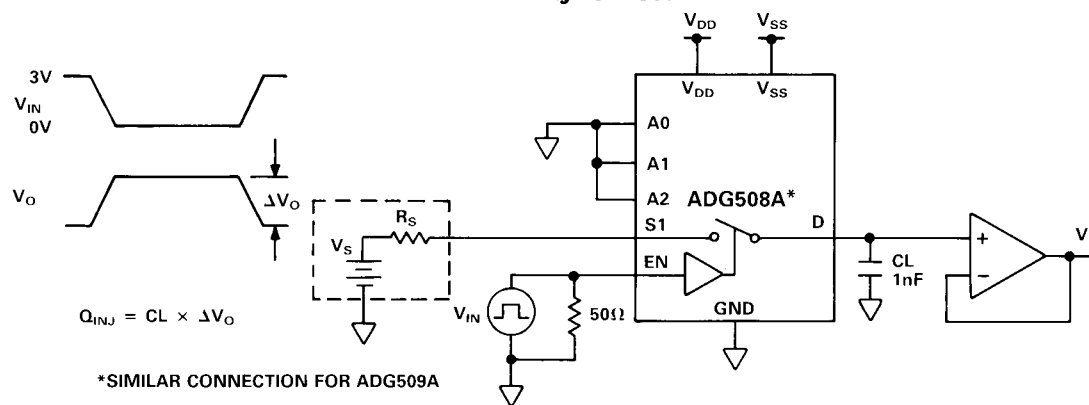


## ADG508A/ADG509A

### TEST CIRCUIT 8 ENABLE DELAY, $t_{ON}(EN)$ , $t_{OFF}(EN)$



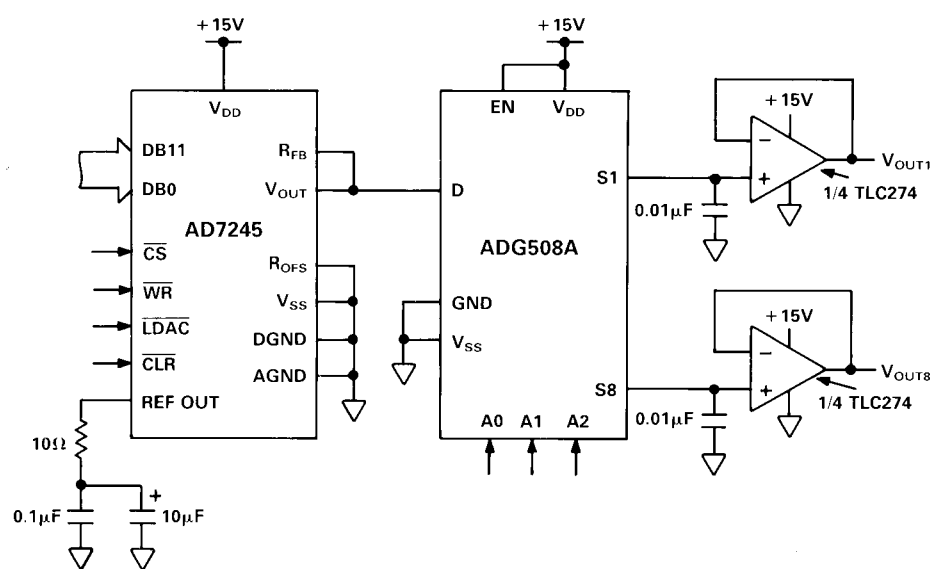
### TEST CIRCUIT 9 CHARGE INJECTION



#### SINGLE SUPPLY OCTAL DAC APPLICATION

The following circuit shows the ADG508A connected as a demultiplexer to provide eight separate digitally programmable voltages (0 to +10V) from the AD7245. The AD7245 is a complete 12-bit, voltage output DAC with output amplifier and Zener

voltage reference on a monolithic CMOS chip. The entire system operates from a single +15V power supply. The ADG508A is ideally suited for the application because it has both low charge injection and  $I_S$  (OFF) leakage current.



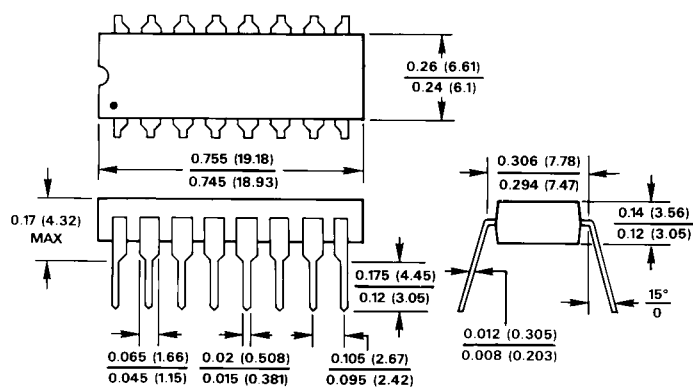
*ADG508A in a Single-Supply Octal DAC Circuit*

# ADG508A/ADG509A

## MECHANICAL INFORMATION OUTLINE DIMENSIONS

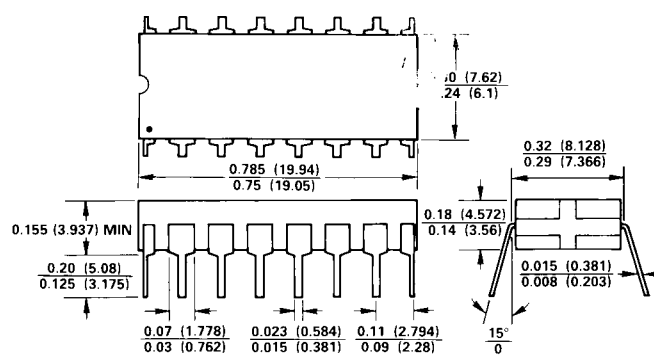
Dimensions shown in inches and (mm).

### 16-Pin Plastic (N-16)



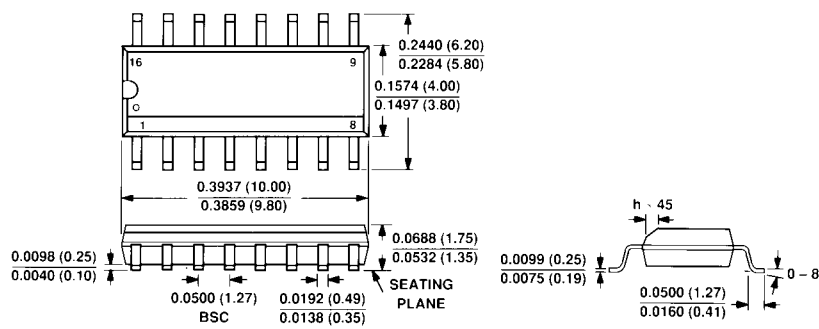
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH  
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

### 16-Pin Cerdip (Q-16)

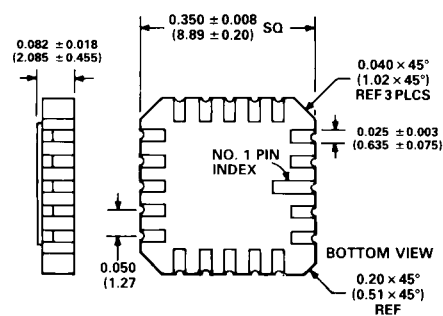


NOTES:  
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.  
LEADS ARE SOLDER OF TIN-PLATED KOVAR OR ALLOY 42

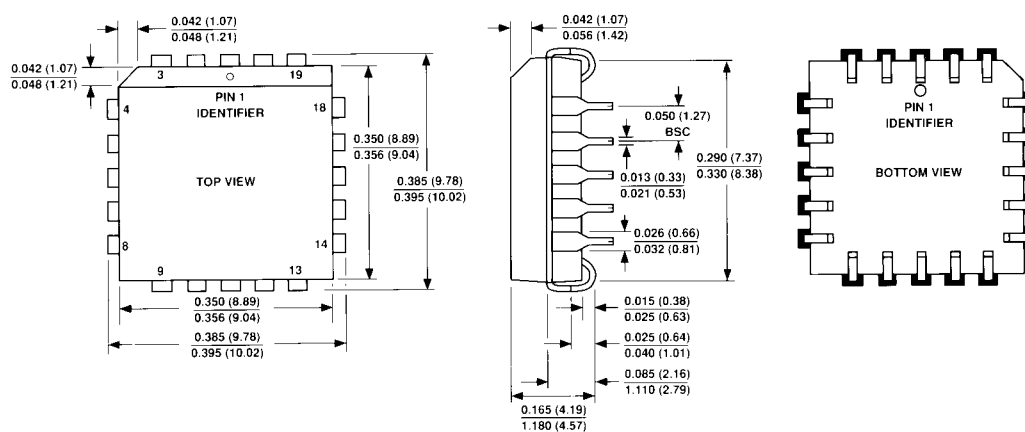
### 16-Lead Narrow Body SOIC (R-16A)



### 20-Terminal Leadless Ceramic Chip Carrier (E-20A)



### 20-Terminal Plastic Leaded Chip Carrier (P-20A)



C104a-9-11/87

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