3-Phase IMVP-II and IMVP-III Core Controller for Mobile CPUs

ADP3204*

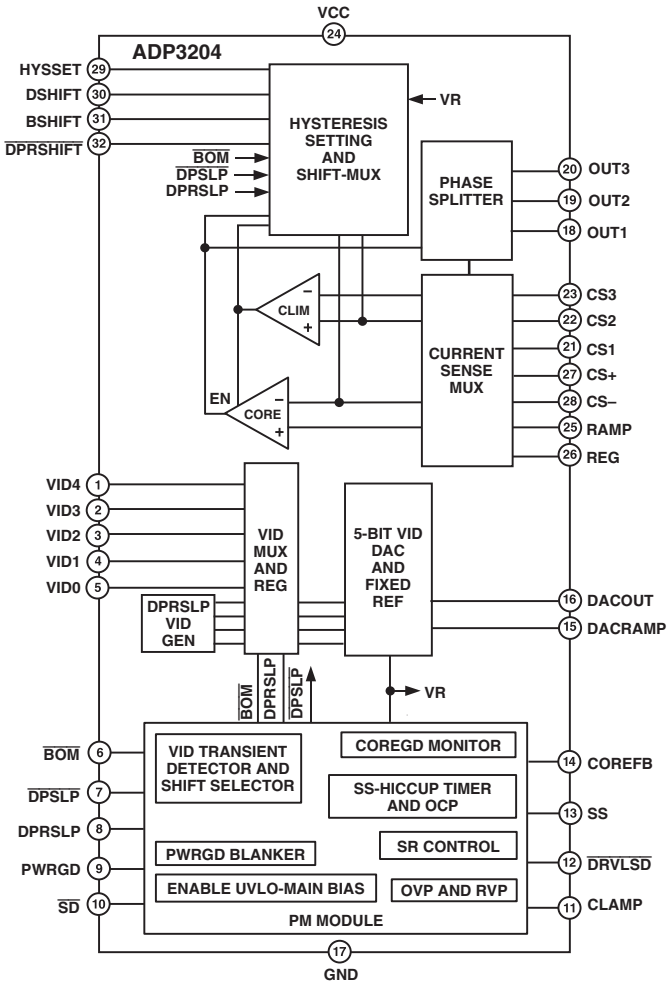
FEATURES

Pin Selectable 1-, 2-, or 3-Phase Operation
Static and Dynamic Current Sharing Characteristics
Backward Compatible to IMVP-II
Superior Load Transient Response with ADOPT®
Analog Devices' Optimal Positioning Technology
Noise-Blanking for Speed and Stability
Synchronous Rectifier Control Extends Battery Life
Smooth Output Transition During VID Code Change
Cycle-by-Cycle Current Limiting
Hiccup or Latched Overload Protection
Transient-Glitch-Free Power Good
Soft Start Eliminates Power-On In-Rush Current Surge
Two-Level Overvoltage and Reverse Voltage Protection

APPLICATIONS

IMVP-II and IMVP-III Core DC-to-DC Converters
Fixed Voltage Mobile CPU Core DC-to-DC Converters
Notebook/Laptop Power Supplies
Programmable Output Power Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3204 is a 1-, 2-, or 3-phase hysteretic peak current dc-to-dc buck converter controller dedicated to power a mobile processor's core. The optimized low voltage design is powered from the 3.3 V system supply. The nominal output voltage is set by a 5-bit VID code. To accommodate the transition time required by the newest processors, the ADP3204 features high speed operation to allow a minimized inductor size that results in the fastest change of current to the output. To further allow for the minimum number of output capacitors to be used, the ADP3204 features active voltage positioning with ADOPT optimal compensation to ensure a superior load transient response. The output signals interface with a maximum of three ADP3415 MOSFET drivers that are optimized for high speed and high efficiency for driving both the top and bottom MOSFETs of the buck converter. The ADP3204 is capable of controlling the synchronous rectifiers to extend battery lifetime in light load conditions.

ADOPT is a trademark of Analog Devices, Inc.
*Protected by U.S.Patent No. 5,969,657; other patents pending.

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ADP3204–SPECIFICATIONS[1]

(0°C ≤ T_A ≤ 100°C, High (H) = VCC, Low (L) = 0 V, VCC = 3.3 V, $\overline{SD}$ = H, V_{COREFB} = V_{DAC} (V_{DACOUT}), V_{REG} = V_{CS-} = V_{VID} = 1.25 V, $C_{DACRAMP}$ = 100 pF, R_{OUT1} = R_{OUT2} = R_{OUT3} = 100 kΩ, C_{OUT1} = C_{OUT2} = C_{OUT3} = 10 pF, C_{SS} = 0.047 μF, R_{PWRGD} = 680 Ω to 1.2 V, R_{CLAMP} = 5.1 kΩ to VCC, HYSSET, BSHIFT, DSHIFT, and DPRSHIFT are open, $\overline{BOM}$ = H, $\overline{DPSLP}$ = H, DPRLP = L, unless otherwise noted.) Current sunk by a pin has a positive sign, sourced by a pin has a negative sign. Negative sign is disregarded for min and max values.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY-UVLO-SHUTDOWN						
Normal Supply Current	I_{CC}			7	11	mA
UVLO Supply Current	I_{CCUVLO}				425	μA
Shutdown Supply Current	I_{CCSD}	$\overline{SD}$ = L, 3.0 V ≤ VCC ≤ 3.6 V		70		μA
UVLO Threshold		$\overline{SD}$ = H				
	V_{CCH}	V_{CC} ramping up, V_{SS} = 0 V			2.95	V
	V_{CCL}	V_{CC} ramping down, V_{SS} floating	2.60			V
UVLO Hysteresis	V_{CCHYS}			55		mV
Shutdown Threshold (CMOS Input)	V_{SDTH}			V_{CC}/2		V
POWER GOOD						
Core Feedback Threshold Voltage	$V_{COREFBH}$	0.9 V < V_{DAC} < 1.675 V				
		V_{COREFB} ramping up	1.12 V_{DAC}		1.14 V_{DAC}	V
		V_{COREFB} ramping down	1.10 V_{DAC}		1.12 V_{DAC}	V
		V_{COREFB} ramping up	0.88 V_{DAC}		0.90 V_{DAC}	V
		V_{COREFB} ramping down	0.86 V_{DAC}		0.88 V_{DAC}	V
Power Good Output Voltage (Open-Drain Output)	V_{PWRGD}	V_{COREFB} = V_{DACOUT}	0.95 V_{CC}		V_{CC}	V
		V_{COREFB} = 0.8 V_{DACOUT}	0		0.8	V
Masking Time[2]	$t_{PWRGDMSK}$[3]			100		μs
SOFT START/HICCUP TIMER						
Charge/Discharge Current	I_{SS}	V_{SS} = 0 V		–55		μA
		V_{SS} = 0.5 V		1.2		μA
Soft Start Enable/Hiccup Termination Threshold	V_{SSEN}	V_{REG} = 1.25 V, V_{RAMP} = V_{COREFB} = 1.27 V				
		V_{SS} ramping down		200	300	mV
Soft Start Termination/Hiccup Enable Threshold	V_{SSTERM}	V_{RAMP} = V_{COREFB} = 1.27 V, V_{SS} ramping up	1.70	2.00	2.25	V
VID DAC						
VID Input Threshold (CMOS Inputs)	$V_{VID0..4}$			V_{CC}/2		V
VID Input Current (Internal Active Pull-Up)	$I_{VID0..4}$	VID0 to VID4 = L		85		μA
Output Voltage	V_{DAC}	See VID Code, Table 1	0.600		1.750	V
Accuracy	$\Delta V_{DAC}/V_{DAC}$					
		1.750 V ≥ V_{DAC} ≥ 0.850 V	–1.0		+1.0	%
		0.825 V ≥ V_{DAC} ≥ 0.600 V	–8.5		+8.5	mV
Settling Time	t_{DACS}[4]	$C_{DACRAMP}$ = 100 pF		3.5		μs
		$C_{DACRAMP}$ = 1 nF		25		μs
DACRAMP Inner Resistance[5]	$R_{DACRAMP}$			10		kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CORE COMPARATOR						
Input Offset Voltage (Ramp-Reg)	V_{COREOS}	V_{REG} = 1.25 V		±1.5		mV
Input Bias Current	I_{REG}, I_{RAMP}	V_{REG} = V_{RAMP} = 1.25 V		±1		µA
Output Voltage	V_{OUT_H}	V_{CC} = 3.0 V	2.5		3.0	V
(OUT1, OUT2, and OUT3)	V_{OUT_L}	V_{CC} = 3.6 V	0		0.4	V
Propagation Delay Time	t_{RMPOUT_PD}[6]	T_A = 25°C		35		ns
		T_A = Full Range		45		ns
Rise and Fall Time	t_{OUT_R}[7]			7		ns
(OUT1, OUT2, and OUT3)	t_{OUT_F}[7]			7		ns
Noise Blanking Time	t_{BLNK}	OUT L-H Transition		70		ns
		OUT H-L Transition		130		ns
CURRENT LIMIT COMPARATOR						
Input Offset Voltage	V_{CLIMOS}	V_{CS-} = 1.25 V		±1		mV
Input Bias Current	I_{CS+}, I_{CS-}	V_{CS+} = 1.25 V		–3		µA
Propagation Delay Time	t_{CLPD}[6]	T_A = 25° C		55		ns
		T_A = Full Range		65		ns
CURRENT SENSE MULTIPLEXER						
Trans-Resistance	$R_{CS1-CS+}$,	MUX switch is ON		150		Ω
	$R_{CS2-CS+}$,	MUX switch is OFF		50		MΩ
	$R_{CS3-CS+}$					
Common-Mode Voltage Range		V_{CS1} = V_{CS2} = V_{CS3}	0		2	V
HYSTERESIS SETTING						
Hysteresis Current	I_{RAMP_H},	V_{REG} = 1.25 V				
	$-I_{CS+\_H}$	V_{RAMP} = 1.23 V				
		I_{HYSSET} = 10 µA	–8	–10	–12	µA
		I_{HYSSET} = 100 µA	–85	–100	–115	µA
		V_{RAMP} = 1.27 V				
		I_{HYSSET} = 10 µA	8	10	12	µA
		I_{HYSSET} = 100 µA	85	100	115	µA
Hysteresis Reference Voltage	V_{HYSSET}			V_{DAC}		V
CURRENT LIMIT SETTING						
Hysteresis Current	I_{CS-}	V_{RAMP} = 1.23 V				
		V_{REG} = V_{CS-} = V_{COREFB} = 1.25 V				
		V_{CS+} = 1.23 V				
		I_{HYSSET} = 10 µA	–27	–31.5	–36	µA
		I_{HYSSET} = 100 µA	–270	–301.5	–333	µA
		V_{CS+} = 1.27 V				
		I_{HYSSET} = 10 µA	–18	–21.5	–25	µA
		I_{HYSSET} = 100 µA	–180	–201.5	–223	µA
		V_{CS+} = 1.23 V, $\overline{BOM}$ = L				

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SHIFT SETTING						
Battery-Shift Current	I_{RAMPB}, I_{CS+B}	V_{VID} = 1.25 V I_{BSHIFT} = –100 μA, $\overline{BOM}$ = L $\overline{DPSLP}$ = H	–92.5	–100	–107.5	mA
Battery-Shift Reference Voltage	V_{BSHIFT}			V_{DAC}		V
Deep Sleep-Shift Current	I_{RAMPD}, I_{CS+D}	V_{VID} = 1.25 V I_{DSHIFT} = –100 μA, $\overline{BOM}$ = H $\overline{DPSLP}$ = L	–92.5	–100	–107.5	mA
Deep Sleep-Shift Reference Voltage	V_{DSHIFT}			V_{DAC}		V
Deeper Sleep-Shift Current	I_{REGDPR} $I_{COREFBDPR}$[8]	$I_{DPRSHIFT}$ = –100 μA, DPRSLP = H V_{VID} = 1.25 V, $I_{DPRSHIFT}$ = –100 μA, DPRSLP = H	–90 110	–100 130	–110 150	μA μA
Deeper Sleep-Shift Reference Voltage	$V_{DPRSHIFT}$			V_{DAC}		V
SHIFT CONTROL INPUTS						
$\overline{BOM}$ Threshold (CMOS Input)	V_{BOM}			V_{CC}/2		V
$\overline{DPSLP}$ Threshold (CMOS Input)	V_{DSLP}			V_{CC}/2		V
DPRSLP Mode Threshold[8] (CMOS Input)	V_{DPRSLP}			V_{CC}/2		V
LOW SIDE DRIVE CONTROL						
Output Voltage (CMOS Output)	V_{DRVLSD}	DPRSLP = H DPRSLP = L	0 0.7 V_{CC}		0.4 V_{CC}	V V
Output Current	I_{DRVLSD}	DPRSLP = H, V_{DRVLSD} = 1.5 V DPRSLP = L, V_{DRVLSD} = 1.5 V	+0.4 –0.4			mA mA
OVER/REVERSE VOLTAGE PROTECTION CORE FEEDBACK						
Overvoltage Threshold	$V_{COREFB, OVP}$[9]	V_{COREFB}		2.0		V
Reverse-Voltage Threshold	$V_{COREFB, RVP}$[9]	V_{COREFB}		–0.3		V
Output Current (Open-Drain Output)	I_{CLAMP}	V_{COREFB} = 2.2 V, V_{CLAMP} = 1.5 V V_{COREFB} = V_{DAC}, V_{CLAMP} = 1.5 V	2	6	10	μA mA

NOTES

[1] All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2] Two test conditions: 1) PWRGD is OK but forced to fail by applying an out-of-the-Core Good-window voltage ($V_{COREFB, BAD}$ = 1.0 V at V_{VID} = 1.25 V setting) to the COREFB pin right after the moment that $\overline{BOM}$ or DPRSLP is asserted/de-asserted. PWRGD should not fail immediately only with the specified blanking delay time. 2) PWRGD is forced to fail ($V_{COREFB, BAD}$ = 1.0 V at V_{VID} = 1.25 V setting) but gets into the Core Good-window ($V_{COREFB, GOOD}$ = 1.25 V) right after the moment that $\overline{BOM}$ or DPRSLP is asserted/de-asserted. PWRGD should not go high immediately only with the specified blanking delay time.

[3] Guaranteed by design

[4] Measured from 50% of VID code transition amplitude to the point where V_{DACOUT} settles within ±1% of its steady state value.

[5] Measured between DACRAMP and DACOUT pins.

[6] 40 mVpp amplitude impulse with 20 mV overdrive. Measured from the input threshold intercept point to 50% of the output voltage swing.

[7] Measured between the 30% and 70% points of the output voltage swing.

[8] DPRSLP circuit meets the minimum 30 ns DPRSLPVR signal assertion requirement; guaranteed by design.

[9] COREFB pin has a resistor divider to GND whose resistance is 41.3 kΩ (typ), guaranteed by design.

ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage (VCC) . . . . . –0.3 V to +7 V
All Other Inputs/Outputs . . . . . –0.3 V to V_{CC} + 0.3 V
Junction Temperature Range . . . . . 0°C to +150°C
Junction to Air Thermal Resistance (θ_{JA}) . . . . . 98°C/W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Quantity per Reel
ADP3204JCP-REEL	0°C to 100°C	LFCSP-32	CP-32	5000
ADP3204JCP-REEL7	0°C to 100°C	LFCSP-32	CP-32	1500

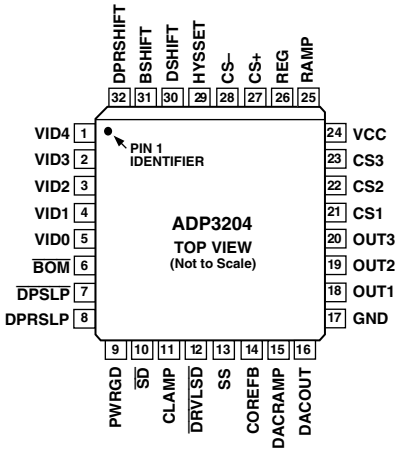
Table I. VID CODE

VID4	VID3	VID2	VID1	VID0	VOUT
0	0	0	0	0	1.750
0	0	0	0	1	1.700
0	0	0	1	0	1.650
0	0	0	1	1	1.600
0	0	1	0	0	1.550
0	0	1	0	1	1.500
0	0	1	1	0	1.450
0	0	1	1	1	1.400
0	1	0	0	0	1.350
0	1	0	0	1	1.300
0	1	0	1	0	1.250
0	1	0	1	1	1.200
0	1	1	0	0	1.150
0	1	1	0	1	1.100
0	1	1	1	0	1.050
0	1	1	1	1	1.000
1	0	0	0	0	0.975
1	0	0	0	1	0.950
1	0	0	1	0	0.925
1	0	0	1	1	0.900
1	0	1	0	0	0.875
1	0	1	0	1	0.850
1	0	1	1	0	0.825
1	0	1	1	1	0.800
1	1	0	0	0	0.775
1	1	0	0	1	0.750
1	1	0	1	0	0.725
1	1	0	1	1	0.700
1	1	1	0	0	0.675
1	1	1	0	1	0.650
1	1	1	1	0	0.625
1	1	1	1	1	0.600

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3204 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1–5	VID[4:0]	Voltage Identification Inputs. These are the VID inputs for logic control of the programmed reference voltage that appears at the DACOUT pin, and, via external component configuration, is used for setting the output voltage regulation point. The VID pins have a specified internal pull-up current that, if left open, will default the pins to a logic high state. The VID code does not set the DAC output voltage directly but through a transparent latch that is clocked by the $\overline{\text{BOM}}$ pin's GMUXSEL signal rising and falling edge.
6	$\overline{\text{BOM}}$	Battery Optimized Mode Control (Active Low). This digital input pin corresponds to the system's GMUXSEL signal that corresponds to Battery Optimized Mode of the CPU operation in its active low state and Performance Optimized Mode (POM) in its deactivated high state. The signal also controls the optimal positioning of the core voltage regulation level by offsetting it downward in Battery Optimized Mode according to the functionality of the BSHIFT and RAMP pins. It is also used to initiate a masking period for the PWRGD signal whenever a GMUXSEL signal transition occurs.
7	$\overline{\text{DPSLP}}$	Deep Sleep Mode Control (Active Low). This is a digital input pin corresponding to the system's $\overline{\text{STPCPU}}$ signal that, in its active state, corresponds to Deep Sleep Mode of the CPU operation, which is a subset operating mode of either $\overline{\text{BOM}}$ or POM operation. The signal controls the optimal positioning of the core voltage regulation level by offsetting it downward according to the functionality of the DSHIFT and RAMP pins.
8	DPRSLP	Deeper Sleep Mode Control (Active High). This is a digital input pin corresponding to the system's DPRSLPVR signal corresponding to Deeper Sleep Mode of the CPU operation. When the signal when it is activated it controls the DAC output voltage by disconnecting the VID signals from the DAC input and setting a specified internal Deeper Sleep code instead. At de-assertion of the DPRSLPVR signal, the DAC output voltage returns to the voltage level determined by the externalVID code. The DPRSLPVR signal is also used to initiate a blanking period for the PWRGD signal to disable its response to a pending dynamic core voltage change that corresponds to the VID code transition.
9	PWRGD	Power Good (Active High). This open-drain output pin, via the assistance of an external pull-up resistor to the desired voltage, indicates that the core voltage is within the specified tolerance of the VID programmed value, or else is in a VID transition state as indicated by a recent state transition of either the $\overline{\text{BOM}}$ or DPRSLP pins. PWRGD is deactivated (pulled low) when the IC is disabled in UVLO mode, or starting up, or the COREFB voltage is out of the core power-good window. The open-drain output allows external wired ANDing (logical NORing) with other open drain/collector power-good indicators.
10	$\overline{\text{SD}}$	Shutdown (Active Low). This is a digital input pin coming from a system signal that, in its active state shuts down the IC operation, placing the IC in its lowest quiescent current state for maximum power savings.

PIN FUNCTION DESCRIPTIONS (continued)

Pin	Mnemonic	Function
11	CLAMP	Clamp (Active High). This is open-drain output pin, via the assistance of an external pull-up resistor, indicates that the core voltage should be clamped for its protection. To allow the highest level of protection, the CLAMP signal is developed using both a redundant reference and a redundant feedback path with respect to those of the main regulation loop. In a preferred and more conservative configuration, the core voltage is clamped by an external FET. The initial protection function is served when it is activated by detection of either an overvoltage or a reverse-voltage condition on the COREFB pin. Due to loss of the latched signal at IC power-off, a backup protection function is served by connecting the pull-up resistor to a system "ALWAYS" regulator output (e.g., V5_ALWAYS). If the external FET is used, this implementation will keep the core voltage clamped until the ADP3204 has power reapplied, thus keeping protection for the CPU even after a hard-failure power-down and restart (e.g., a shorted top or bottom FET).
12	$\overline{\text{DRVLSD}}$	Drive-Low Shutdown (Active Low). In its active state, this digital output pin indicates that the lower FET of the core VR should be disabled. In the suggested application schematic, this pin is directly connected to the pin of the same name on the ADP3415 or other driver IC. Drive-low shutdown is normally activated by the DPRSLP signal corresponding to a light load condition, but a number of dynamic conditions can override the control of this pin as needed.
13	SS	Soft Start. The output of this analog I/O pin is a controlled current source used to charge or discharge an external grounded capacitor; the input is the detected voltage that is indicative of elapsed time. The pin controls the soft start time of the IC as well as the hiccup cycle time during overload, including but not limited to short circuit. Hiccup operation was added to reduce short circuit power dissipation by more than an order of magnitude, while still allowing an automatic restart when the failure mode ceased. The hiccup operation can be overwritten and changed to latched-off operation by clamping the SS pin voltage to a voltage level somewhere above ~ 0.2 V. In this configuration, the controller does not restart after a hiccup cycle is initiated, but stays latched off.
14	COREFB	Core Feedback. This high impedance analog input pin is used to monitor the output voltage for setting the proper state of the PWRGD and CLAMP pins. It is generally recommended to RC-filter the noise from the monitored core voltage, as suggested by the application schematic.
15	DACRAMP	DAC Output Ramp Rate Setting. The rate at which the DAC output voltage can ramp up or down from one voltage to another when the VID code changes can be controlled by an external DACRAMP capacitor connected from this pin to the DACOUT pin. The time constant of the DACOUT voltage variation is determined by the internal resistance appearing across the DACRAMP and DACOUT pins, and the capacitance of the DACRAMP capacitor. Not having any DACRAMP capacitor connected to these pins results in the fastest rate. Use of the DACRAMP rate control and the Deeper Sleep Shift adjustment features are exclusive.
16	DACOUT	Digital-to-Analog Converter Output of the VID input. This output voltage is the VID controlled reference voltage whose primary function is to determine the output voltage regulation point.
17	GND	Ground
18–20	OUT1–3	Outputs to Driver 1–3. These digital output pins are used to command the state of theswitched nodes via the drivers. They should be connected to the IN pin of the drivers of the appropriate channels.
21	CS1	Current Sense, Channel 1. This high impedance analog input pin is used for providing negative feedback of the current information for the first channel.
22	CS2	Current Sense, Channel 2. This high impedance analog input pin is used to provide negative feedback of the current information for the second channel. The pin is also used to determine whether the chip is acting as a single or a multiphase controller. If the CS2 pin is tied to VCC but not to a sense resistor, then three-phase operation is disabled. In this condition, the second phase output signal (OUT2) is not switching but stays static low; the first and third phase output signals (OUT1 and OUT2) are switching in phase. It's the user's discretion to use only one or both of the two signals to drive a single- or dual-channel power stage.
23	CS3	Current Sense, Channel 3. This high impedance analog input pin is used to provide negative feedback of the current information for the third channel. The pin is also used to determine whether the chip is acting as a dual- or three-phase controller. If the pin is tied to VCC but not to a sense resistor, then three-phase operation is disabled; the chip works as a dual-phase controller. In this condition, the third phase output signal (OUT3) is not switching but stays static low; the first and second phase output signals (OUT1, OUT2) are interleaved out-of-phase signals. In single-phase operation, CS3 should be left open instead of being tied to VCC.

PIN FUNCTION DESCRIPTIONS (continued)

Pin	Mnemonic	Function
24	VCC	Power Supply. This should be connected to the system's 3.3 V power supply output.
25	RAMP	Regulation Ramp Feedback Input. The RAMP pin voltage is compared against the REG pin for cycle-by-cycle switching response. Several switched current sources also appear at this input: the cycle-by-cycle hysteresis-setting switched current programmed by the HYSSET pin, the $\overline{\text{BOM}}$ shift current programmed by the BSHIFT pin, and the Deep Sleep shift current programmed by the DSHIFT pin. The external resistive termination at this pin sets the magnitude of the hysteresis applied to the regulation loop.
26	REG	Regulation Voltage Summing Input. This is a high impedance analog input pin into which the voltage reference of the feedback loop allows the summing of both the DACOUT voltage and the core voltage for programming the output resistance of the core voltage regulator. This is also the pin at which an optimized transient response can be tailored using Analog Devices' patented ADOPT design technique.
27	CS+	Current Limit Positive Sense. This high impedance analog I/O pin is multiplexed between either of the three current-sense inputs during the high state of the OUT pin of the respective channel. During the common off-time of both channels, the pin voltage reflects the average of the three channels. The multiplexed current sense signal is passed to the core comparator through an external resistive termination connected from this pin to the RAMP pin. The external (RAMP) resistor sets the magnitude of the hysteresis applied to the regulation loop.
28	CS–	Current Limit Negative Sense. This high impedance analog input pin which is normally Kelvin connected to the negative node of the current sense resistor(s) via a current-limit programming resistor. A hysteretically-controlled current—three times the current programmed at the HYSSET pin—also flows out of this pin and develops a current-limit-setting voltage across that resistor, which must then be matched by the inductor current flowing in the current sensing resistor in order to trigger the current limit function. When triggered, the current flowing out of this pin is reduced to two-thirds of its previous value, producing hysteresis in the current limiting function.
29	HYSSET	Hysteresis Set. This is an analog I/O pin whose output is the VID reference voltage and whose input is a current that is programmed by an external resistance to ground. The current is used in the IC to set the hysteretic currents for the Core Comparator and the Current Limit Comparator. Modification of the resistance will affect both the hysteresis of the feedback regulation, and the current limit set point and hysteresis.
30	DSHIFT	Deep Sleep Shift. This is an analog I/O pin whose output is the VID reference voltage and whose input is a current that is programmed by an external resistance to ground. The current is used in the IC to set a switched bias current out of the RAMP pin, depending on whether it is activated by the $\overline{\text{DSLP}}$ signal. When activated, this added bias current creates a downward shift of the regulated core voltage to a predetermined optimum level for regulation corresponding to Deep Sleep Mode of CPU operation. The use of the DACOUT voltage as the reference makes the Deep Sleep offset a fixed percentage of the VID setting, as required by specifications.
31	BSHIFT	Battery Optimized Mode ($\overline{\text{BOM}}$) Shift. This is an analog I/O pin whose output is the VID reference voltage and whose input current is programmed by an external resistance to ground. The current is used in the IC to set a switched bias current out of the RAMP pin, depending on whether it is activated by the $\overline{\text{BOM}}$ signal. When activated, this added bias current creates a downward shift of the regulated core voltage to a predetermined optimum level for regulation corresponding to Battery Optimized Mode of CPU operation. The use of the DACOUT voltage as the reference makes the DSHIFT a fixed percentage of the VID setting, as required by specifications.

SoftStart and Hiccup
A capacitor from the SS pin to ground determines both the soft start time and the frequency at which hiccup will occur under a continuous short circuit or overload.

System Signal Interface
Several pins of the ADP3204 are meant to connect directly to system signals. The VID pins connect to the system VID control signals. The DPRSLP pin connects to the system's DPRSLPVR signal. The $\overline{\text{DPSLP}}$ pin connects to the system's $\overline{\text{DPSLP}}$ or STPCPU signal. The $\overline{\text{BOM}}$ signal connects to the system's GMUXSEL signal. In an IMVP-II system, the GMUXSEL signal precedes any VID code change with a few nanoseconds, while in an IMVP-III system, it follows it with a maximum 12 µs delay. To comply with both specifications, the ADP3204 has a VID register in front of the DAC inputs that is written by a short pulse generated at the rising or falling edge of the GMUXSEL signal. In an IMVP-II configuration, if the external VID multiplex settling time is longer than the internal VID register's write pulsewidth, then the insertion of an external RC delay network in the GMUXSEL signal path (in front of the $\overline{\text{BOM}}$ pin) is recommended. The Intel specification calls for maximum 200 ns VID code setup time. This specification can be met with a simple RC network that consists of only a 220 kΩ resistor and no external capacitor, just the $\overline{\text{BOM}}$ pin's capacitance.

Undervoltage Lockout
The ADP3204's supply pin, VCC, has undervoltage lockout (UVLO) functionality to ensure that if the supply voltage is too low to maintain proper operation, the IC will remain off and in a low current state.

Overvoltage Protection (OVP) and Reverse Voltage Protection (RVP)
The ADP3204 features a comprehensive redundantly monitored OVP and RVP implementation to protect the CPU core against an excessive or reverse voltage, e.g., as might be induced by a component or connection failure in the control or power stage. Two pins are associated with the OVP/RVP circuitry—a pin for output voltage feedback, COREFB, which is also used for power good monitoring but not for voltage regulation, and an output pin, CLAMP.

The CLAMP pin defaults to a low state at startup of the ADP3204 and remains low until an overvoltage or reverse voltage condition is detected. If either condition is detected, the CLAMP signal is asserted and latched high.

For maximum and fastest protection, the CLAMP pin should be used to drive the gate of a power MOSFET whose drain source is connected across the CPU core voltage. Detection of overvoltage or reverse voltage will clamp the core voltage to essentially zero, thus quickly removing the fault condition and preventing further energy from being applied to the CPU core.

For a less comprehensively protective and less costly solution, the CLAMP pin may be used to latch the disconnection of input power. The latch should be powered whenever any input power source is present. Typically, such a latching circuit is already present in a system design, so it becomes only a matter of allowing the CLAMP pin to also trigger the latch. In this configuration, the latched off state of the system would be indicative of a system failure. The overvoltage/reverse voltage protective means is via not allowing the continued application of energy to the CPU core. The design objective should be, however, to ensure that the CPU core could safely absorb the remaining energy in the power converter, since this energy is not clamped as in the preferred configuration.

LAYOUT CONSIDERATIONS

Advantages in PCB Layout
Analog Devices provides ADP3204/3415 as a dedicated three-phase power management solution for IMVP-III Intel P4 mobile core supply.

This three-phase solution separates the controller (ADP3204) and the MOSFET drivers (ADP3415). Today, most motherboards only leave small pieces of PCB area for the power management circuit. Therefore, the separation of the controller and the MOSFET drivers gives much greater freedom in layout than any single chip solution.

Meanwhile, the separation also provides the freedom to place the analog controller in a relatively quiet area in the motherboard. This can minimize the susceptibility of the controller to injected noise. Any single chip solution with a high speed loop design will suffer larger susceptibility to jitter that appears as modulation of the output voltage.

The ADP3204 maximizes the integration of IMVP-III features. Therefore, no additional externally implemented functions are required to comply with IMVP-III specifications. This saves PCB area for component placement on the motherboard.

PCB Layout Consideration for ADP3204/3415
The following guidelines are recommended for optimal performance of the ADP3204 and ADP3415 in a power converter. The circuitry is considered in three parts: the power switching circuitry, the output filter, and the control circuitry.

Placement Overview
1. For ideal component placement, the output filter capacitors will divide the power switching circuitry from the control section. As an approximate guideline considered on a single-sided PCB, the best layout would have components aligned in the following order: ADP3415, MOSFETs and input capacitor, output inductor, current sense resistor, output capacitors, control components, and ADP3204. Note that the ADP3204 and ADP3415 are completely separated for an ideal layout, which is impossible with a single-chip solution. This keeps the noisy switched power section isolated from the precision control section and gives more freedom in the layout of the power switching circuitry.
2. Whenever a power dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad if possible and immediately surrounding it, is recommended. Two important reasons for this are: improvement of the current rating through the vias (if it is a current path) and improved thermal performance, especially if there is opportunity to spread the heat with a plane on the opposite side of the PCB.