

# Integrated Analog Front-End for Heart Rate Monitors and Low-Cost Pulse Oximeters

Check for Samples: [AFE4400](#)

## FEATURES

- Fully-Integrated Analog Front-End for Pulse Oximeter Applications:
  - Flexible Pulse Sequencing and Timing Control
- Transmit:
  - Integrated LED Driver (H-Bridge or Push/Pull)
  - 95-dB Dynamic Range
  - LED Current:
    - Programmable to 75 mA with 8-Bit Current Resolution
  - Low Power:
    - 100  $\mu$ A + Average LED Current
  - Programmable LED On-Time
  - Independent LED2 and LED1 Current Reference
- Receive Channel with High Dynamic Range:
  - 13 Noise-Free Bits (0.1 Hz to 5 Hz)
  - Low Power: < TBD mA at 3.3-V Supply
  - Flexible Receive Sample Time
  - Flexible Transimpedance Amplifier with Programmable LED Settings
  - Integrated Digital Ambient Estimation and Subtraction
- Integrated Fault Diagnostics:
  - Photodiode and LED Open and Short Detection
  - Cable On/Off Detection
- Supplies:
  - Rx = 2.0 V to 3.6 V
  - Tx = 3.0 V or 3.6 V
- Package: Compact QFN-40 (6 mm  $\times$  6 mm)
- Specified Temperature Range: 0°C to +70°C

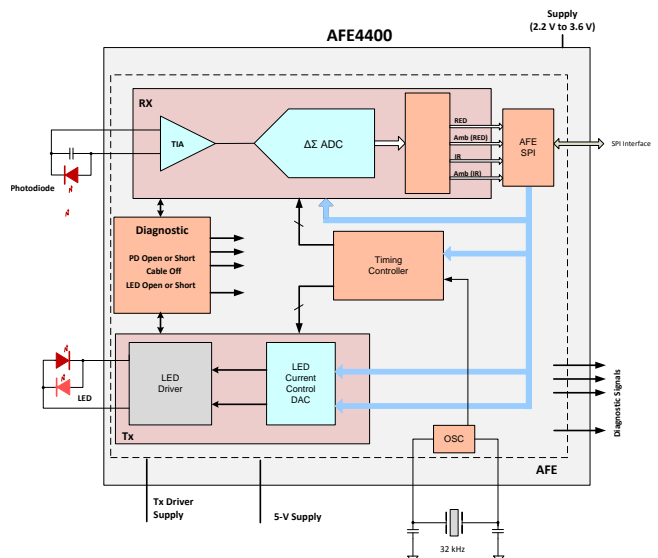
## APPLICATIONS

- Low-Cost Medical Pulse Oximeter Applications
- Optical HRM
- Industrial Photometry Applications

## DESCRIPTION

The AFE4400 is a fully-integrated analog front-end (AFE) that is ideally suited for pulse oximeter applications. The device consists of a low-noise receiver channel with an integrated analog-to-digital converter (ADC), an LED transmit section, and diagnostics for sensor and LED fault detection. The AFE4400 is a very configurable timing controller. This flexibility enables the user to have complete control of the device timing characteristics. To ease clocking requirements and provide a low-jitter clock to the AFE4400, an oscillator is also integrated that functions from an external crystal. The device communicates to an external microcontroller or host processor using an SPI™ interface.

The AFE4400 is a complete AFE solution packaged in a single, compact QFN-40 package (6 mm  $\times$  6 mm) and is specified over the operating temperature range of 0°C to +70°C.


**Figure 1. Block Diagram**


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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	LED DRIVE CONFIGURATION	LED DRIVE CURRENT (mA, max)	POWER SUPPLY (V)	OPERATING TEMPERATURE RANGE
AFE4400CRHA	QFN-40	Bridge, push-pull	75	3	0°C to +70°C

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
AVDD to AVSS		-0.3 to +7	V
DVDD to DGND		-0.3 to +7	V
AGND to DGND		-0.3 to +0.3	V
Analog input to AVSS		AVSS - 0.3 to AVDD + 0.3	V
Digital input to DVDD		DVSS - 0.3 to DVDD + 0.3	V
Input current to any pin except supply pins <sup>(2)</sup>		±10	mA
Input current	Momentary	±100	mA
	Continuous	±10	mA
Operating temperature range		-40 to +95	°C
Storage temperature range, T <sub>stg</sub>		-60 to +150	°C
Maximum junction temperature, T <sub>J</sub>		+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±1000	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±500	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing beyond the supply rails must be current-limited to 10 mA or less.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		AFE4400	UNITS
		RHA (QFN)	
		40 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	35	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	31	
θ <sub>JB</sub>	Junction-to-board thermal resistance	26	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.1	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	n/a	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	n/a	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		VALUE	UNIT
<b>SUPPLIES</b>			
RX_ANA_SUP	AFE analog supply	2.0 to 3.6	V
RX_DIG_SUP	AFE digital supply	2.0 to 3.6	V
TX_CTRL_SUP	Transmit controller supply	3.0 to 3.6	V
LED_DRV_SUP	H-bridge configuration	$[3.0 \text{ or } (1.4 + V_{LED} + V_{CABLE})^{(1)(2)}, \text{ whichever is greater}]$ to 5.25	V
	Common anode configuration	$[3.0 \text{ or } (1.3 + V_{LED} + V_{CABLE})^{(1)(2)}, \text{ whichever is greater}]$ to 5.25	V
Difference between LED_DRV_SUP and TX_CTRL_SUP		-0.3 to +0.3	V
<b>TEMPERATURE</b>			
Specified temperature range		0 to +70	°C
Operating temperature range <sup>(3)</sup>		-40 to +85	°C
Storage temperature range		-60 to +150	°C

- (1)  $V_{LED}$  refers to the voltage drop across the external LED connected between the TXP and TXM pins (in H-bridge mode) and from the TXP and TXM pins to LED\_DRV\_SUP (in the common anode configuration).
- (2)  $V_{CABLE}$  refers to voltage drop across any cable, connector, or any other component in series with the LED.
- (3) Operating temperature range is the temperature range at which the device functions, without damaging the device. Device performance may not meet the temperature specification beyond the specified temperature range.

## ELECTRICAL CHARACTERISTICS

Minimum and maximum specifications are at  $T_A = -20^\circ\text{C}$  to  $+85^\circ\text{C}$ . Typical specifications are at  $+25^\circ\text{C}$ .

All specifications are at  $RX\_ANA\_SUP = RX\_DIG\_SUP = 3.0\text{ V}$ ,  $TX\_CTRL\_SUP = LED\_DRV\_SUP = 3.3\text{ V}$ , and  $f_{CLK} = 8\text{ MHz}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>PERFORMANCE (Full-Signal Chain)</b>						
PRF	Pulse repetition frequency				1300	SPS
	PRF duty cycle				25%	
$I_{IN\_FS}$	Full-scale input current	$R_F = 10\text{ k}\Omega$		50		$\mu\text{A}$
		$R_F = 1\text{ M}\Omega$		0.5		$\mu\text{A}$
CMRR	Common-mode rejection ratio	$f_{CM} = 50\text{ Hz}, 60\text{ Hz}$		TBD		dB
PSRR	Power-supply rejection ratio	$f_{PS} = 50\text{ Hz}, 60\text{ Hz}$		TBD		dB
<b>RECEIVER FUNCTIONAL BLOCK LEVEL SPECIFICATION</b>						
Total integrated noise current, input referred (receiver alone) over 0.1-Hz to 5-Hz bandwidth		$R_F = 500\text{ k}\Omega$ , ambient cancellation enabled, stage 2 gain = 4, PRF = 1300 Hz, LED duty cycle = 25%		1.4		$\text{pA}_{RMS}$
		$R_F = 500\text{ k}\Omega$ , ambient cancellation enabled, stage 2 gain = 4, PRF = 1300 Hz, LED duty cycle = 5%		5		$\text{pA}_{RMS}$
<b>I-V TRANSIMPEDANCE AMPLIFIER</b>						
G	Gain	$R_F = 10\text{ k}\Omega$ to $1\text{ M}\Omega$	TBD		TBD	$\text{V}/\mu\text{A}$
	Feedback resistance	$R_F$	10k, 25k, 50k, 100k, 250k, 500k, and 1M			$\Omega$
	Feedback resistor tolerance	$R_F$		$\pm 20\%$		
	Feedback capacitance	$C_F$	5, 10, 25, 50, 100, and 250			$\text{pF}$
	Feedback capacitor tolerance	$C_F$		$\pm 20\%$		
	Full-scale differential output voltage			1	TBD	V
	Common-mode voltage on input pins	Set internally		0.9		V
	External differential input capacitance	Includes equivalent capacitance of photodiode, cables, EMI filter, and so forth	TBD		1000	$\text{pF}$
	Shield output voltage, $V_{CM}$	With a 1-k $\Omega$ series resistor and a 10-nF decoupling capacitor to ground		0.9		V
<b>AMBIENT CANCELLATION STAGE</b>						
	Gain		1, 1.5, 2, 3, and 4			V/V
	Current DAC range		0		10	$\mu\text{A}$
	Current DAC step size			1		$\mu\text{A}$
<b>LOW-PASS FILTER</b>						
	Low-pass corner frequency	3-dB attenuation		500		Hz
	Pass-band attenuation, 2 Hz to 10 Hz	Duty cycle = 25%		0.004		dB
		Duty cycle = 10%		0.041		dB
<b>ANALOG-TO-DIGITAL CONVERTER</b>						
	Resolution				22	Bits
	Sample rate		TBD		TBD	SPS
	ADC full-scale voltage			$\pm 1.2$		V
	ADC minimum time for conversion			50		$\mu\text{s}$
	ADC reset time		2			$t_{CLK}$

## ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications are at  $T_A = -20^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Typical specifications are at  $+25^{\circ}\text{C}$ .

All specifications are at  $RX\_ANA\_SUP = RX\_DIG\_SUP = 3.0\text{ V}$ ,  $TX\_CTRL\_SUP = LED\_DRV\_SUP = 3.3\text{ V}$ , and  $f_{CLK} = 8\text{ MHz}$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TRANSMITTER</b>					
Output current range		Selectable 0 and 75			mA
LED current DAC error		±10%			
Output current resolution		8			Bits
Transmitter noise dynamic range, over 0.1-Hz to 5-Hz bandwidth	At 25-mA output current	95			dB
Voltage on TXP (or TXM) pin when low-side switch connected to TXP (or TXM) turns on	At 75-mA output current, H-bridge LED driver configuration	TBD + (voltage drop across LED, cable, and so forth) to 5.25			V
	At 75-mA output current, common anode LED driver configuration	TBD + (voltage drop across LED, cable, and so forth) to 5.25			V
Minimum sample time of LED1 and LED2 pulses		50			µs
LED current DAC leakage current	LED_ON = 0	1			µA
	LED_ON = 1	50			µA
Output current settling time (with resistive load)	From zero current to TBD mA	TBD			µs
	From TBD mA to zero current	TBD			µs
<b>DIAGNOSTICS</b>					
Duration of diagnostics state machine	Start of diagnostics after the DIAG_EN register bit is set. End of diagnostic is indicated by DIAG_END going high.	16			4k cycles of 4-MHz clock
Open fault resistance		> TBD			MΩ
Short fault resistance		< TBD			kΩ
<b>INTERNAL OSCILLATOR</b>					
$f_{CLKOUT}$ CLKOUT frequency	With an 8-MHz crystal connected to the XIN, XOUT pins	4			MHz
CLKOUT duty cycle		50%			
Crystal oscillator start-up time	With an 8-MHz crystal connected to the XIN, XOUT pins with TBD-pF load capacitor from each pin to ground	TBD			µs
Oscillator power consumption		TBD			µW
<b>EXTERNAL CLOCK</b>					
Maximum allowable external clock jitter		50			ps

## ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications are at  $T_A = -20^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Typical specifications are at  $+25^{\circ}\text{C}$ .

All specifications are at  $\text{RX\_ANA\_SUP} = \text{RX\_DIG\_SUP} = 3.0\text{ V}$ ,  $\text{TX\_CTRL\_SUP} = \text{LED\_DRV\_SUP} = 3.3\text{ V}$ , and  $f_{\text{CLK}} = 8\text{ MHz}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TIMING</b>						
	Wake-up time from complete power-down			TBD		ms
	Wake-up time from Rx power-down			TBD		$\mu\text{s}$
	Wake-up time from Tx power-down			TBD		$\mu\text{s}$
$t_{\text{RESET}}$	Active low RESET pulse duration			TBD		$\mu\text{s}$
$t_{\text{DIAGEND}}$	DIAG_END pulse duration at the completion of diagnostics			TBD		CLKOUT cycles
$t_{\text{ADCRDY}}$	ADC_RDY pulse duration			TBD		CLKOUT cycles
<b>SPI TIMING</b>						
$f_{\text{SPICLK}}$	SCLK frequency			TBD		MHz
$t_{\text{SPLSU}}$	SPISIMO input data setup time with respect to SCLK rising edge			TBD		ns
$t_{\text{SPLHO}}$	SPISIMO input data hold time with respect to SCLK rising edge			TBD		ns
$t_{\text{SOMI\_VAL}}$	SPISOMI output data valid time			TBD		ns
$t_{\text{SOMI\_HO}}$	SPISOMI output data hold time			TBD		ns
$t_{\text{RISE}}$	Rise time from 20% to 80%			TBD		ns
$t_{\text{FALL}}$	Fall time from 80% to 20%			TBD		ns
<b>DIGITAL SIGNAL CHARACTERISTICS</b>						
$V_{\text{IH}}$	Logic high input voltage	AFE_PDN, SCLK, SPISIMO, SPISTE, RESET	0.8 DVDD	> 1.3	DVDD + 0.1	V
$V_{\text{IL}}$	Logic low input voltage	AFE_PDN, SCLK, SPISIMO, SPISTE, RESET	-0.1	< 0.4	0.2 DVDD	V
$I_{\text{IN}}$	Logic input current	$0\text{ V} < V_{\text{DigitalInput}} < \text{DVDD}$	-10		10	$\mu\text{A}$
$V_{\text{OH}}$	Logic high output voltage	DIAG_END, LED_ALM, PD_ALM, SPISOMI, ADC_RDY, CLKOUT	0.9 DVDD	> (RX_DIG_SUP - 0.2 V)		V
$V_{\text{OL}}$	Logic low output voltage	DIAG_END, LED_ALM, PD_ALM, SPISOMI, ADC_RDY, CLKOUT		< 0.4	0.1 DVDD	V
<b>SUPPLY CURRENT</b>						
Normal operation	$I_{\text{AVDD}}$	AVDD - AVSS = 5.0 V		TBD		mA
	$I_{\text{DVDD}}$	DVDD = 3.0 V		TBD		mA
Receiver analog supply current		RX_ANA_SUP = 3.0 V, with 8-MHz clock running, Rx stage 2 disabled		0.6		mA
		RX_ANA_SUP = 3.0 V, with 8-MHz clock running, Rx stage 2 enabled		0.9		mA
Receiver digital supply current		RX_DIG_SUP = 3.0 V		0.27		mA
LED_DRV_SUP	LED driver supply current	With zero LED current setting		0.1		mA
TX_CTRL_SUP	Transmitter control supply current			0.033		mA
Complete power-down		Receiver current only (RX_ANA_SUP + RX_DIG_SUP)		0.027		mA
		Transmitter current only (LED_DRV_SUP + TX_CTRL_SUP)		0.01		mA
Power-down Rx alone		Receiver current only (RX_ANA_SUP + RX_DIG_SUP)		0.373		mA
Power-down Tx alone		Transmitter current only (LED_DRV_SUP + TX_CTRL_SUP)		0.01		mA
<b>POWER DISSIPATION</b>						
Quiescent power dissipation		Normal operation (excluding LEDs)		1.54		mW
		Power-down		0.1		$\mu\text{W}$

## ELECTRICAL CHARACTERISTICS (continued)

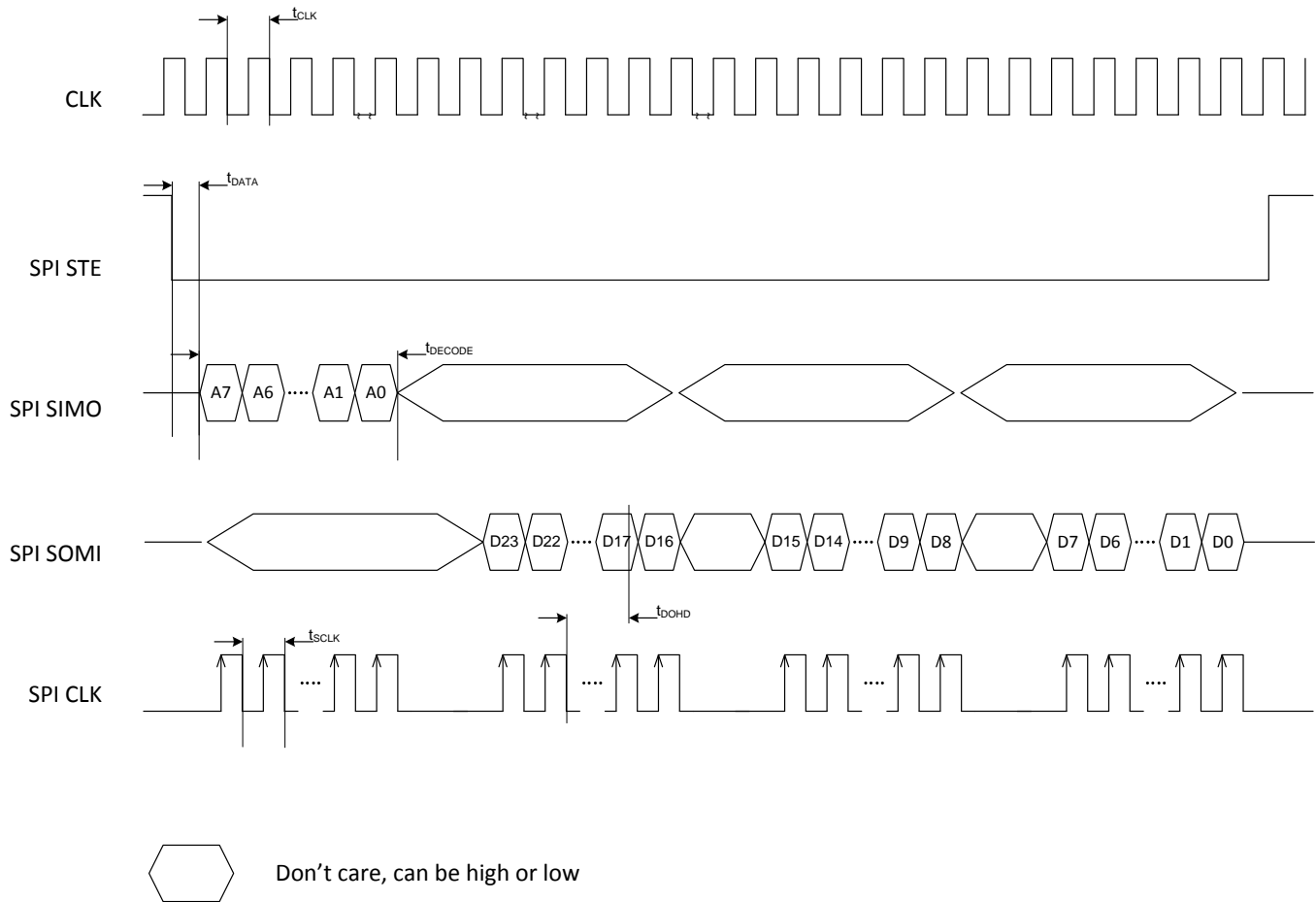
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All specifications are at  $RX\_ANA\_SUP = RX\_DIG\_SUP = 3.0\text{ V}$ ,  $TX\_CTRL\_SUP = LED\_DRV\_SUP = 3.3\text{ V}$ , and  $f_{CLK} = 8\text{ MHz}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-down AFE	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		0.01		mW
	TX_CTRL_SUP			0.01		mW
	RX_ANA_SUP			0.02		mW
	RX_DIG_SUP			0.06		mW
Power-down Rx	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		0.28		mW
	TX_CTRL_SUP			0.1		mW
	RX_ANA_SUP			0.5		mW
	RX_DIG_SUP			0.62		mW
Power-down Tx	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		0.01		mW
	TX_CTRL_SUP			0.01		mW
	RX_ANA_SUP			1.8		mW
	RX_DIG_SUP			0.8		mW
After reset, with 8-MHz clock running	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		0.28		mW
	TX_CTRL_SUP			0.1		mW
	RX_ANA_SUP			1.8		mW
	RX_DIG_SUP			0.8		mW
With stage 2 mode enabled and 8-MHz clock running	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		0.28		mW
	TX_CTRL_SUP			0.1		mW
	RX_ANA_SUP			2.7		mW
	RX_DIG_SUP			0.8		mW

## PARAMETRIC MEASUREMENT INFORMATION

### SERIAL INTERFACE TIMING



- (1) The SPI\_READ register bit must be enabled before attempting a serial readout from the AFE.
- (2) Specify the register address whose contents must be read back on A[7:0].
- (3) The AFE outputs the contents of the specified register on the SOMI pin.

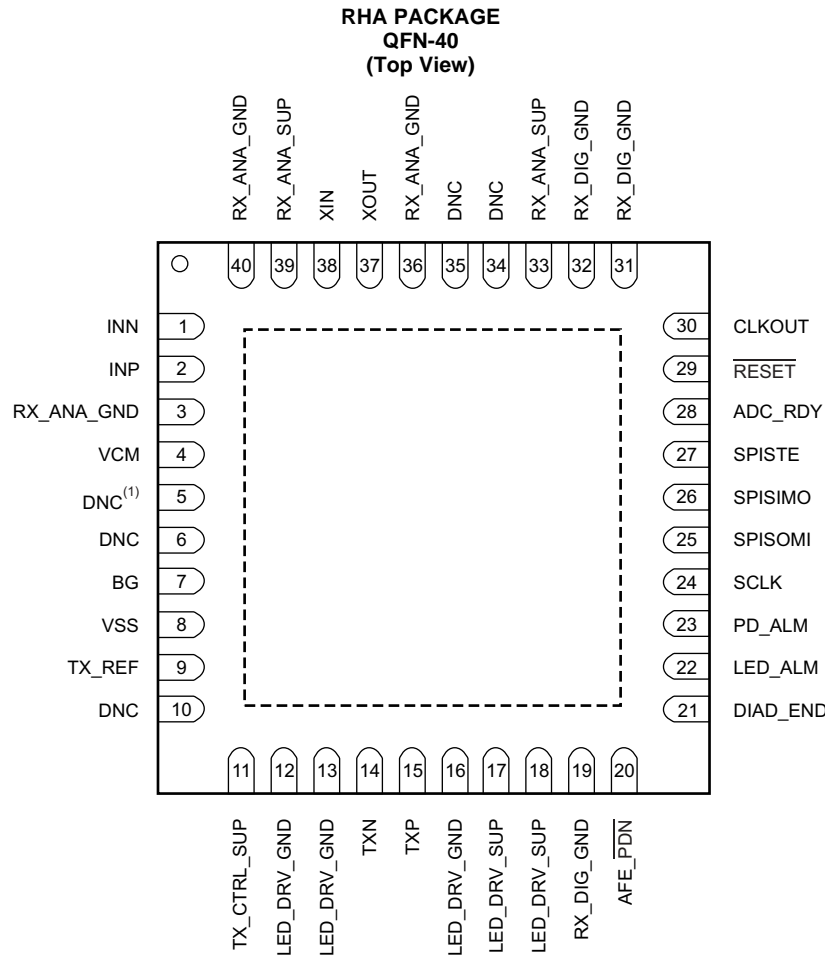
**Figure 2. Serial Interface Timing Diagram<sup>(1)(2)(3)</sup>**

**Table 1. Timing Requirements for Figure 2**

PARAMETER		TBD V ≤ DVDD ≤ TBD V		UNIT
		MIN	MAX	
t <sub>CLK</sub>	Master clock period	TBD	TBD	ns
t <sub>SCLK</sub>	SCLK period	TBD	TBD	ns
t <sub>SPWH, L</sub>	SCLK pulse duration, high and low	TBD	TBD	ns
t <sub>DIST</sub>	SPISIMO valid to SCLK falling edge: setup time	TBD	TBD	ns
t <sub>DIHD</sub>	Valid SPISIMO after SCLK falling edge: hold time	TBD	TBD	ns
t <sub>DOHD</sub>	SCLK falling edge to invalid SPISOMI hold time	TBD	TBD	ns
t <sub>DOST</sub>	SCLK rising edge to SPISOMI valid: setup time	TBD	TBD	ns
t <sub>SPISTE</sub>	SPISTE high pulse	TBD	TBD	ns
t <sub>SDECODE</sub>	Command decode time	TBD	TBD	ns



PIN CONFIGURATION



(4) DNC = Do not connect.

PIN DESCRIPTIONS

NAME	NO.	FUNCTION	DESCRIPTION
ADC_RDY	28	Digital	Output signal that indicates ADC conversion completion. Can be connected to the interrupt input pin of an external microcontroller.
AFE_PDN	20	Digital	AFE-only power-down input; active low. Can be connected to the port pin of an external microcontroller.
BG	7	Reference	Decoupling capacitor for internal band-gap voltage to ground. (2.2-µF decoupling capacitor to ground)
CLKOUT	30	Digital	Buffered 4-MHz output clock output. Can be connected to the clock input pin of an external microcontroller.
DIAG_END	21	Digital	Output signal that indicates completion of diagnostics. Can be connected to the port pin of an external microcontroller.
DNC <sup>(1)</sup>	5, 6, 10, 34, 35	—	Do not connect these pins. Leave as open circuit.
INN	1	Analog	Receiver input pin. Connect to photodiode anode.
INP	2	Analog	Receiver input pin. Connect to photodiode cathode.
LED_DRV_GND	12, 13, 16	Supply	LED driver ground pin, H-bridge. Connect to common board ground.
LED_DRV_SUP	17, 18	Supply	LED driver supply pin, H-bridge. Connect a TBD-µF bulk capacitor to ground.
LED_ALM	22	Digital	Output signal that indicates an LED cable fault. Can be connected to the port pin of an external microcontroller.
PD_ALM	23	Digital	Output signal that indicates a PD sensor or cable fault. Can be connected to the port pin of an external microcontroller.

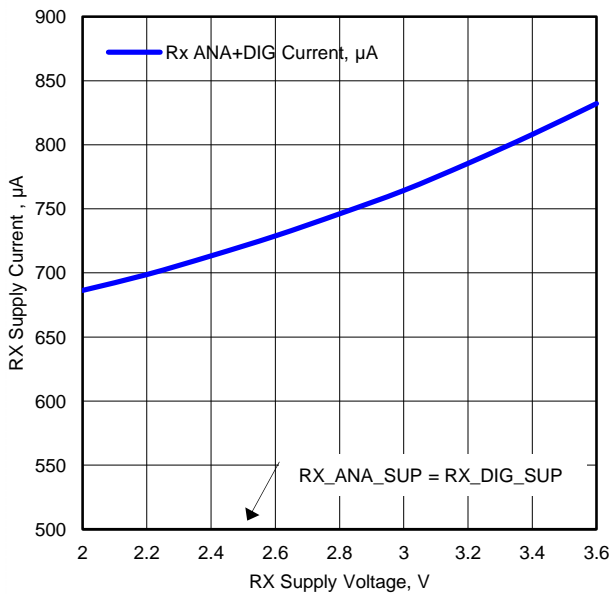
(1) Leave pins as open circuit. Do not connect.

**PIN DESCRIPTIONS (continued)**

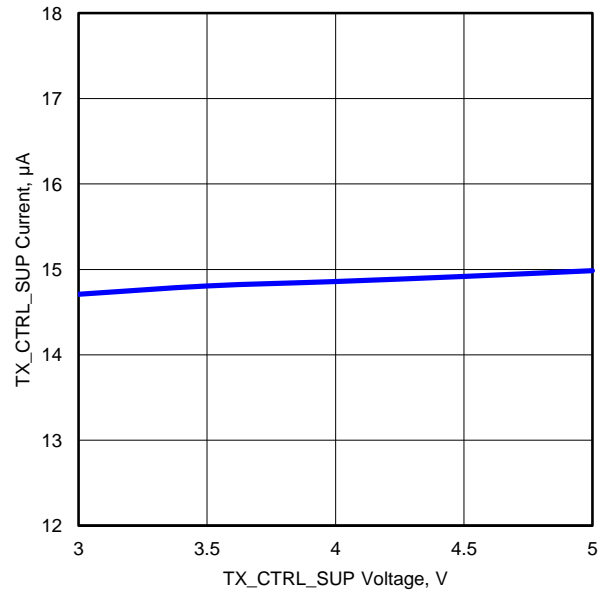
NAME	NO.	FUNCTION	DESCRIPTION
$\overline{\text{RESET}}$	29	Digital	AFE-only reset input, active low. Can be connected to the port pin of an external microcontroller
RX_ANA_GND	3, 36, 40	Supply	Rx analog ground pin. Connect to common board ground.
RX_ANA_SUP	33, 39	Supply	Rx analog supply pin (2.2 V to 3.6 V); 0.1- $\mu$ F decoupling capacitor to ground
RX_DIG_GND	19, 32	Supply	Rx digital ground pin. Connect to common board ground.
RX_DIG_SUP	31	Supply	Rx digital supply pin (2.2 V to 3.6 V); 0.1- $\mu$ F decoupling capacitor to ground
SCLK	24	SPI	SPI clock pin
SPISIMO	26	SPI	SPI serial in master out
SPISOMI	25	SPI	SPI serial out master in
SPISTE	27	SPI	SPI serial interface enable
TX_CTRL_SUP	11	Supply	Transmit control supply pin, 3.3 V (0.1- $\mu$ F decoupling capacitor to ground)
TX_REF	9	Reference	Tx reference voltage
TXN	14	Analog	LED driver out B, H-bridge output. Connect to LED.
TXP	15	Analog	LED driver out B, H-bridge output. Connect to LED.
VCM	4	Reference	Input common-mode voltage output. Connect a series resistor (1 k $\Omega$ ) and a decoupling capacitor (10 nF) to ground. The voltage across the capacitor can be used to shield (guard) the INP, INM traces.
VSS	8	Supply	Substrate ground. Connect to common board ground.
XOUT	37	Digital	Crystal oscillator pins. Connect an external 8-MHz crystal between these pins with the correct load capacitor (as specified by vendor) to ground. Connect to crystal and connect a TBD-pF capacitor from each pin to ground.
XIN	38	Digital	Crystal oscillator pins. Connect an external 8-MHz crystal between these pins with the correct load capacitor (as specified by vendor) to ground. Connect to crystal and connect a TBD-pF capacitor from each pin to ground.

**TYPICAL CHARACTERISTICS**

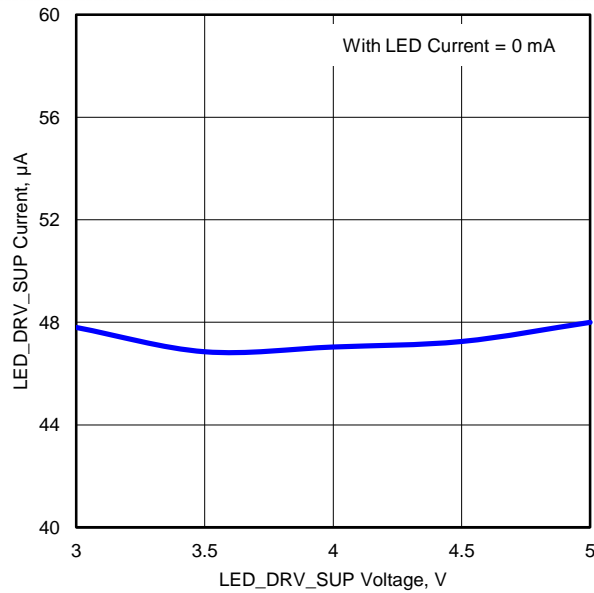
At  $T_A = +25^\circ\text{C}$ ,  $RX\_ANA\_SUP = RX\_DIG\_SUP = 3.0\text{ V}$ ,  $TX\_CTRL\_SUP = LED\_DRV\_SUP = 3.3\text{ V}$ , and  $f_{CLK} = 8\text{ MHz}$ , unless otherwise noted.



**Figure 3. TOTAL Rx CURRENT vs VOLTAGE**



**Figure 4. TX\_CTRL\_SUP CURRENT vs VOLTAGE**

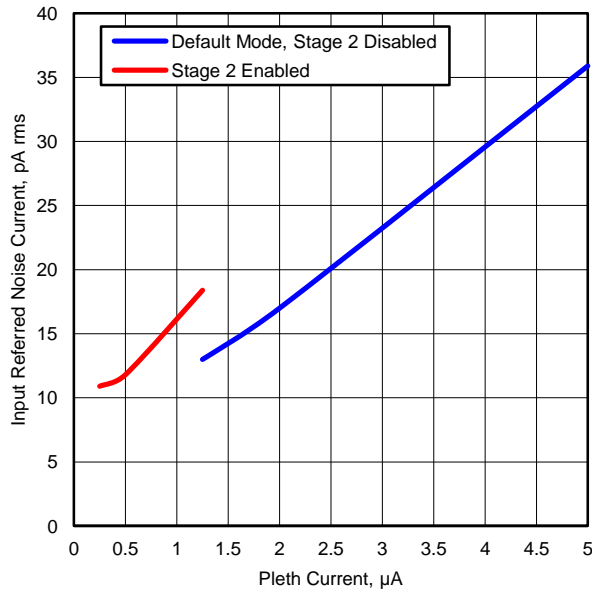


**Figure 5. LED\_DRV\_SUP CURRENT vs VOLTAGE**

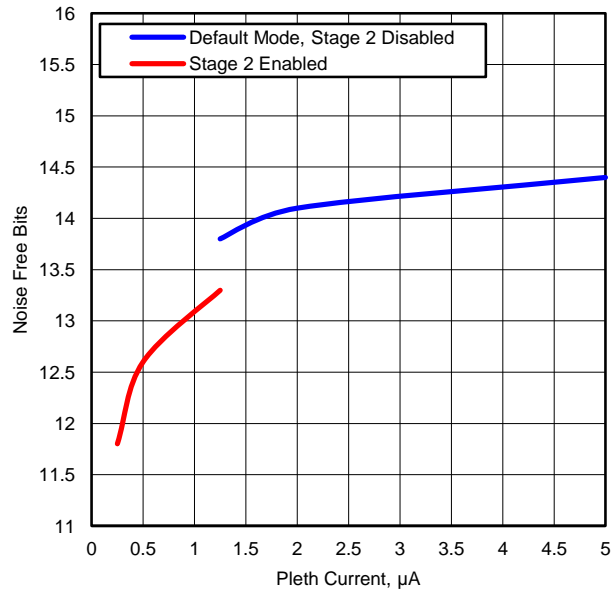
**PRODUCT PREVIEW**

**TYPICAL CHARACTERISTICS (continued)**

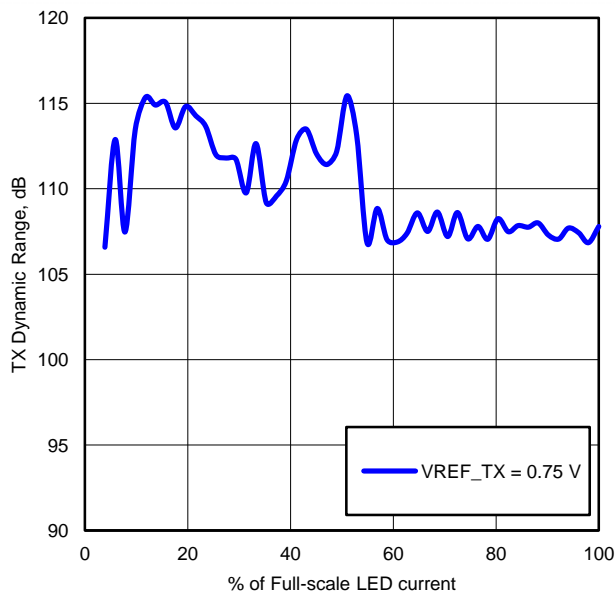
At  $T_A = +25^\circ\text{C}$ ,  $RX\_ANA\_SUP = RX\_DIG\_SUP = 3.0\text{ V}$ ,  $TX\_CTRL\_SUP = LED\_DRV\_SUP = 3.3\text{ V}$ , and  $f_{CLK} = 8\text{ MHz}$ , unless otherwise noted.



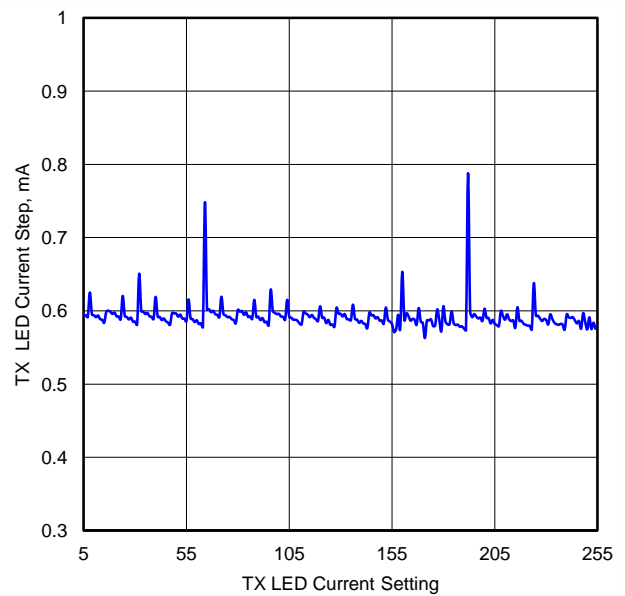
**Figure 6. INPUT-REFERRED NOISE CURRENT vs PLETH CURRENT <sup>(1)</sup>**



**Figure 7. NOISE-FREE BITS vs PLETH CURRENT <sup>(2)</sup>**



**Figure 8. Tx DYNAMIC RANGE**



**Figure 9. Tx LED CURRENT STEP vs Tx LED SETTING**

(1) Data at PRF = 625 Hz, 5% duty cycle.  
 (2) Data at PRF = 625 Hz, 5% duty cycle.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $RX\_ANA\_SUP = RX\_DIG\_SUP = 3.0\text{ V}$ ,  $TX\_CTRL\_SUP = LED\_DRV\_SUP = 3.3\text{ V}$ , and  $f_{CLK} = 8\text{ MHz}$ , unless otherwise noted.



Figure 10. RX\_DIG\_SUP NOISE MEASUREMENTS

## OVERVIEW

The AFE4400 is a complete analog front-end (AFE) solution targeted for pulse oximeter applications. The device consists of a low-noise receiver channel, an LED transmit section, and diagnostics for sensor and LED fault detection. To ease clocking requirements and provide the low-jitter clock to the AFE, an oscillator is also integrated that functions from an external crystal. The device communicates to an external microcontroller or host processor using an SPI interface. Figure 11 shows a detailed block diagram for the AFE4400. The blocks are described in more detail in the following sections.

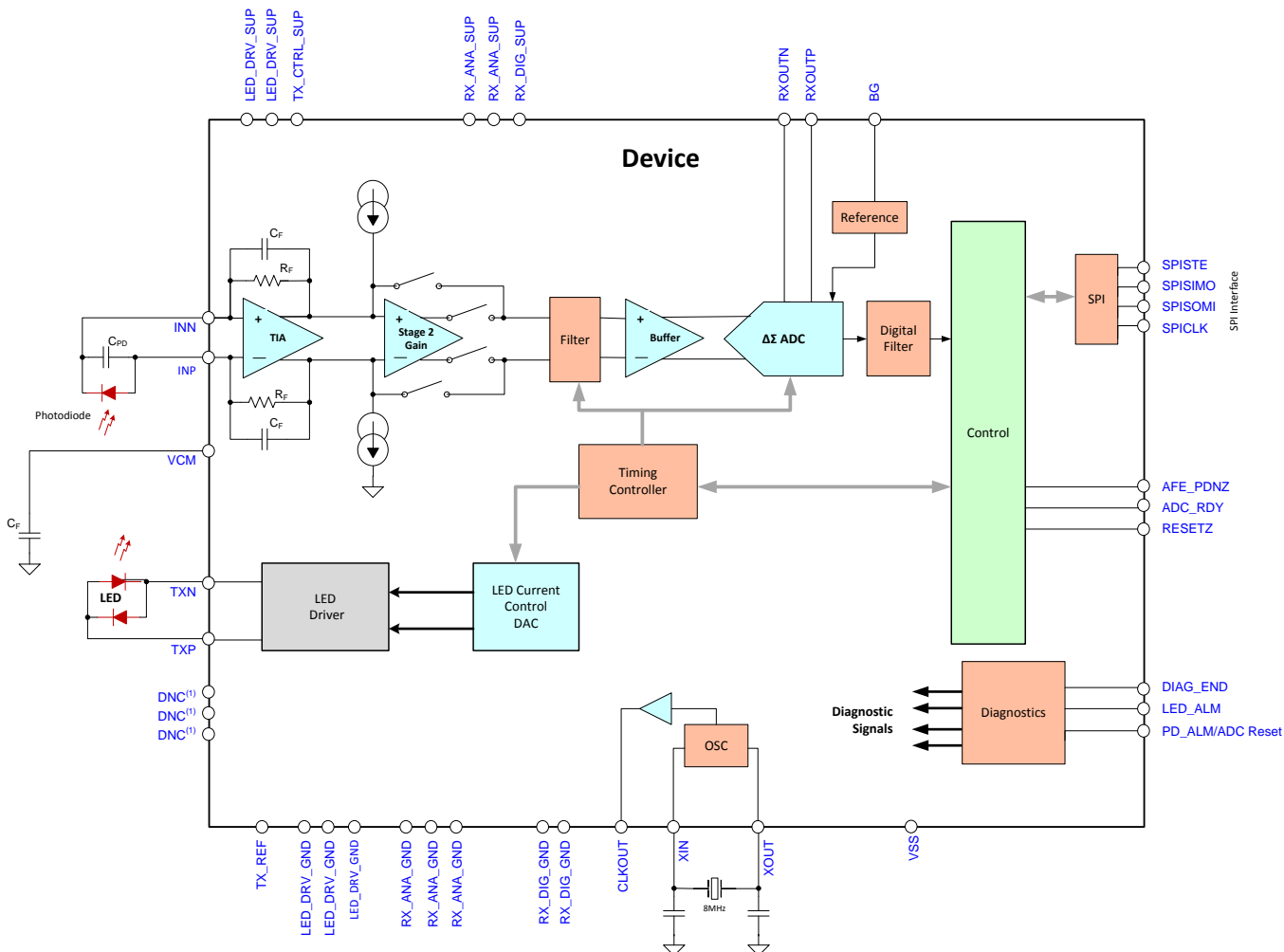


Figure 11. Detailed Block Diagram

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## RECEIVER CHANNEL

This section describes the functionality of the receiver channel.

### Receiver Front-End

The receiver consists of a differential current-to-voltage (I-V) transimpedance amplifier that converts the input photodiode current into an appropriate voltage, as shown in Figure 12. The feedback resistor of the amplifier ( $R_F$ ) is programmable to support a wide range of photodiode currents. Available  $R_F$  values include: 1 M $\Omega$ , 500 k $\Omega$ , 250 k $\Omega$ , 100 k $\Omega$ , 50 k $\Omega$ , 25 k $\Omega$ , and 10 k $\Omega$ .

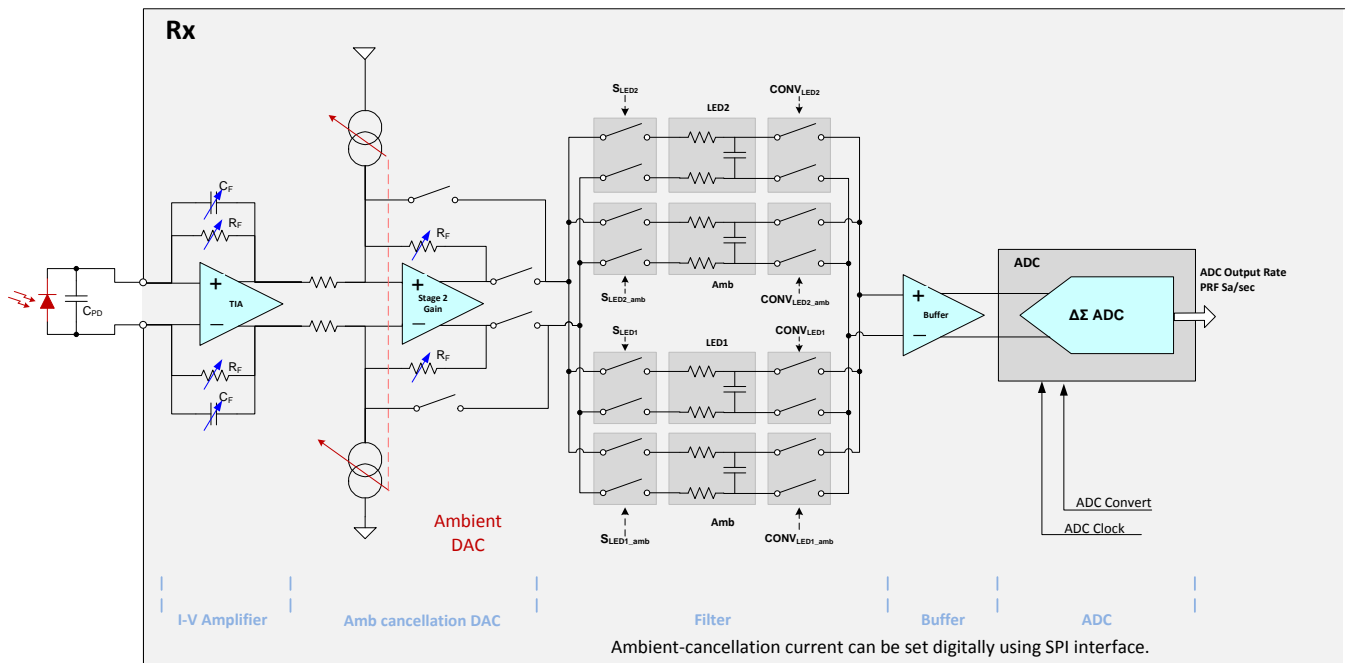


Figure 12. Receiver Front-End

The  $R_F$  amplifier and the feedback capacitor ( $C_F$ ) form a low-pass filter for the input signal current. Always ensure that the low-pass filter has sufficiently high bandwidth (as shown by Equation 1) because the input current consists of pulses. For this reason, the feedback capacitor is also programmable. Available  $C_F$  values include: 5 pF, 10 pF, 25 pF, 50 pF, 100 pF, and 250 pF. Any combination of these capacitors can also be used.

$$R_F \times C_F \leq \frac{\text{Rx Sample Time}}{10} \quad (1)$$

The output voltage of the I-V amplifier includes the pleth component (the desired signal) and a component resulting from the ambient light leakage; see . The I-V amplifier is followed by the second stage, which consists of a current digital-to-analog converter (DAC) that sources the cancellation current and an amplifier that gains up the pleth component alone. The amplifier has five programmable gain settings: 1, 1.5, 2, 3, and 4. The gained-up pleth signal is then low-pass filtered (500-Hz bandwidth) and buffered before driving a 22-bit ADC. The current DAC has a cancellation current range of 10  $\mu\text{A}$  with 10 steps (1  $\mu\text{A}$  each). The DAC value can be digitally specified with the SPI interface.

The output of the ambient cancellation amplifier is separated into LED2 and LED1 channels. When LED2 is on, the amplifier output is filtered and sampled on capacitor  $C_R$ . Similarly, the LED1 signal is sampled on the  $C_{LED1}$  capacitor when LED1 is ON. In between the LED2 and LED1 pulses, the idle amplifier output is sampled to estimate the ambient signal on capacitors  $C_{LED2\_amb}$  and  $C_{LED1\_amb}$ .

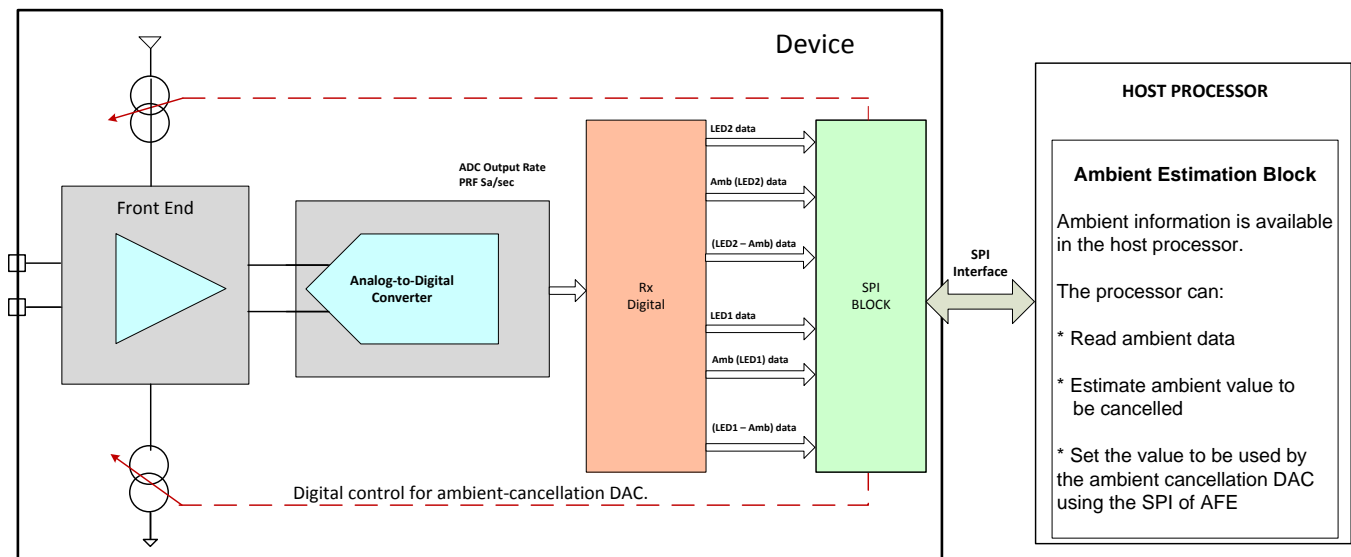
The sampling duration is termed the *Rx sample time* and is programmable for each signal, independently. The sampling can start after the I-V amplifier output is stable (to account for LED and cable settling times). The Rx sample time is used for all dynamic range calculations; the minimum time supported is 50  $\mu\text{s}$ .

A single, 22-bit ADC converts the sampled LED2, LED1, and ambient signals sequentially. Each conversion takes 25% of the pulse repetition period and provides a single digital code at the ADC output. As discussed in the [Receiver Timing](#) section, the conversions are staggered so that the LED2 conversion starts after the end of the LED2 sample phase, and so on. This configuration also means that the Rx sample time for each signal is no greater than 25% of the pulse repetition period.

Note that four data streams are available at the ADC output (LED2, LED1, ambient LED2, and ambient LED1) at the same rate as the pulse repetition frequency. The ADC is followed by a digital ambient subtraction block that additionally outputs the (LED2 – ambient LED2) and (LED1 – ambient LED1) data values.

### Ambient Cancellation Scheme

The receiver provides digital samples corresponding to ambient duration. The host processor (external to the AFE) can use these ambient values to estimate the amount of ambient light leakage. The processor must then set the value of the ambient cancellation DAC using the SPI, as shown in [Figure 13](#).



**Figure 13. Ambient Cancellation Loop (Closed by the Host Processor)**

Using the set value, the ambient cancellation stage subtracts the ambient component and gains up only the pleth component of the received signal; see [Figure 14](#). The amplifier gain is programmable to 1, 1.5, 2, 3, and 4.



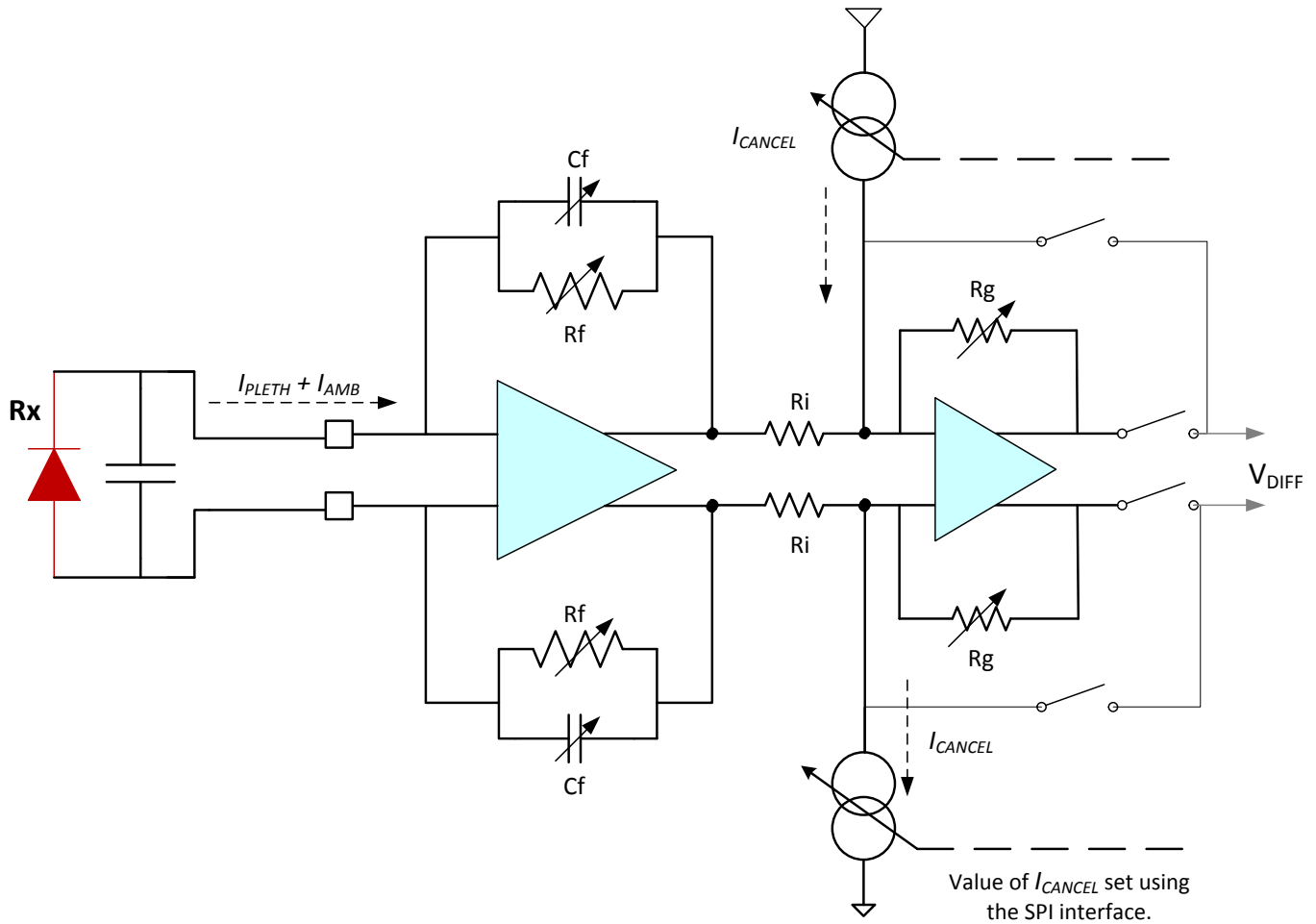


Figure 14. Front-End (I-V Amplifier and Cancellation Stage)

The differential output of the second stage is  $V_{DIFF}$ , as given by Equation 2:

$$V_{DIFF} = 2 \times \left[ I_{PLETH} \times \frac{R_F}{R_I} + I_{AMB} \times \frac{R_F}{R_I} - I_{CANCEL} \right] \times R_G$$

where:

$$R_I = 100 \text{ k}\Omega,$$

$I_{PLETH}$  = photodiode current pleth component,

$I_{AMB}$  = photodiode current ambient component, and

$I_{CANCEL}$  = the cancellation current DAC value (as estimated by the host processor).

(2)

## Receiver Control Signals

**LED2 sample phase ( $S_{LED2}$ ):** When this signal is high, the amplifier output corresponds to the LED2 on-time. The amplifier output is filtered and sampled into capacitor  $C_{LED2}$ . To avoid settling effects resulting from the LED or cable, program  $S_{LED2}$  to start after the LED turns on. This settling delay is programmable.

**Ambient sample phase ( $S_{LED2\_amb}$ ):** When this signal is high, the amplifier output corresponds to the LED2 off-time and can be used to estimate the ambient signal (for the LED2 phase). The amplifier output is filtered and sampled into capacitor  $C_{LED2\_amb}$ .

**LED1 sample phase ( $S_{LED1}$ ):** When this signal is high, the amplifier output corresponds to the LED1 on-time. The amplifier output is filtered and sampled into capacitor  $C_{LED1}$ . To avoid settling effects resulting from the LED or cable, program  $S_{LED1}$  to start after the LED turns on. This settling delay is programmable.

**Ambient sample phase ( $S_{LED1\_amb}$ ):** When this signal is high, the amplifier output corresponds to the LED1 off-time and can be used to estimate the ambient signal (for the LED1 phase). The amplifier output is filtered and sampled into capacitor  $C_{LED1\_amb}$ .

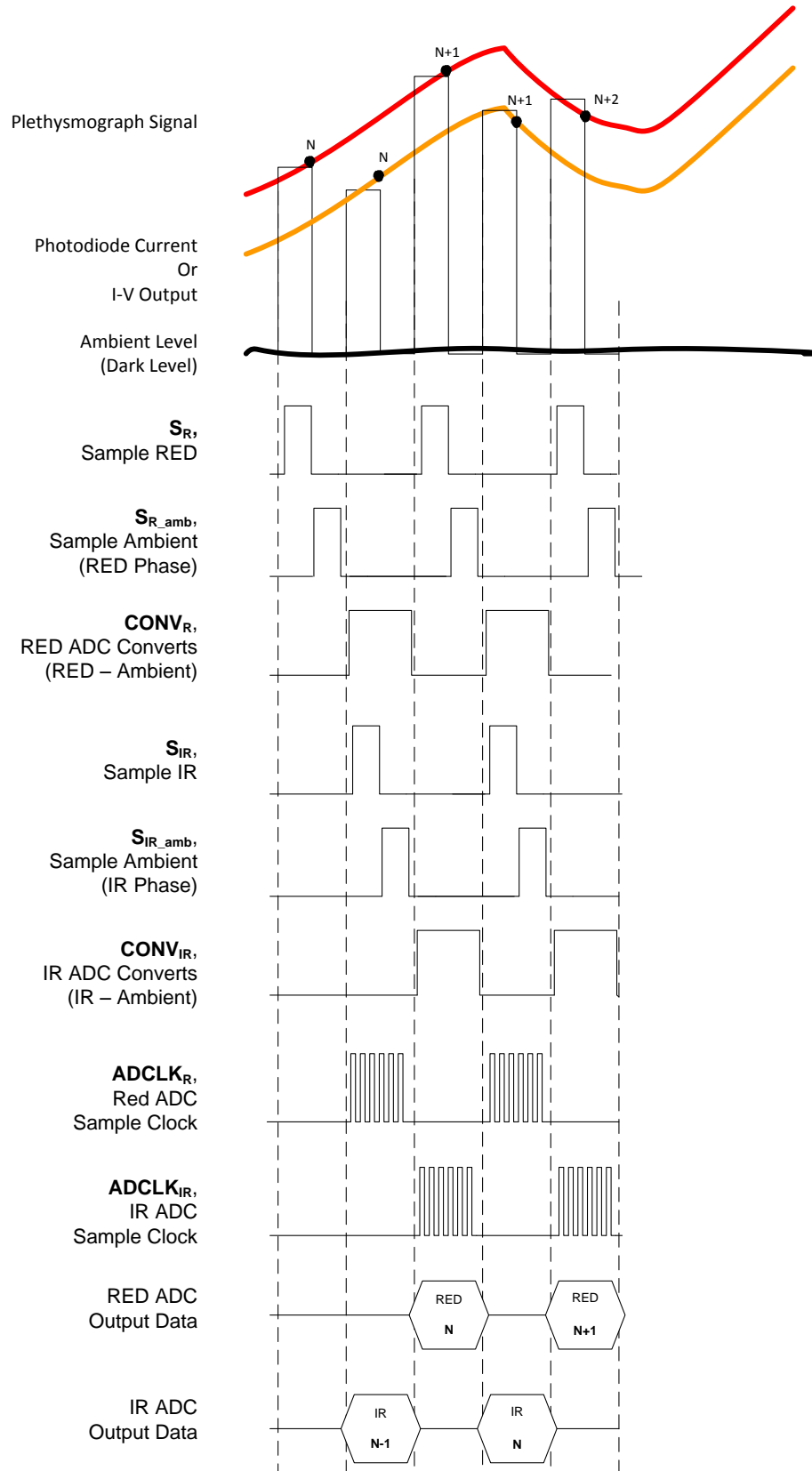
**LED2 convert phase ( $CONV_{LED2}$ ):** When this signal is high, the voltage sampled on  $C_{LED2}$  is buffered and applied to the ADC for conversion. The conversion time duration is always 25% of the pulse repetition period. At the end of the conversion, the ADC provides a single digital code corresponding to the LED2 sample.

**Ambient convert phases ( $CONV_{LED2\_amb}$ ,  $CONV_{LED1\_amb}$ ):** When this signal is high, the voltage sampled on  $C_{LED2\_amb}$  (or  $C_{LED1\_amb}$ ) is buffered and applied to the ADC for conversion. The conversion time duration is always 25% of the pulse repetition period. At the end of the conversion, the ADC provides a single digital code corresponding to the ambient sample.

**LED1 convert phase ( $CONV_{LED1}$ ):** When this signal is high, the voltage sampled on  $C_{LED1}$  is buffered and applied to the ADC for conversion. The conversion time duration is always 25% of the pulse repetition period. At the end of the conversion, the ADC provides a single digital code corresponding to the LED1 sample.

## Receiver Timing

See [Figure 15](#) for a timing diagram detailing the control signals related to the LED on-time, Rx sample time, and the ADC conversion times for each channel.



NOTE: Relationship to the AFE4400 EVM is: LED1 = IR and LED2 = RED.

Figure 15. Rx Timing Diagram

## CLOCKING AND TIMING SIGNAL GENERATION

The crystal oscillator generates a master clock signal using an external 8-MHz crystal. A divide-by-2 block converts the 8-MHz clock to 4 MHz, which is used by the AFE to operate the timer modules, ADC, and diagnostics. The 4-MHz clock is buffered and output from the AFE in order to clock an external microcontroller. The clocking functionality is shown in Figure 16.

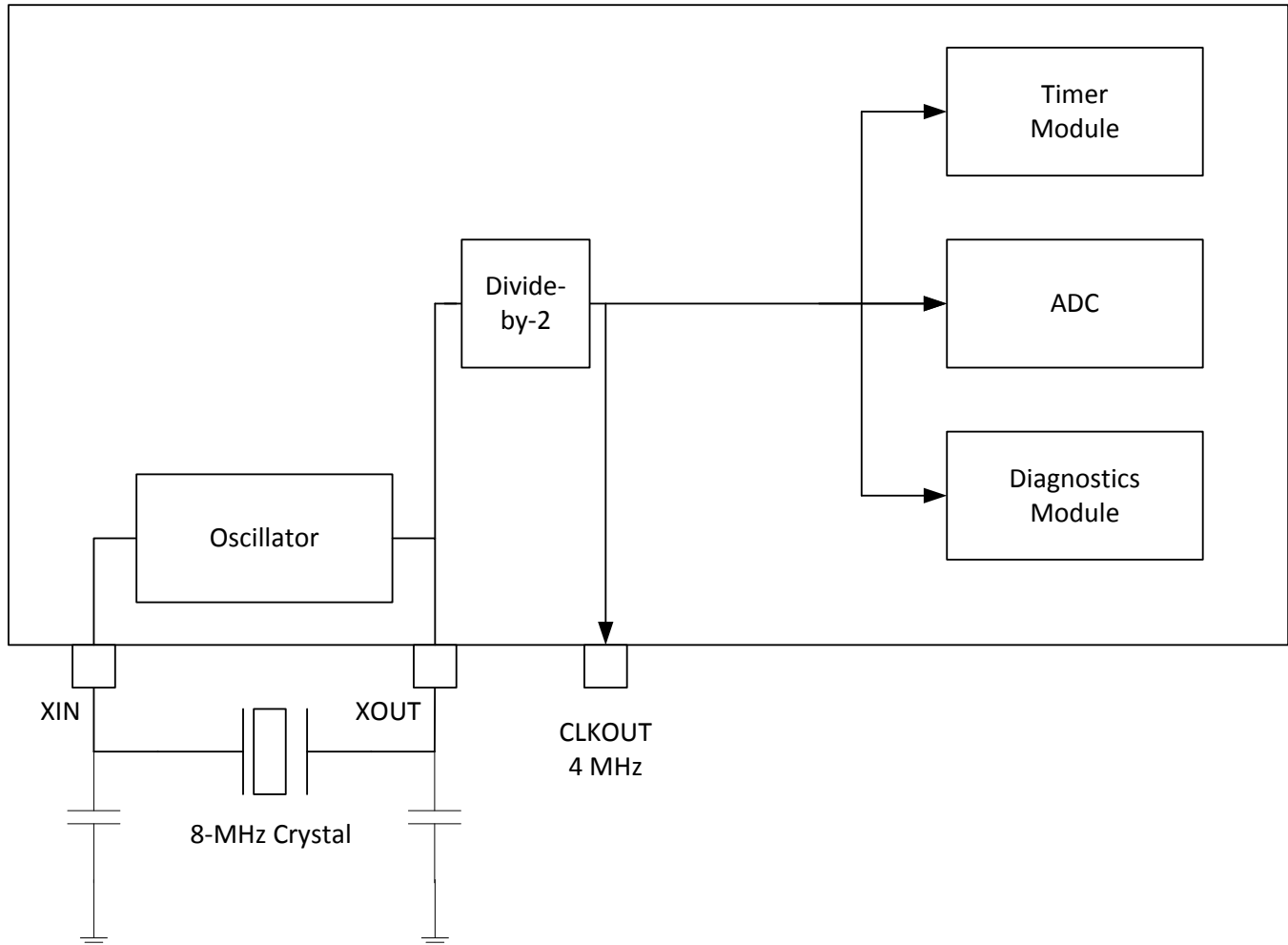
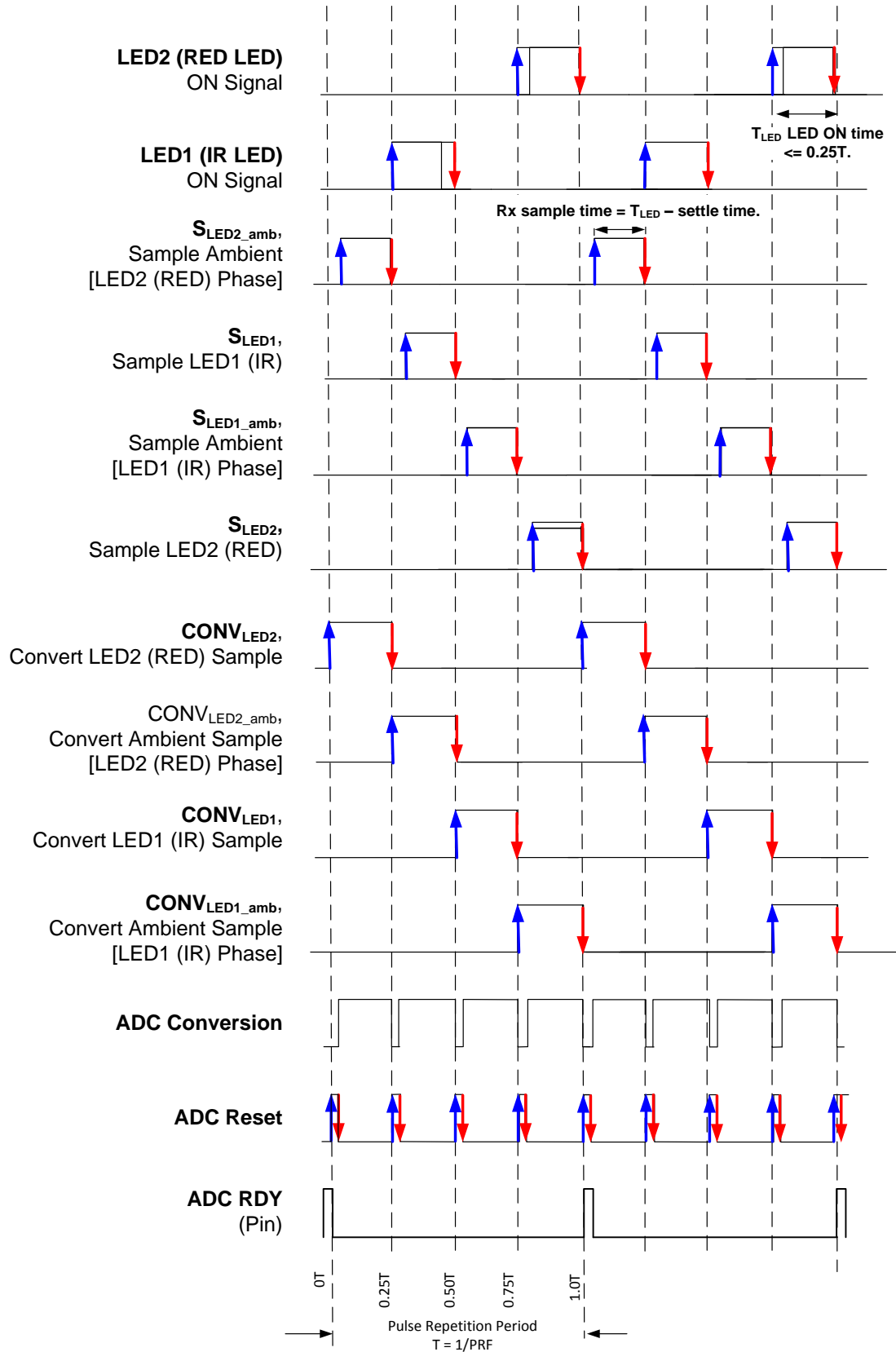


Figure 16. AFE Clocking

## TIMER MODULE

See Figure 17 for a timing diagram detailing the various timing edges that are programmable using the timer module. The rising and falling edge positions of 11 signals can be controlled. The module uses a single 16-bit counter (running off of the 4-MHz clock) to set the time-base.

All timing signals are set with reference to the pulse repetition period (PRP). Therefore, a dedicated compare register compares the 16-bit counter value with the reference value specified in the PRF register. Every time that the 16-bit counter value is equal to the reference value in the PRF register, the counter is reset to '0'.



NOTE: Programmable edges are shown in blue and red.

Figure 17. AFE Control Signals

For the 11 signals in Figure 15, the start and stop edge positions are programmable with respect to the PRF period. Each signal uses a separate timer compare module that compares the counter value with preprogrammed reference values for the start and stop edges. All reference values can be set using the SPI interface.

When the counter value equals the start reference value, the output signal is set. When the counter value equals the stop reference value, the output signal is reset. Figure 18 shows a diagram of the timer compare register. With a 4-MHz clock, the edge placement resolution is 0.25  $\mu$ s. The ADC conversion signal requires four pulses in each PRF clock period. The 11th timer compare register uses four sets of start and stop registers to control the ADC conversion signal.

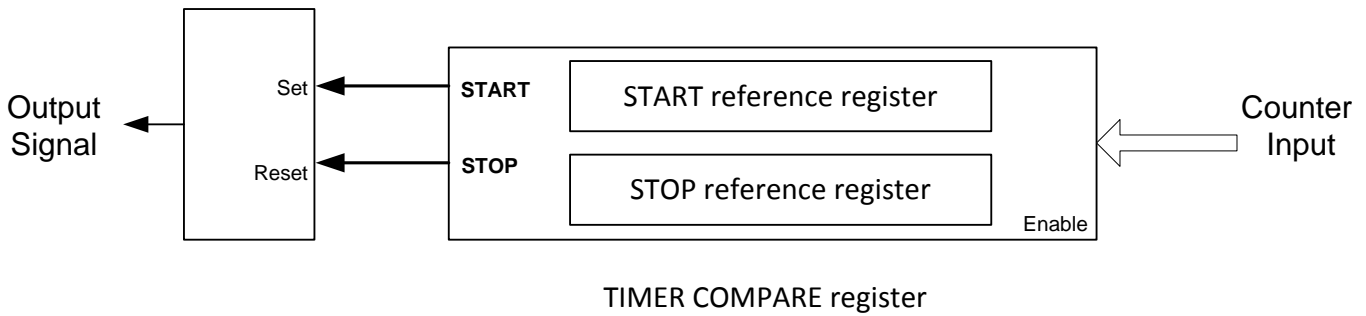


Figure 18. Compare Register

The ADC conversion signal requires four pulses in each PRF clock period. Timer compare register 11 uses four sets of start and stop registers to control the ADC conversion signal, as shown in Figure 19.

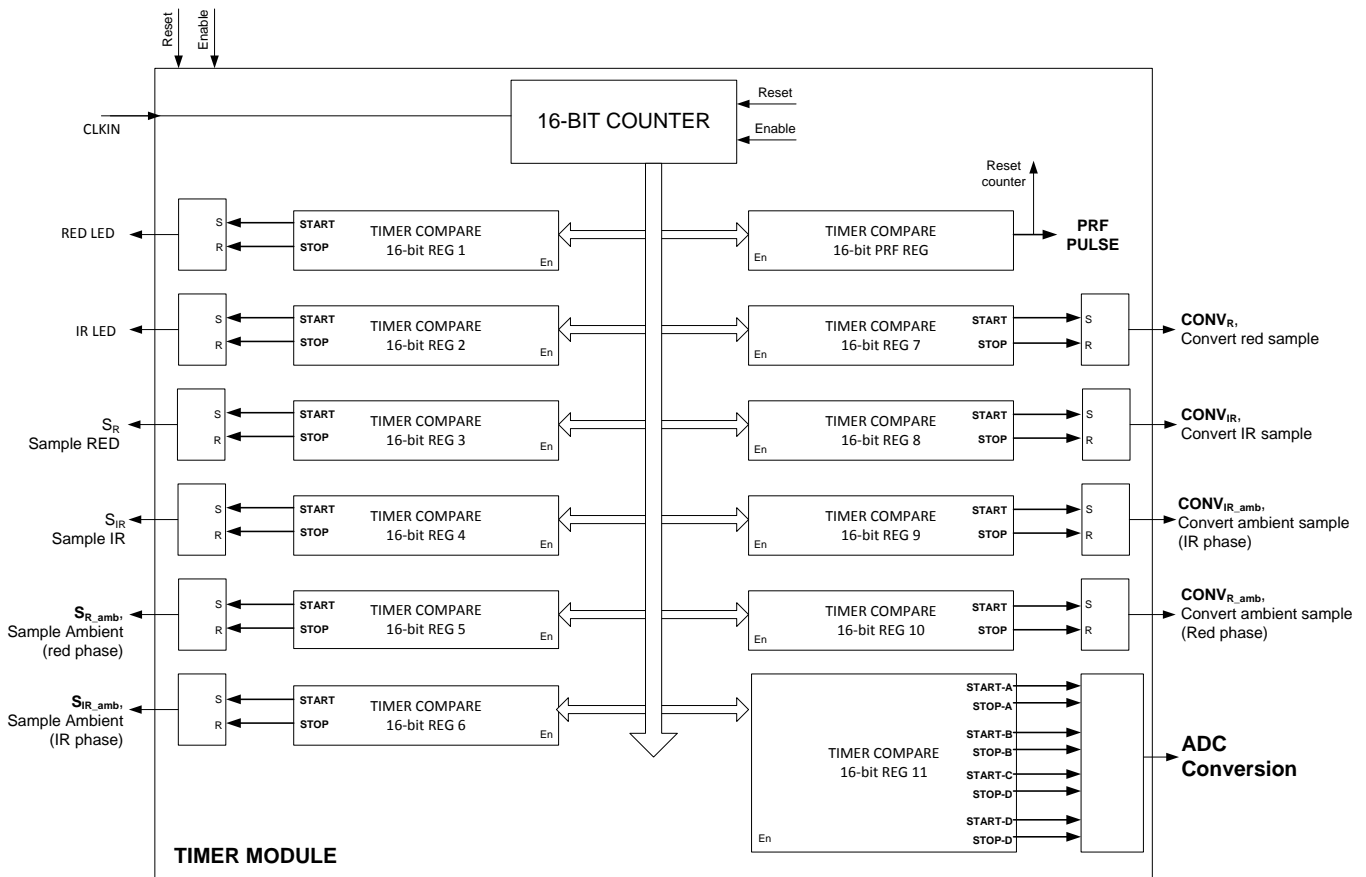


Figure 19. Timer Module

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## Using the Timer Module

The timer module registers can be used to program the start and end instants in units of 4-MHz clock cycles. These timing instants and the corresponding registers are listed in [Table 2](#).

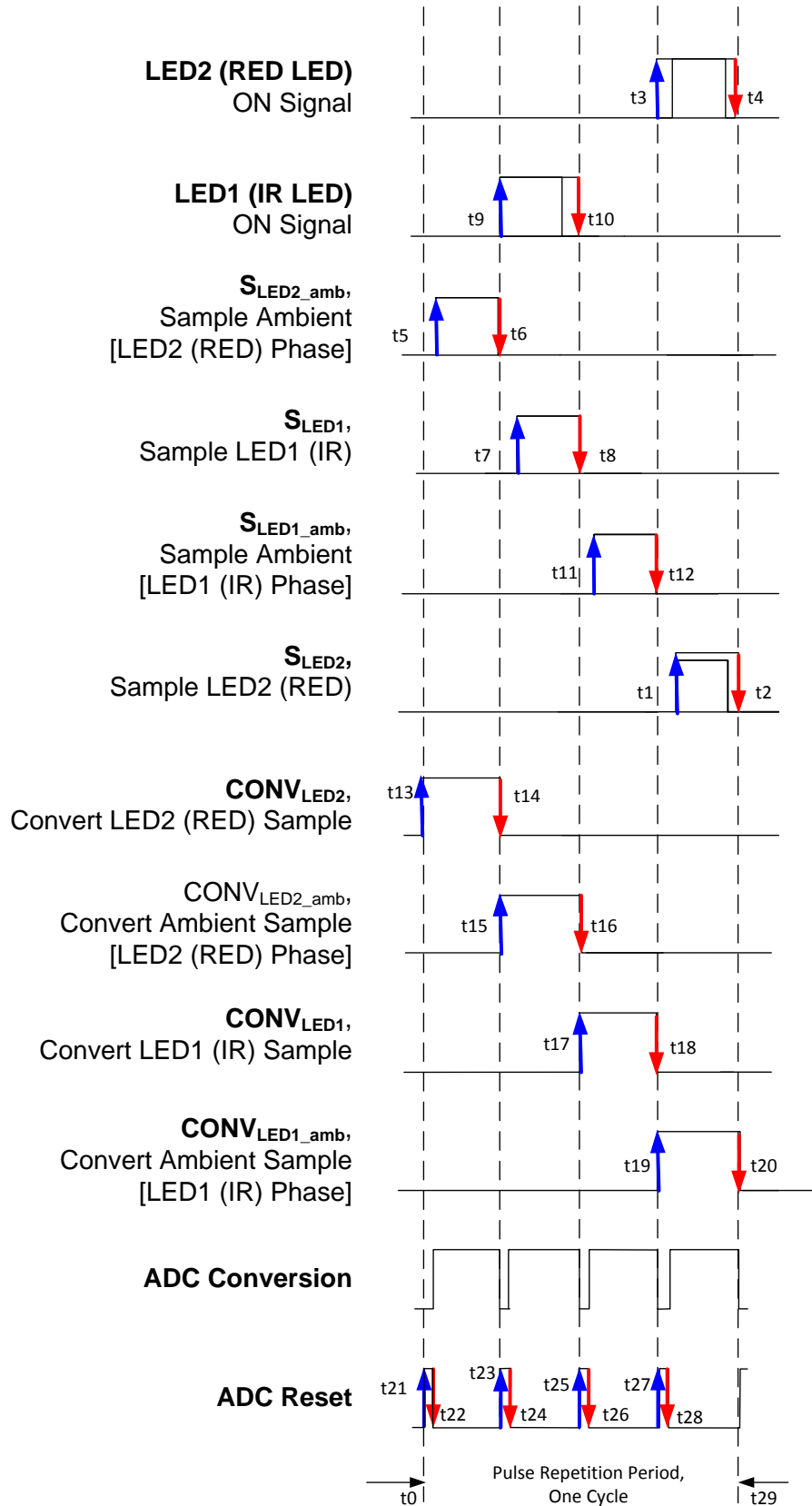
Note that the device does not restrict the values in these registers; thus, the start and end edges can be positioned anywhere within the pulse repetition period. Care must be taken by the user to program suitable values in these registers to avoid overlapping the signals and to make sure none of the edges exceed the value programmed in the PRP register. Writing the same value in the start and end registers results in a pulse duration of one clock cycle. The following steps describe the timer sequencing configuration:

1. With respect to the start of the PRP period (indicated by timing instant  $t_0$  in [Figure 20](#)), the following sequence of conversions must be followed in order: convert LED2 → LED2 ambient → LED1 → LED1 ambient.
2. Also, starting from  $t_0$ , the sequence of sampling instants must be staggered with respect to the respective conversions as follows: sample LED2 ambient → LED1 → LED1 ambient → LED2.
3. Finally, align the edges for the two LED pulses with the respective sampling instants.

**Table 2. Clock Edge Mapping to SPI Registers**

TIME INSTANT (See <a href="#">Figure 20</a> and <a href="#">Figure 21</a> )	DESCRIPTION	CORRESPONDING REGISTER ADDRESS AND REGISTER BITS	EXAMPLE (Decimal)
$t_0$	Start of pulse repetition period	No register control	—
$t_1$	Start of sample LED2 pulse	LED2STC[15:0], register 01h	4800
$t_2$	End of sample LED2 pulse	LED2ENDC[15:0], register 02h	6399
$t_3$	Start of LED2 pulse	LED2LEDSTC[15:0], register 03h	4800
$t_4$	End of LED2 pulse	LED2LEDENDC[15:0], register 04h	6399
$t_5$	Start of sample LED2 ambient pulse	ALED2STC[15:0], register 05h	0
$t_6$	End of sample LED2 ambient pulse	ALED2ENDC[15:0], register 06h	1599
$t_7$	Start of sample LED1 pulse	LED1STC[15:0], register 07h	1600
$t_8$	End of sample LED1 pulse	LED1ENDC[15:0], register 08h	3199
$t_9$	Start of LED1 pulse	LED1LEDSTC[15:0], register 09h	1600
$t_{10}$	End of LED1 pulse	LED1LEDENDC[15:0], register 0Ah	3199
$t_{11}$	Start of sample LED1 ambient pulse	ALED1STC[15:0], register 0Bh	3200
$t_{12}$	End of sample LED1 ambient pulse	ALED1ENDC[15:0], register 0Ch	4799
$t_{13}$	Start of convert LED2 pulse	LED2CONVST[15:0], register 0Dh	2
$t_{14}$	End of convert LED2 pulse	LED2CONVEND[15:0], register 0Eh Must start one AFE clock cycle after the ADC reset pulse ends.	1599
$t_{15}$	Start of convert LED2 ambient pulse	ALED2CONVST[15:0], register 0Fh Must start one AFE clock cycle after the ADC reset pulse ends.	1602
$t_{16}$	End of convert LED2 ambient pulse	ALED2CONVEND[15:0], register 10h	3199
$t_{17}$	Start of convert LED1 pulse	LED1CONVST[15:0], register 11h Must start one AFE clock cycle after the ADC reset pulse ends.	3202
$t_{18}$	End of convert LED1 pulse	LED1CONVEND[15:0], register 12h	4799
$t_{19}$	Start of convert LED1 ambient pulse	ALED1CONVST[15:0], register 13h Must start one AFE clock cycle after the ADC reset pulse ends.	4802
$t_{20}$	End of convert LED1 ambient pulse	ALED1CONVEND[15:0], register 14h	6399
$t_{21}$	Start of first ADC conversion reset pulse	ADCRSTCNT0[15:0], register 15h	0
$t_{22}$	End of first ADC conversion reset pulse	ADCRSTENDCT0[15:0], register 16h	0
$t_{23}$	Start of second ADC conversion reset pulse	ADCRSTSTCT1[15:0], register 17h	1600
$t_{24}$	End of second ADC conversion reset pulse	ADCRSTENDCT1[15:0], register 18h	1600
$t_{25}$	Start of third ADC conversion reset pulse	ADCRSTSTCT2[15:0], register 19h	3200
$t_{26}$	End of third ADC conversion reset pulse	ADCRSTENDCT2[15:0], register 1Ah	3200
$t_{27}$	Start of fourth ADC conversion reset pulse	ADCRSTSTCT3[15:0], register 1Bh	4800
$t_{28}$	End of fourth ADC conversion reset pulse	ADCRSTENDCT3[15:0], register 1Ch	4800
$t_{29}$	End of pulse repetition period	PRPCOUNT[15:0], register 1Dh	6399

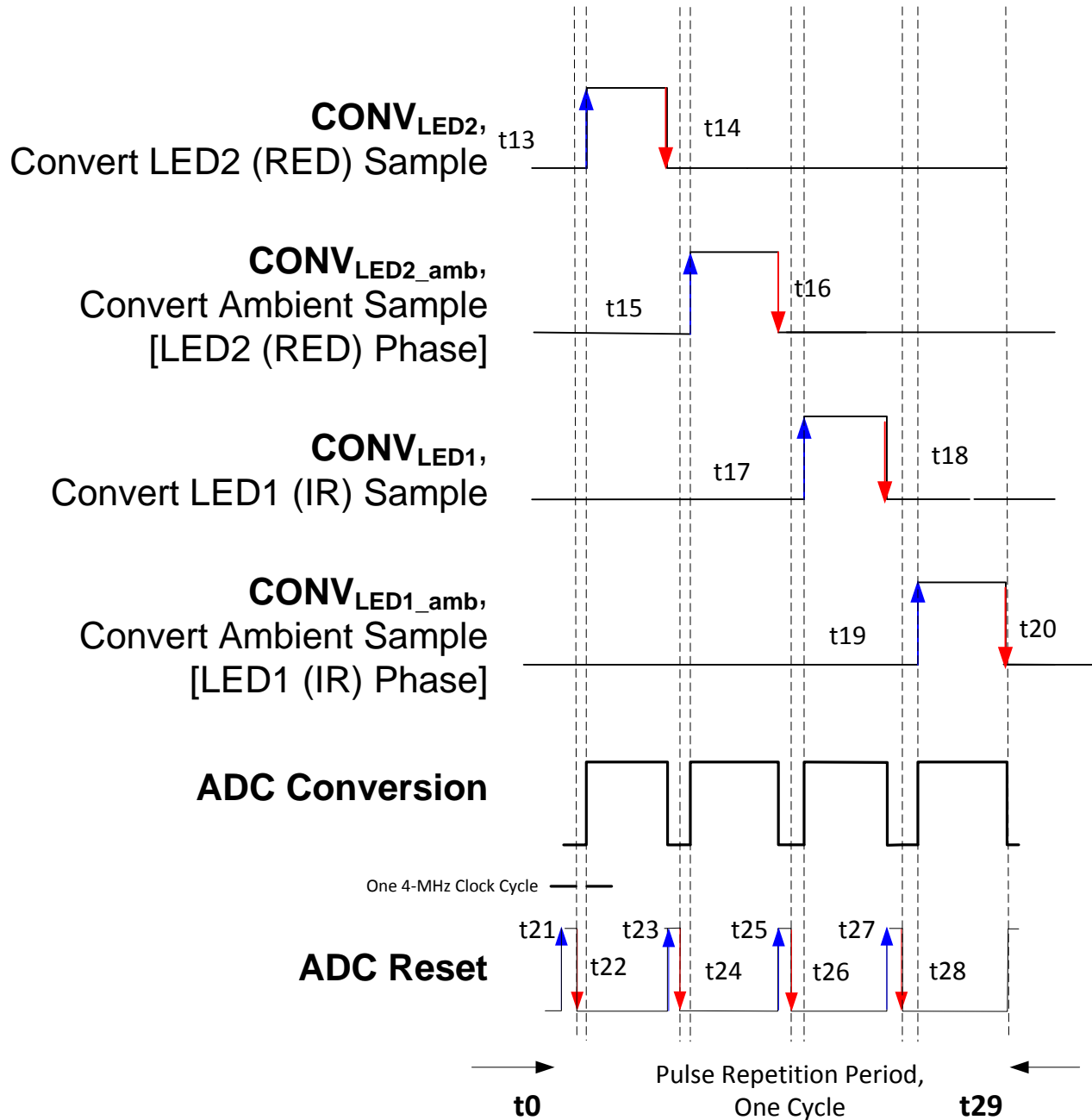
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(1) RED = LED2, IR = LED1.

Figure 20. Programmable Clock Edges





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(1) RED = LED2, IR = LED1.

**Figure 21. Relationship Between the ADC Reset and ADC Conversion Signals**

## ADC OPERATION AND AVERAGING MODULE

The ADC reset signal must be positioned at 25% intervals of the pulse repetition period (that is, 0%, 25%, 50%, and 75%). After the falling edge of the ADC reset signal, the ADC conversion phase starts. Each ADC conversion takes 50  $\mu$ s.

The ADC operates with averaging. The averaging module averages multiple ADC samples and reduce noise to improve dynamic range because the ADC conversion time is usually shorter than 25% of the pulse repetition period. Figure 22 shows a diagram of the averaging module.

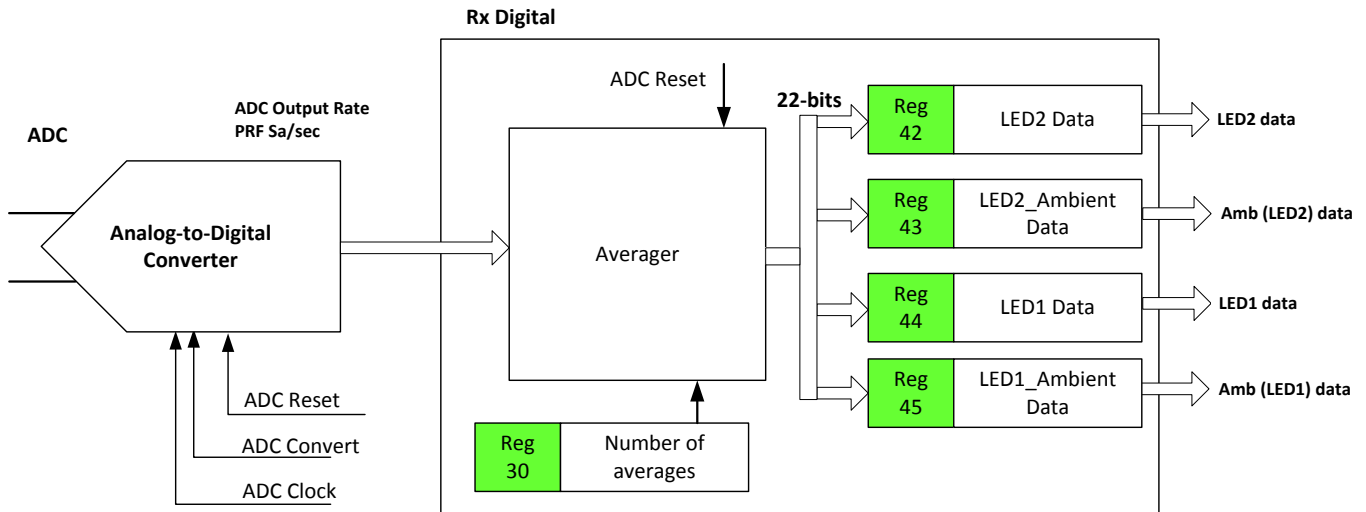


Figure 22. Averaging Module

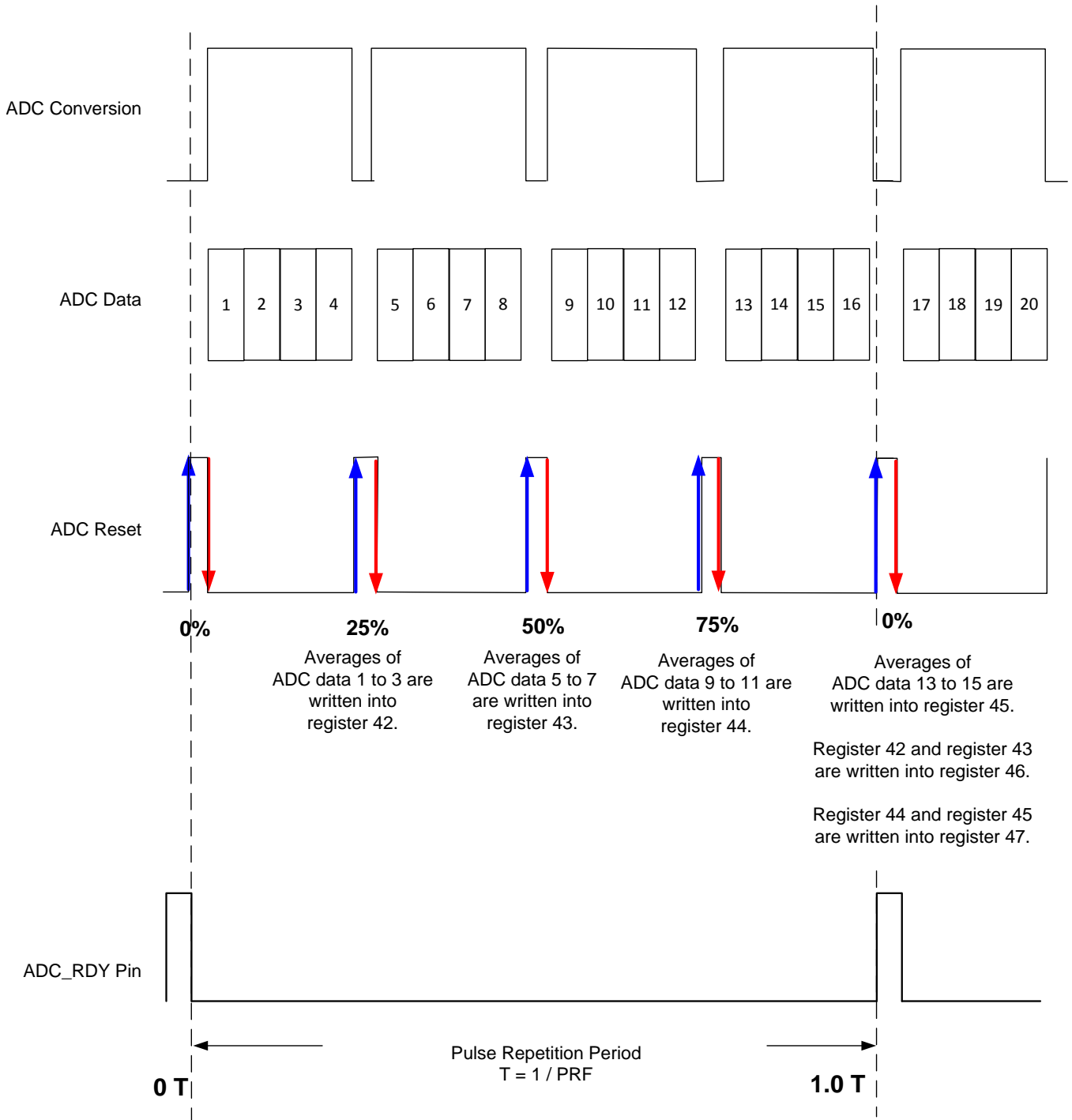
### Operation With Averaging

In this mode, the ADC digital samples are accumulated and averaged after every 50  $\mu$ s. At the next rising edge of the ADC reset signal, the average value (22-bit) is written into the output registers sequentially as follows (see Figure 23):

- At the 25% reset signal, the averaged 22-bit word is written to register 2Ah.
- At the 50% reset signal, the averaged 22-bit word is written to register 2Bh.
- At the 75% reset signal, the averaged 22-bit word is written to register 2Ch.
- At the next 0% reset signal, the averaged 22-bit word is written to register 2Dh. The contents of registers 2Ah and 2Bh are written to register 2Eh and the contents of registers 2Ch and 2Dh are written to register 2Fh.

At the rising edge of the ADC\_RDY signal, the contents of all six result registers can be read out.

The number of samples to be used per conversion phase is preset to 3.



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NOTE: This example shows data 3 averages.

Figure 23. ADC Data with Averaging

### RECEIVER SUBSYSTEM POWER PATH

The block diagram in [Figure 24](#) shows the AFE4400 Rx subsystem power routing.

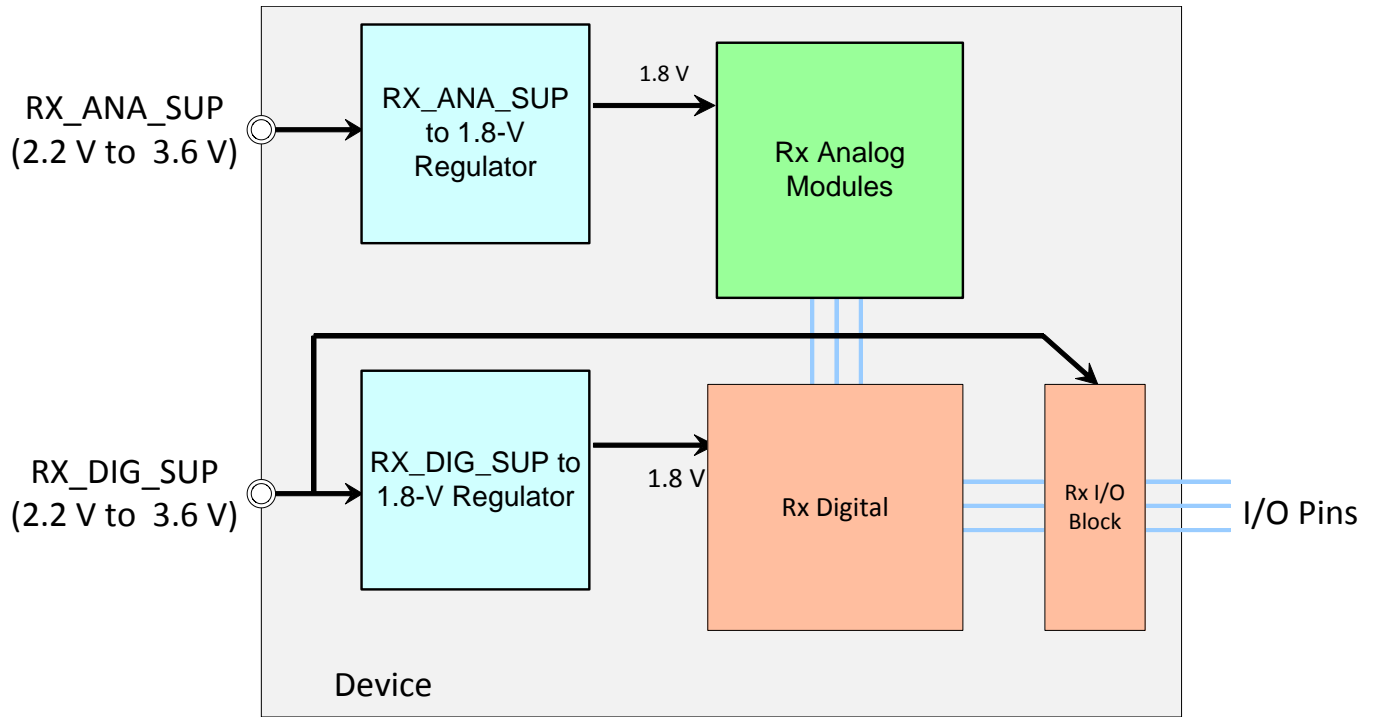


Figure 24. Receive Subsystem Power Routing

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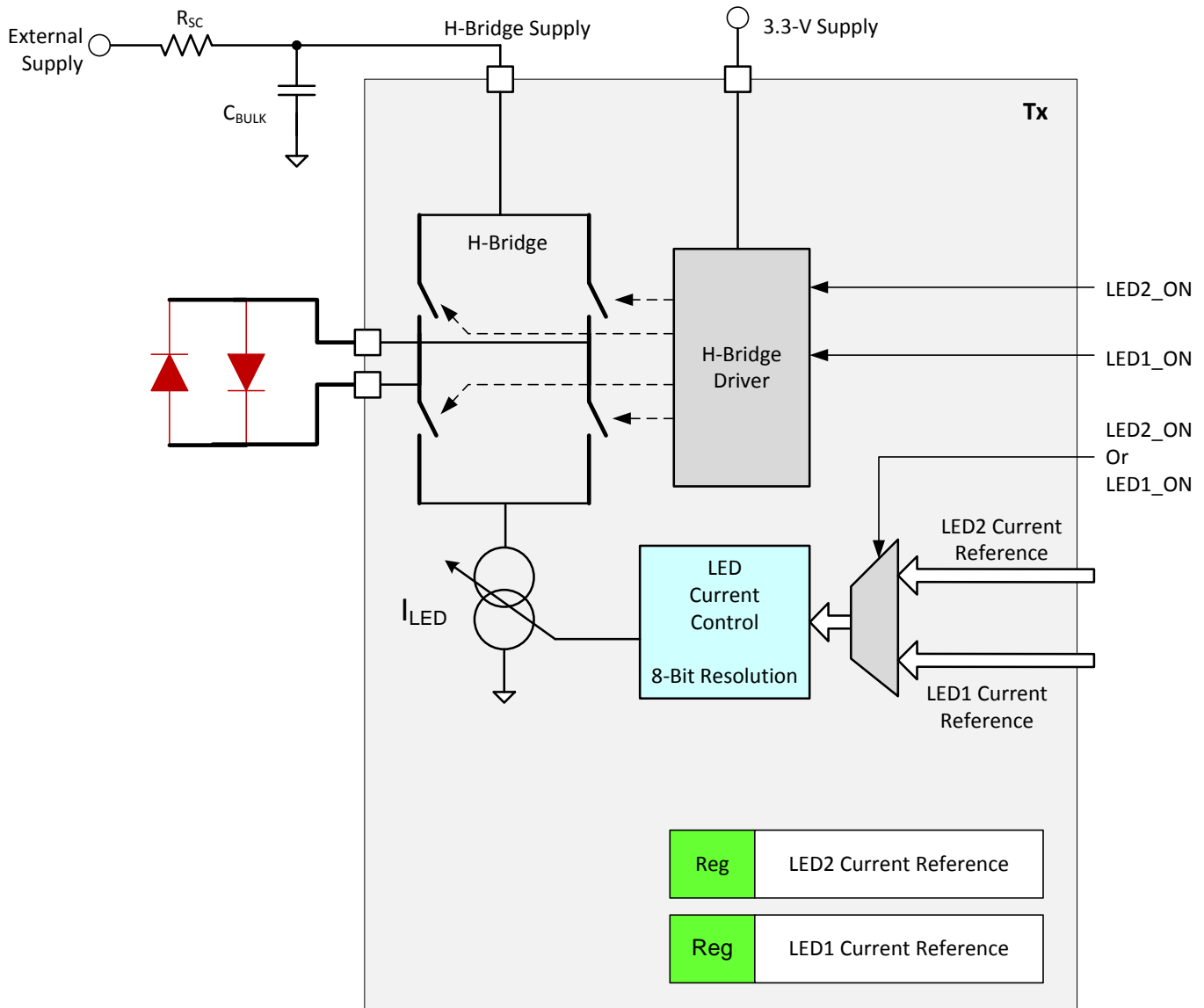
### TRANSMIT SECTION

The transmit section integrates the LED driver and the LED current control section with 8-bit resolution. This integration is designed to meet a dynamic range of better than 105 dB (based on a 1-sigma LED current noise).

The LED2 and LED1 reference currents can be independently set. The current source ( $I_{LED}$ ) locally regulates and ensures that the actual LED current tracks the specified reference.

Two LED driver schemes are supported:

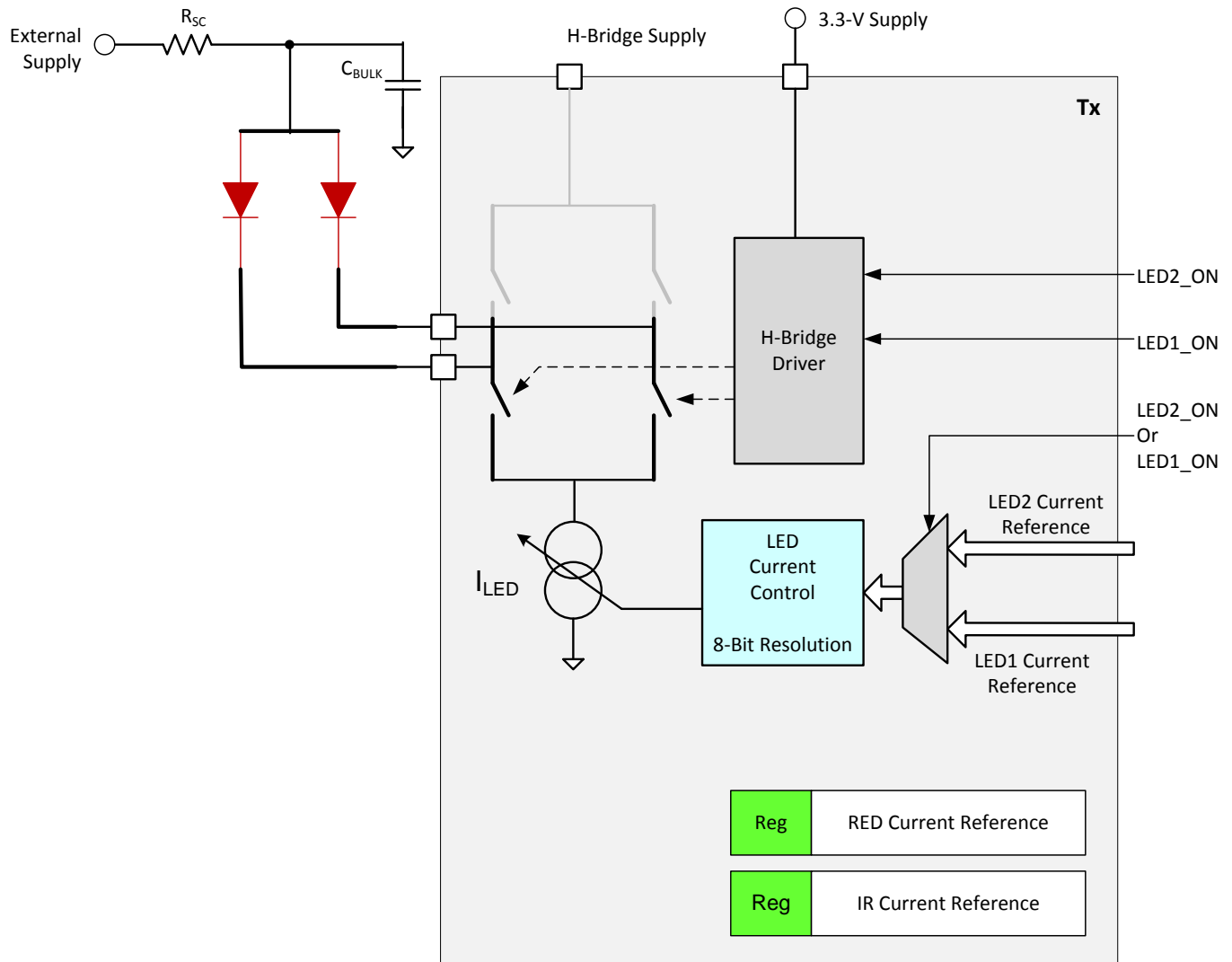
- An H-bridge drive for a two-terminal back-to-back LED package, as shown in Figure 25. The minimum H-bridge supply voltage must be 2.5 V + (maximum voltage drop across the LED).
- A push-pull drive for a three-terminal LED package; see Figure 26. The minimum external supply voltage = 2.0 V + (maximum voltage drop across the LED) + (voltage drop across  $R_{SC}$ .)



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NOTE: The  $R_{SC}$  resistance value must be selected by the user to consider the LED maximum allowable current and LED temperature limit.

Figure 25. Transmit: H-Bridge Drive



NOTE: The  $R_{SC}$  resistance value must be selected by the user to consider the LED maximum allowable current and LED temperature limit.

**Figure 26. Transmit: Push-Pull LED Drive for Common Anode LED Configuration**

**Transmitter Power Path**

The block diagram in Figure 27 shows the AFE4400 Tx subsystem power routing.

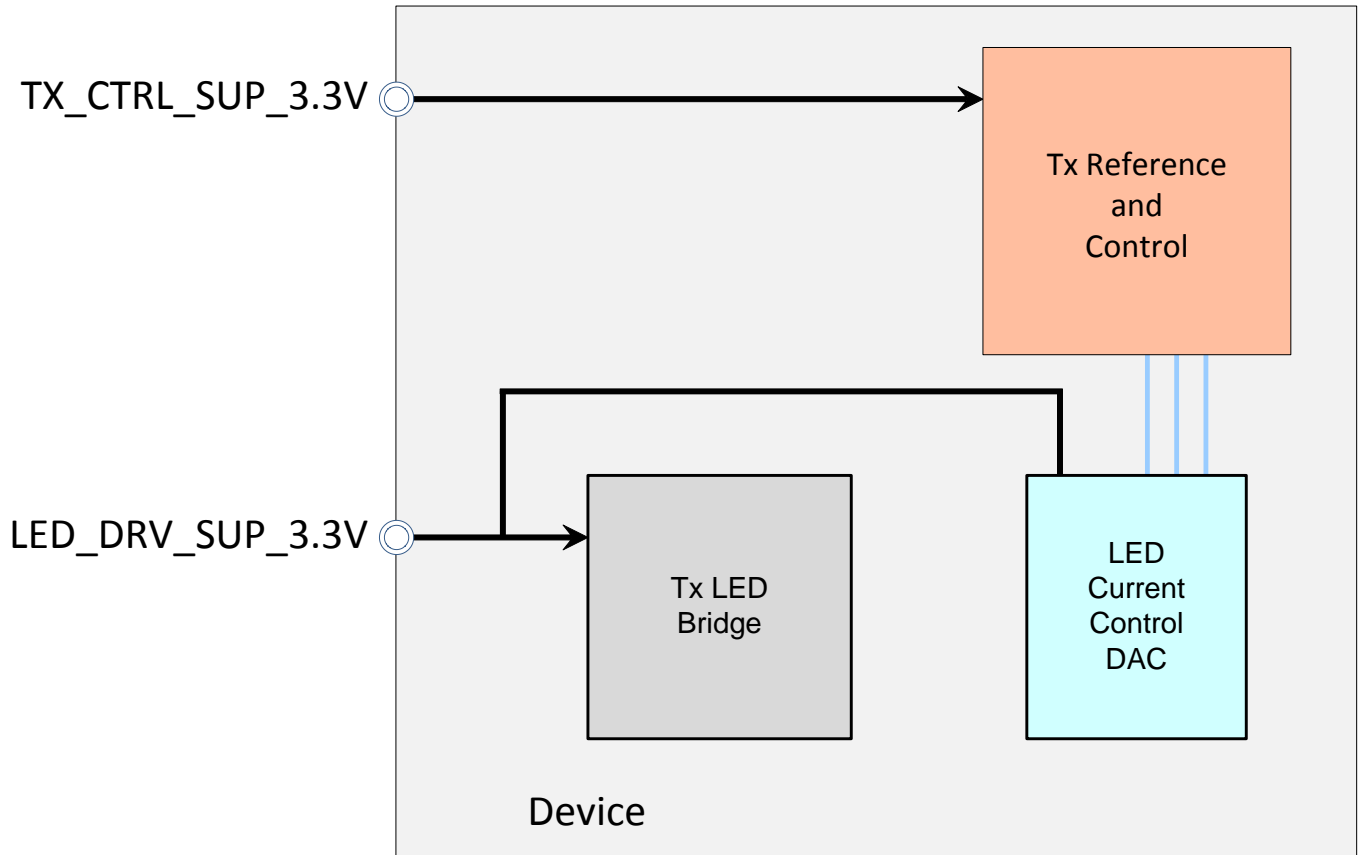


Figure 27. Transmit Subsystem Power Routing

**LED Power Reduction During Periods of Inactivity**

The diagram in Figure 28 shows how LED bias current passes 50  $\mu$ A whenever LED\_ON occurs. In order to minimize power consumption in periods of inactivity, the LED\_ON control must be turned off.

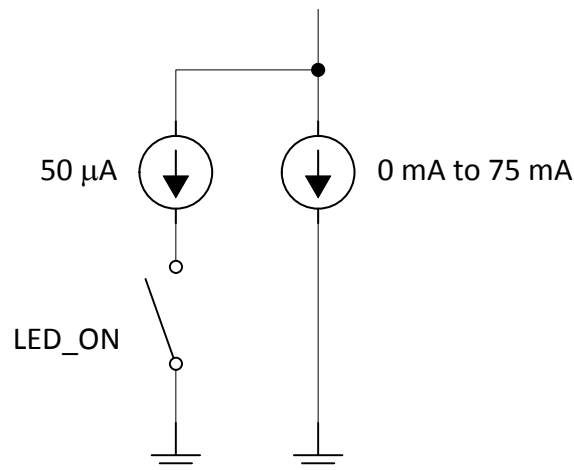


Figure 28. LED Bias Current

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## DIAGNOSTICS

The device includes diagnostics to detect open or short conditions of the LED and photosensor, LED current profile feedback, and cable on or off detection.

### Photodiode-Side Fault Detection

Figure 29 shows the diagnostic for the photodiode-side fault detection.

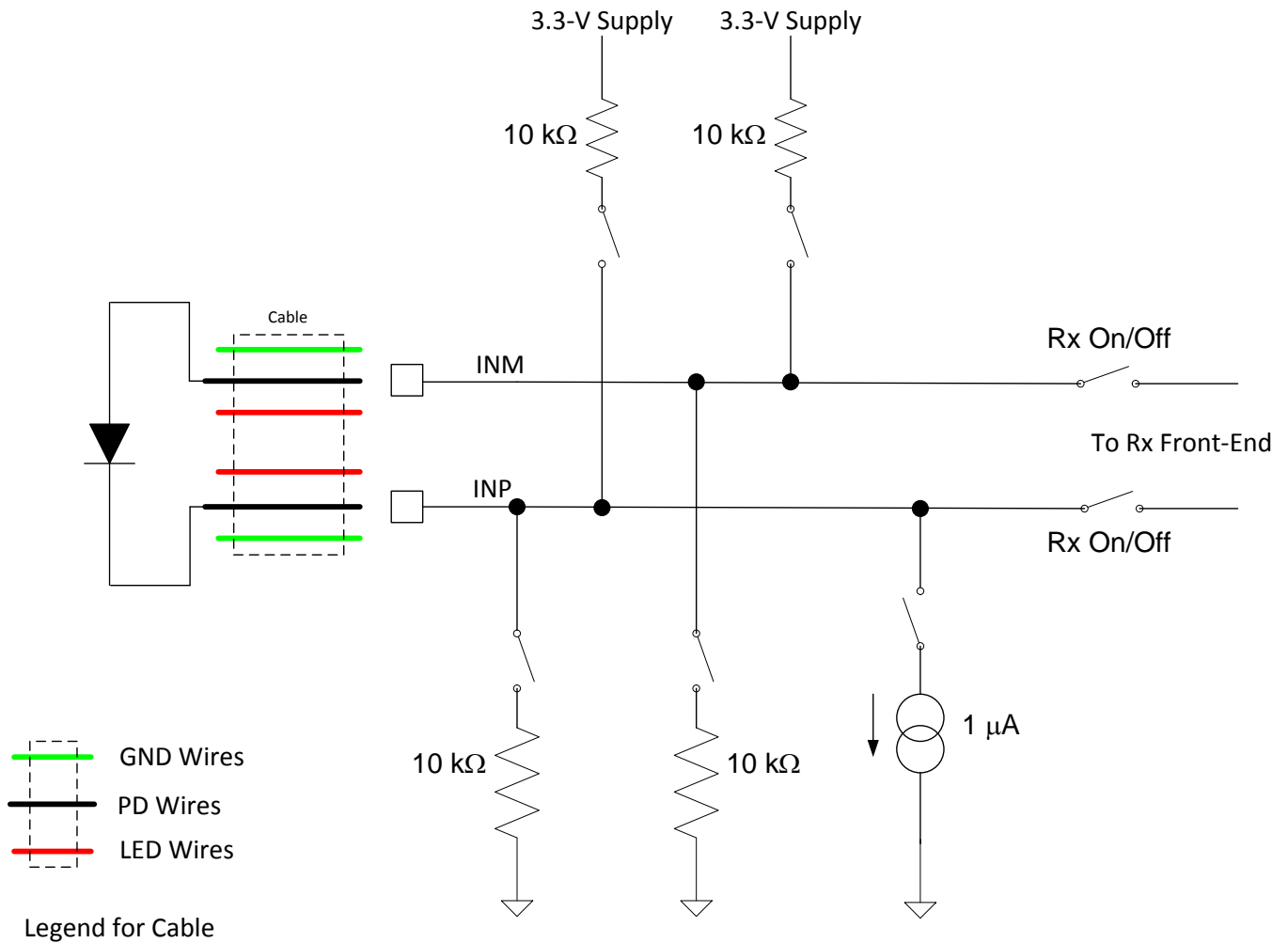


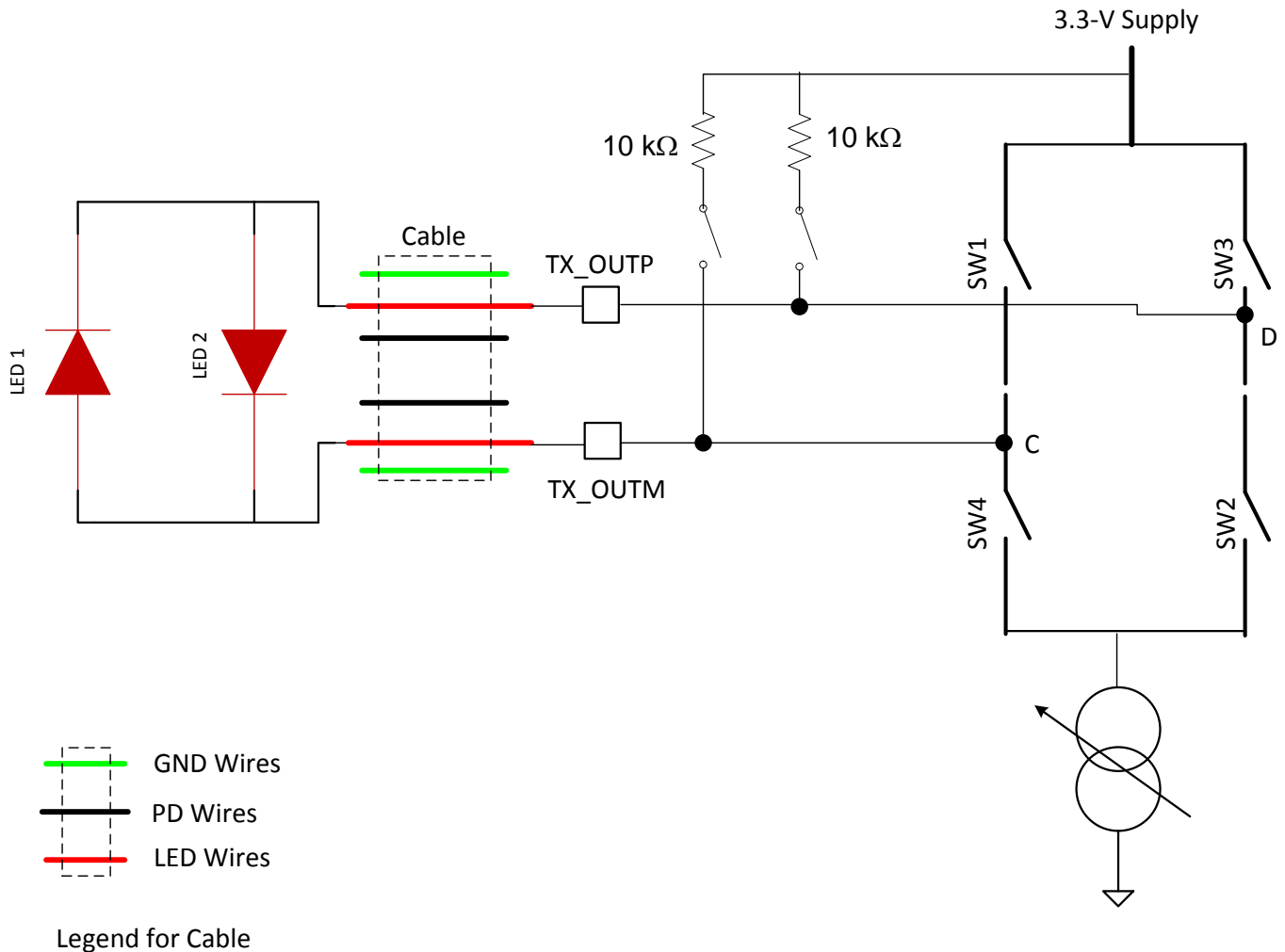
Figure 29. Photodiode Diagnostic

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**Transmitter-Side Fault Detection**

Figure 30 shows the diagnostic for the transmitter-side fault detection.



**Figure 30. Transmitter Diagnostic**

**Diagnostics Module**

The diagnostics module, when enabled, checks for nine types of faults sequentially. The results of all faults are latched in 11 separate flags. At the end of the sequence, the state of the 11 flags are combined to generate two interrupt signals: PD\_ALM for photodiode-related faults and LED\_ALM for transmit-related faults. The status of all flags can also be read using the SPI interface. Table 3 details each fault and flag used.

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**Table 3. Fault and Flag Diagnostics<sup>(1)</sup>**

MODULE	SEQ.	FAULT	TEST AND COMPARE	DESCRIPTION	THRES HOLDS	V1	V1	V1	V1	V2	V3	V1	V1	V2	V3	V3		
						FLAG1	FLAG2	FLAG3	FLAG4	FLAG5	FLAG6	FLAG7	FLAG8	FLAG9	FLAG10	FLAG11		
—	—	No fault	—	—	—	0	0	0	0	0	0	0	0	0	0	0		
PD	1	Rx INP cable shorted to LED cable	Pull-down A and compare	Rx off		1												
				Tx on (SW1 and SW3 on)		1												
				Pull-down A with 10-kΩ resistor		1												
				Compare A with V1		1												
				(A > V1) implies that A is shorted to the LED cable	V1 = 2.5 V	1												
PD	2	Rx INM cable shorted to LED cable	Pull-down B and compare	Rx off			1											
				Tx on (SW1 and SW3 on)			1											
				Pull-down B with 10-kΩ resistor			1											
				Compare B with V1			1											
				(B > V1) implies that B is shorted to the LED cable	V1 = 2.5 V		1											
PD	3	Rx INP cable shorted to GND cable	Connect A to supply and compare	Rx and Tx off, pull A with 10-kΩ resistor to supply				1										
				Compare A with V1				1										
				(A < V1) implies that A is shorted to GND	V1 = 2.5 V			1										
PD	4	Rx INM cable shorted to GND cable	Connect B to supply and compare	Rx and Tx off, pull B with 10-kΩ resistor to supply					1									
				Compare B with V1					1									
				(B < V1) implies that B is shorted to GND	V1 = 2.5 V				1									
PD	5	PD open or shorted	Connect a 1-μA current source at A, connect B to supply with a 10-kΩ resistor, and compare	Rx and Tx off, compare lower node A with V2 and V3						1	1							
				(A > V2) implies that PD is shorted	V2 = 5 V – 0.25 V					1	1							
				(A < V3) implies that PD is open	V3 = 0.25 V							1						

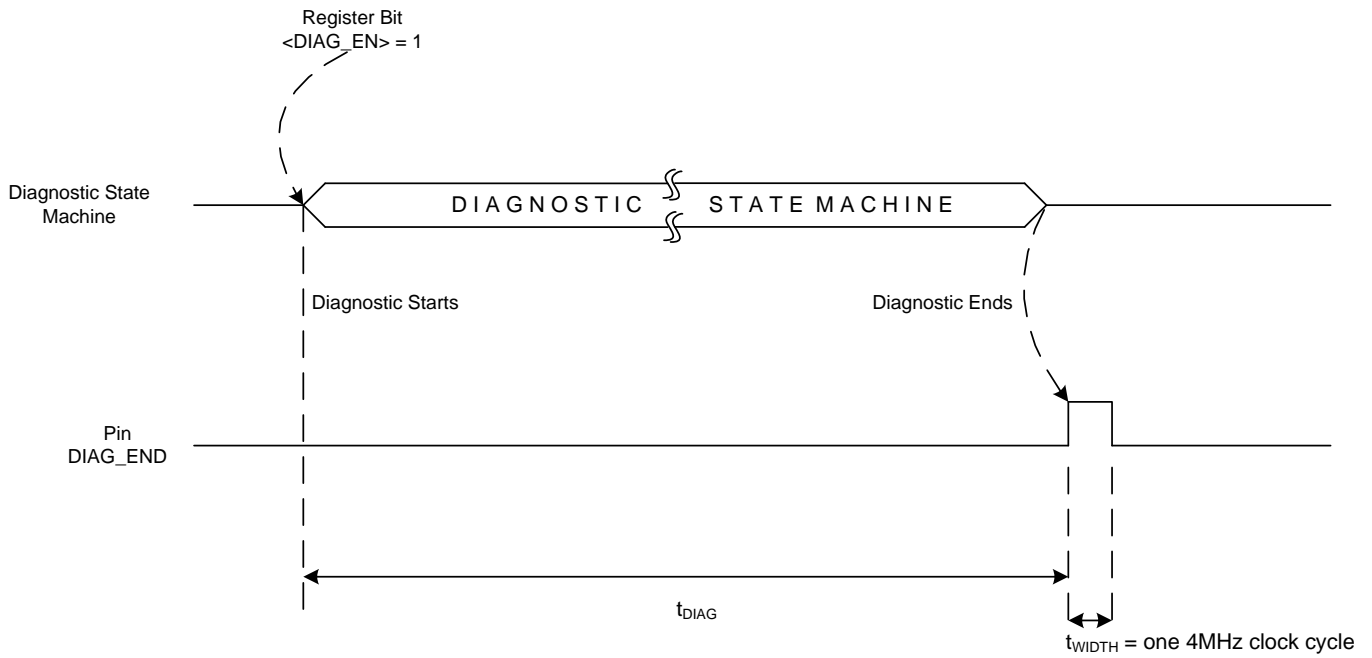
(1) Resistances below 10 kΩ are considered to be shorted.

**Table 3. Fault and Flag Diagnostics<sup>(1)</sup> (continued)**

MODULE	SEQ.	FAULT	TEST AND COMPARE	DESCRIPTION	THRES HOLDS	V1	V1	V1	V1	V2	V3	V1	V1	V2	V3	V3		
						FLAG1	FLAG2	FLAG3	FLAG4	FLAG5	FLAG6	FLAG7	FLAG8	FLAG9	FLAG10	FLAG11		
LED	6	Tx OUTM line shorted to GND cable	Connect node C to supply and compare	Rx and Tx off								1						
				Pull C with 10-kΩ resistor to supply									1					
				Compare C with V1										1				
				(C < V1) implies that C is shorted to GND	V1 = 2.5 V									1				
LED	7	Tx OUTP line shorted to GND cable	Connect node D to supply and compare	Rx and Tx off									1					
				Pull D with 10-kΩ resistor to supply	V1 = 2.5 V									1				
				Compare D with V1										1				
				(D < V1) implies that D is shorted to GND										1				
LED	8	LED open or shorted	Turn on Tx and compare	Tx current source on, turn on S3 and S4										1	1			
				Compare lower node C with V2 and V3										1	1			
				(C > V2) implies that LED is shorted	V2 = 5 V – 0.25 V									1	1			
				(C < V3) implies that LED2 is open	V3 = 0.25 V											1		
LED	9	LED open or shorted	Turn on Tx and compare	Tx current source on, turn on S1 and S2												1		
				Compare lower node D with V3													1	
				(D < V3) implies that LED1 is open	V3 = 0.25 V												1	

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Figure 31 shows the timing for the diagnostic function.



**Figure 31. Diagnostic Timing Diagram**

By default, the diagnostic function takes  $t_{DIAG} = 8 \text{ ms}$  to complete.

## SERIAL PROGRAMMING INTERFACE

The SPI-compatible serial interface consists of four signals: SCLK (serial clock), SPISOMI (serial interface data output), SPISIMO (serial interface data input), and SPISTE (serial interface enable).

The serial clock (SCLK) is the serial peripheral interface (SPI) serial clock. SCLK shifts in commands and shifts out data from the device. SCLK features a Schmitt-triggered input and clocks data out on the SPISOMI. Data are clocked in on the SPISIMO pin. Even though the input has hysteresis, TI recommends keeping SCLK as clean as possible to prevent glitches from accidentally shifting the data. If SCLK is held low for TBD ms, the serial interface resets and the next SCLK pulse starts a new communication cycle. This timeout feature can be used to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

The SPI serial out master in (SPISOMI) pin is used with SCLK to clock out the AFE4400 data. The SPI serial in master out (SPISIMO) pin is used with SCLK to clock in data to the AFE4400. The SPI serial interface enable (SPISTE) pin enables the serial interface to clock data on the SPISIMO pin in to the device.

## READING AND WRITING DATA

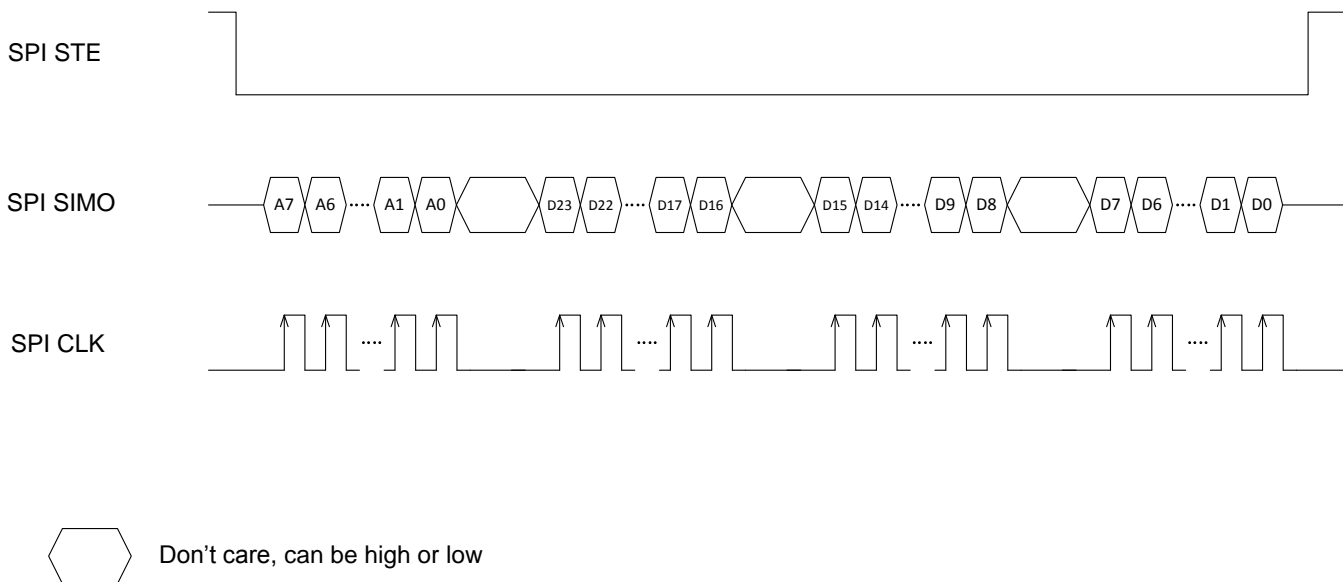
The device has a set of internal registers that can be accessed by the serial programming interface formed by the SPISTE, SCLK, SPISIMO, and SPISOMI pins.

### Writing Data

When SPISTE is low,

- Serially shifting bits into the device is enabled.
- Serial data (on the SPISIMO pin) are latched at every SCLK rising edge.
- The serial data are loaded into the register at every 32nd SCLK rising edge.

In case the word length exceeds a multiple of 32 bits, the excess bits are ignored. Data can be loaded in multiples of 32-bit words within a single active SPISTE pulse. The first eight bits form the register address and the remaining 24 bits form the register data. [Figure 32](#) shows a diagram of the write timing.

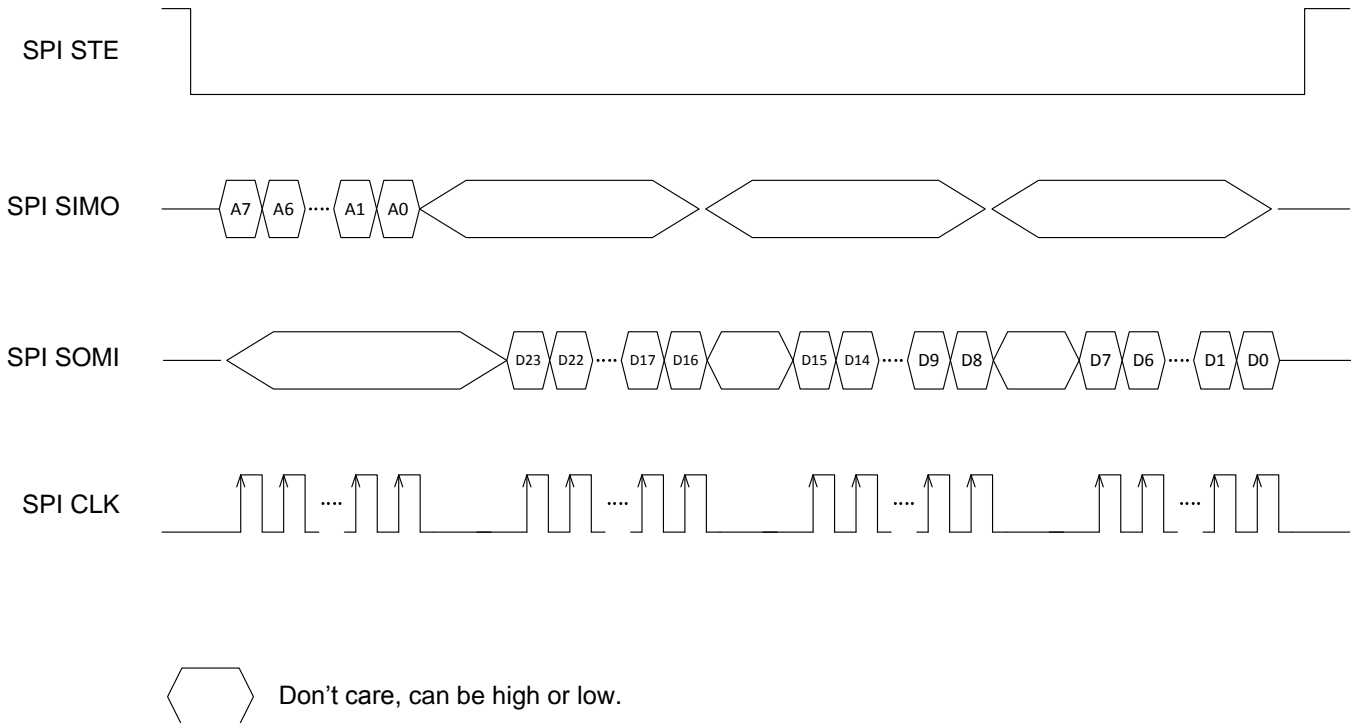


**Figure 32. AFE SPI Write Timing Diagram**

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## Reading Data

The AFE4400 includes a mode where the contents of the internal registers can be read back on the SPISOMI pin. This mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the AFE. To enable this mode, first set the SPI\_READ register bit using the SPI write command, as described in the [Writing Data](#) section. In the next command, specify the SPI register address with the desired content to be read. Within the same SPI command sequence, the AFE outputs the contents of the specified register on the SPISOMI pin. [Figure 33](#) shows a timing diagram for the SPI read operation.



- (1) The SPI\_READ register bit must be enabled before attempting a serial readout from the AFE.
- (2) Specify the register address of the content that must be readback on bits A[7:0].
- (3) The AFE outputs the contents of the specified register on the SPISOMI pin.

**Figure 33. AFE SPI Read Timing Diagram**

## Register Initialization

After power-up, the internal registers **must** be initialized to the default values. This initialization can be done in one of two ways:

- Through a hardware reset by applying a low-going pulse on the  $\overline{\text{RESET}}$  pin, or
- By applying a software reset. Using the serial interface, set SW\_RESET (bit D3 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets to '0'. In this case, the RESET pin is kept high (inactive).

## AFE SPI Interface Design Considerations

Note that when the AFE4400 is deselected, the SPISOMI, CLKOUT, ADC\_RDY, PD\_ALM, LED\_ALM, and DIAG\_END digital output pins do not enter a 3-state mode. This condition, therefore, must be taken into account when connecting multiple devices to the SPI port and for power-management considerations.

## AFE REGISTER MAP

The AFE consists of a set of registers that can be used to configure it, such as receiver timings, I-V amplifier settings, transmit LED currents, and so forth. The registers and their contents are listed in [Table 4](#). These registers can be accessed using the AFE SPI interface.

Table 4. AFE Register Map

NAME	ADDRESS		REGISTER DATA																								
	Hex	Dec	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
CONTROL0	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SW_RST	DIAG_EN	TIM_COUNT_RST	SPI_READ	
LED2STC	01	1	0	0	0	0	0	0	0	0	LED2STC[15:0]																
LED2ENDC	02	2	0	0	0	0	0	0	0	0	LED2ENDC[15:0]																
LED2LEDSTC	03	3	0	0	0	0	0	0	0	0	LED2LEDSTC[15:0]																
LED2LEDENDC	04	4	0	0	0	0	0	0	0	0	LED2LEDENDC[15:0]																
ALED2STC	05	5	0	0	0	0	0	0	0	0	ALED2STC[15:0]																
ALED2ENDC	06	6	0	0	0	0	0	0	0	0	ALED2ENDC[15:0]																
LED1STC	07	7	0	0	0	0	0	0	0	0	LED1STC[15:0]																
LED1ENDC	08	8	0	0	0	0	0	0	0	0	LED1ENDC[15:0]																
LED1LEDSTC	09	9	0	0	0	0	0	0	0	0	LED1LEDSTC[15:0]																
LED1LEDENDC	0A	10	0	0	0	0	0	0	0	0	LED1LEDENDC[15:0]																
ALED1STC	0B	11	0	0	0	0	0	0	0	0	ALED1STC[15:0]																
ALED1ENDC	0C	12	0	0	0	0	0	0	0	0	ALED1ENDC[15:0]																
LED2CONVST	0D	13	0	0	0	0	0	0	0	0	LED2CONVST[15:0]																
LED2CONVST	0E	14	0	0	0	0	0	0	0	0	LED2CONVST[15:0]																
ALED2CONVST	0F	15	0	0	0	0	0	0	0	0	ALED2CONVST[15:0]																
ALED2CONVEND	10	16	0	0	0	0	0	0	0	0	ALED2CONVEND[15:0]																
LED1CONVST	11	17	0	0	0	0	0	0	0	0	LED1CONVST[15:0]																
LED1CONVEND	12	18	0	0	0	0	0	0	0	0	LED1CONVEND[15:0]																
ALED1CONVST	13	19	0	0	0	0	0	0	0	0	ALED1CONVST[15:0]																
ALED1CONVEND	14	20	0	0	0	0	0	0	0	0	ALED1CONVEND[15:0]																
ADCRSTCNT0	15	21	0	0	0	0	0	0	0	0	ADCRSTCNT0[15:0]																
ADCRSTENDCT0	16	22	0	0	0	0	0	0	0	0	ADCRSTENDCT0[15:0]																
ADCRSTSTCT1	17	23	0	0	0	0	0	0	0	0	ADCRSTSTCT1[15:0]																
ADCRSTENDCT1	18	24	0	0	0	0	0	0	0	0	ADCRSTENDCT1[15:0]																
ADCRSTSTCT2	19	25	0	0	0	0	0	0	0	0	ADCRSTSTCT2[15:0]																
ADCRSTENDCT2	1A	26	0	0	0	0	0	0	0	0	ADCRSTENDCT2[15:0]																
ADCRSTSTCT3	1B	27	0	0	0	0	0	0	0	0	ADCRSTSTCT3[15:0]																
ADCRSTENDCT3	1C	28	0	0	0	0	0	0	0	0	ADCRSTENDCT3[15:0]																
PRPCOUNT	1D	29	0	0	0	0	0	0	0	0	PRPCOUNT[15:0]																
CONTROL1	1E	30	0	0	0	0	0	0	0	0	0	0	0	0	CLKALMPIN[2:0]			TIMEREN	0	0	0	0	0	0	1	0	
SPARE1	1F	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TIAGAIN	20	32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4. AFE Register Map (continued)

NAME	ADDRESS		REGISTER DATA																							
	Hex	Dec	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TIA_AMB_GAIN	21	33	0	0	0	0	AMBDAC[3:0]				0	0	0	0	0	0	0	0	CF_LED[4:0]				RF_LED[2:0]			
LEDCNTRL	22	34	0	0	0	0	0	0	LEDCUROFF	1	LED2[7:0]							LED1[7:0]								
CONTROL2	23	35	0	0	0	0	0	0	1	0	0	0	0	0	TXBRGMOD	0	XTALDIS	1	0	0	0	0	0	PDNTX	PDNRX	PDNAFE
SPARE2	24	36	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPARE3	25	37	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPARE4	26	38	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED1	27	39	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED2	28	40	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ALARM	29	41	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ALMPINLKEN	0	0	0	0	0	0	0
LED2VAL	2A	42	LED2VAL[23:0]																							
ALED2VAL	2B	43	ALED2VAL[23:0]																							
LED1VAL	2C	44	LED1VAL[23:0]																							
ALED1VAL	2D	45	ALED1VAL[23:0]																							
LED2-ALED2VAL	2E	46	LED2-ALED2VAL[23:0]																							
LED1-ALED1VAL	2F	47	LED1-ALED1VAL[23:0]																							
DIAG	30	48	0	0	0	0	0	0	0	0	0	0	0	LED_ALM	PD_ALM	LED1OPEN	LED2OPEN	LEDSC	OUTPSHGND	OUTNSHGND	PDOC	PDSC	INNSCGND	INPSCGND	INNSCLED	INPSCLED

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**AFE REGISTER DESCRIPTION**
**CONTROL0: Control Register 0 (Address = 00h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	SW_RST	DIAG_EN	TIM_COUNT_RST	SPI_READ

This register is used for AFE software and count timer reset, diagnostics enable, and SPI read functions.

**Bits D[23:4] Must be '0'**

**Bit D3 SW\_RST: Software reset**

0 = No action (default after reset)

1 = Software reset applied; resets all internal registers to the default values and self-clears to '0'

**Bit D2 DIAG\_EN: Diagnostic enable**

0 = No action (default after reset)

1 = Diagnostic mode is enabled and the diagnostics sequence starts when this bit is set. At the end of the sequence, all fault status are stored in the [DIAG: Diagnostics Flag Register](#). Afterwards, the DIAG\_EN register bit self-clears to '0'.

**Bit D1 TIM\_CNT\_RST: Timer counter reset**

0 = Disables timer counter reset, required for normal timer operation (default after reset)

1 = Timer counters are in reset state

**Bit D0 SPI\_READ: SPI read**

0 = SPI read is disabled (default after reset)

1 = SPI read is enabled

**LED2STC: Sample LED2 Start Count Register (Address = 01h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2STC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2STC[15:0]											

This register sets the start timing value for the LED2 signal sample.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] LED2STC[15:0]: Sample LED2 start count**

The contents of this register can be used to position the start of the sample LED2 signal with respect to the pulse repetition period (PRP), as specified in the PRPCOUNT register. The count is specified as the number of

4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**LED2ENDC: Sample LED2 End Count Register (Address = 02h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2ENDC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2ENDC[15:0]											

This register sets the end timing value for the LED2 signal sample.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] LED2ENDC[15:0]: Sample LED2 end count**

The contents of this register can be used to position the end of the sample LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**LED2LEDSTC: LED2 LED Start Count Register (Address = 03h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2LEDSTC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2LEDSTC[15:0]											

This register sets the start timing value for when the LED2 signal turns on.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] LED2LEDSTC[15:0]: LED2 start count**

The contents of this register can be used to position the start of the LED2 with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**LED2LEDENDC: LED2 LED End Count Register (Address = 04h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2LEDENDC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2LEDENDC[15:0]											

This register sets the end timing value for when the LED2 signal turns off.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] LED2LEDENDC[15:0]: LED2 end count**

The contents of this register can be used to position the end of the LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**ALED2STC: Sample Ambient LED2 Start Count Register (Address = 05h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2STC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2STC[15:0]											

This register sets the start timing value for the ambient LED2 signal sample.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ALED2STC[15:0]: Sample ambient LED2 start count**

The contents of this register can be used to position the start of the sample ambient LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**ALED2ENDC: Sample Ambient LED2 End Count Register (Address = 06h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2ENDC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2ENDC[15:0]											

This register sets the end timing value for the ambient LED2 signal sample.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ALED2ENDC[15:0]: Sample ambient LED2 end count**

The contents of this register can be used to position the end of the sample ambient LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**LED1STC: Sample LED1 Start Count Register (Address = 07h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1STC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1STC[15:0]											

This register sets the start timing value for the LED1 signal sample.

**Bits D[23:17] Must be '0'**

**Bits D[16:0] LED1STC[15:0]: Sample LED1 start count**

The contents of this register can be used to position the start of the sample LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of

4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**LED1ENDC: Sample LED1 End Count (Address = 08h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1ENDC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1ENDC[15:0]											

This register sets the end timing value for the LED1 signal sample.

**Bits D[23:17] Must be '0'**

**Bits D[16:0] LED1ENDC[15:0]: Sample LED1 end count**

The contents of this register can be used to position the end of the sample LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of

4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**LED1LEDSTC: LED1 LED Start Count Register (Address = 09h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1LEDSTC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1LEDSTC[15:0]											

This register sets the start timing value for when the LED1 signal turns on.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] LED1LEDSTC[15:0]: LED1 start count**

The contents of this register can be used to position the start of the LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**LED1LEDENDC: LED1 LED End Count Register (Address = 0Ah, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1LEDENDC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1LEDENDC[15:0]											

This register sets the end timing value for when the LED1 signal turns off.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] LED1LEDENDC[15:0]: LED1 end count**

The contents of this register can be used to position the end of the LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**ALED1STC: Sample Ambient LED1 Start Count Register (Address = 0Bh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1STC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1STC[15:0]											

This register sets the start timing value for the ambient LED1 signal sample.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ALED1STC[15:0]: Sample ambient LED1 start count**

The contents of this register can be used to position the start of the sample ambient LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**ALED1ENDC: Sample Ambient LED1 End Count Register (Address = 0Ch, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1ENDC[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1ENDC[15:0]											

This register sets the end timing value for the ambient LED1 signal sample.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ALED1ENDC[15:0]: Sample ambient LED1 end count**

The contents of this register can be used to position the end of the sample ambient LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**LED2CONVST: LED2 Convert Start Count Register (Address = 0Dh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2CONVST[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2CONVST[15:0]											

This register sets the start timing value for the LED2 conversion.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] LED2CONVST[15:0]: LED2 convert start count**

The contents of this register can be used to position the start of the LED2 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**LED2CONVST: LED2 Convert End Count Register (Address = 0Eh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2CONVST[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2CONVST[15:0]											

This register sets the end timing value for the LED2 conversion.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] LED2CONVST[15:0]: LED2 convert end count**

The contents of this register can be used to position the end of the LED2 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**ALED2CONVST: LED2 Ambient Convert Start Count Register (Address = 0Fh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2CONVST[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2CONVST[15:0]											

This register sets the start timing value for the ambient LED2 conversion.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ALED2CONVST[15:0]: LED2 ambient convert start count**

The contents of this register can be used to position the start of the LED2 ambient conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**ALED2CONVEND: LED2 Ambient Convert End Count Register (Address = 10h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2CONVEND[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2CONVEND[15:0]											

This register sets the end timing value for the ambient LED2 conversion.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ALED2CONVEND[15:0]: LED2 ambient convert end count**

The contents of this register can be used to position the end of the LED2 ambient conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**LED1CONVST: LED1 Convert Start Count Register (Address = 11h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1CONVST[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1CONVST[15:0]											

This register sets the start timing value for the LED1 conversion.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] LED1CONVST[15:0]: LED1 convert start count**

The contents of this register can be used to position the start of the LED1 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**LED1CONVEND: LED1 Convert End Count Register (Address = 12h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1CONVEND[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1CONVEND[15:0]											

This register sets the end timing value for the LED1 conversion.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] LED1CONVEND[15:0]: LED1 convert end count**

The contents of this register can be used to position the end of the LED1 conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**ALED1CONVST: LED1 Ambient Convert Start Count Register (Address = 13h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1CONVST[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1CONVST[15:0]											

This register sets the start timing value for the ambient LED1 conversion.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ALED1CONVST[15:0]: LED1 ambient convert start count**

The contents of this register can be used to position the start of the LED1 ambient conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**ALED1CONVEND: LED1 Ambient Convert End Count Register (Address = 14h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1CONVEND[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1CONVEND[15:0]											

This register sets the end timing value for the ambient LED1 conversion.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ALED1CONVEND[15:0]: LED1 ambient convert end count**

The contents of this register can be used to position the end of the LED1 ambient conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the [Using the Timer Module](#) section for details.

0 = 0000h

1 = PRP value

**ADCRSTCNT0: ADC Reset 0 Start Count Register (Address = 15h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTCNT0[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTCNT0[15:0]											

This register sets the start position of the ADC0 reset conversion signal.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ADCRSTCNT0[15:0]: ADC  $\overline{\text{RESET}}$  0 start count**

The contents of this register can be used to position the start of the ADC reset conversion signal (default value after reset is 0000h). Refer to the [Using the Timer Module](#) section for details.

**ADCRSTENDCT0: ADC Reset 0 End Count Register (Address = 16h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT0[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT0[15:0]											

This register sets the end position of the ADC0 reset conversion signal.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ADCRSTENDCT0[15:0]: ADC  $\overline{\text{RESET}}$  0 end count**

The contents of this register can be used to position the end of the ADC reset conversion signal (default value after reset is 0000h). Refer to the [Using the Timer Module](#) section for details.



**ADCRSTSTCT1: ADC Reset 1 Start Count Register (Address = 17h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTSTCT1[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTSTCT1[15:0]											

This register sets the start position of the ADC1 reset conversion signal.

**Bits D[23:16]**      **Must be '0'**

**Bits D[15:0]**      **ADCRSTSTCT1[15:0]: ADC  $\overline{\text{RESET}}$  1 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the [Using the Timer Module](#) section for details.

**ADCRSTENDCT1: ADC Reset 1 End Count Register (Address = 18h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT1[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT1[15:0]											

This register sets the end position of the ADC1 reset conversion signal.

**Bits D[23:16]**      **Must be '0'**

**Bits D[15:0]**      **ADCRSTENDCT1[15:0]: ADC  $\overline{\text{RESET}}$  1 end count**

The contents of this register can be used to position the end of the ADC reset conversion. Refer to the [Using the Timer Module](#) section for details.

**ADCRSTSTCT2: ADC Reset 2 Start Count Register (Address = 19h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTSTCT2[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTSTCT2[15:0]											

This register sets the start position of the ADC2 reset conversion signal.

**Bits D[23:16]**      **Must be '0'**

**Bits D[15:0]**      **ADCRSTSTCT2[15:0]: ADC  $\overline{\text{RESET}}$  2 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the [Using the Timer Module](#) section for details.

**ADCRSTENDCT2: ADC Reset 2 End Count Register (Address = 1Ah, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT2[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT2[15:0]											

This register sets the end position of the ADC2 reset conversion signal.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ADCRSTENDCT2[15:0]: ADC  $\overline{\text{RESET}}$  2 end count**

The contents of this register can be used to position the end of the ADC reset conversion. Refer to the [Using the Timer Module](#) section for details.

**ADCRSTSTCT3: ADC Reset 3 Start Count Register (Address = 1Bh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTSTCT3[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTSTCT3[15:0]											

This register sets the start position of the ADC3 reset conversion signal.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ADCRSTSTCT3[15:0]: ADC  $\overline{\text{RESET}}$  3 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the [Using the Timer Module](#) section for details.

**ADCRSTENDCT3: ADC Reset 3 End Count Register (Address = 1Ch, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT3[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT3[15:0]											

This register sets the end position of the ADC3 reset conversion signal.

**Bits D[23:16] Must be '0'**

**Bits D[15:0] ADCRSTENDCT3[15:0]: ADC  $\overline{\text{RESET}}$  3 end count**

The contents of this register can be used to position the end of the ADC reset conversion signal (default value after reset is 0000h). Refer to the [Using the Timer Module](#) section for details.

**PRPCOUNT: Pulse Repetition Period Count Register (Address = 1Dh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	PRPCOUNT[15:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PRPCOUNT[15:0]											

This register sets the device pulse repetition period count.

**Bits D[23:16]**      **Must be '0'**

**Bits D[15:0]**      **PRPCOUNT[15:0]: Pulse repetition period count**

The contents of this register can be used to set the pulse repetition period (in number of clock cycles of the 4-MHz clock).

**CONTROL1: Control Register 1 (Address = 1Eh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CLKALMPIN[2:0]			TIMEREN	0	0	0	0	0	0	1	0

This register configures the clock alarm pin and timer.

**Bits D[23:12]**      **Must be '0'**

**Bits D[11:9]**      **CLKALMPIN[2:0]: Clocks on ALM pins**

Internal clocks can be brought to the PD\_ALM and LED\_ALM pins for monitoring. Note that the CLKALMPIN[2:0] register bits must be set before using this register bit. [Table 5](#) defines the settings for the two alarm pins.

**Bit D8**              **TIMEREN: Timer enable**

0 = Timer module is disabled and all internal clocks are off (default after reset)  
1 = Timer module is enabled

**Bits D[7:2]**        **Must be '0'**

**Bit D1**              **Must be '1'**

**Bit D0**              **Must be '0'**

**Table 5. PD\_ALM and LED\_ALM Pin Settings**

CLKALMPIN[2:0]	PD_ALM PIN SIGNAL	LED_ALM PIN SIGNAL
000	Sample LED2	Sample LED1
001	LED2 pulse	LED1 pulse
010	Sample LED2	Sample LED1 pulse
011	LED2 convert	LED1 convert
100	LED2 ambient	LED1 ambient
101	No output	No output
110	No output	No output
111	No output	No output

**SPARE1: SPARE1 Register For Future Use (Address = 1Fh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

**Bits D[23:0]      Must be '0'**

**TIAGAIN: Transimpedance Amplifier Gain Setting Register (Address = 20h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is reserved for factory use.

**Bits D[23:0]      Must be '0'**

**TIA\_AMB\_GAIN: Transimpedance Amplifier and Ambient Cancellation Stage Gain Register**  
**(Address = 21h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	AMBDAC[3:0]				0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	CF_LED[4:0]				RF_LED[2:0]			

This register configures the ambient light cancellation amplifier gain, cancellation current, and filter corner frequency.

**Bits D[23:20] Must be '0'**

**Bits D[19:16] AMBDAC[3:0]: Ambient DAC value**

These bits set the value of the cancellation current.

0000 = 0 $\mu$ A (default after reset)	1000 = 8 $\mu$ A
0001 = 1 $\mu$ A	1001 = 9 $\mu$ A
0010 = 2 $\mu$ A	1010 = 10 $\mu$ A
0011 = 3 $\mu$ A	1011 = Do not use
0100 = 4 $\mu$ A	1100 = Do not use
0101 = 5 $\mu$ A	1101 = Do not use
0110 = 6 $\mu$ A	1110 = Do not use
0111 = 7 $\mu$ A	1111 = Do not use

**Bits D[15:8] Must be '0'**

**Bits D[7:3] CF\_LED[4:0]: Program  $C_F$  for LEDs**

00000 = 5 pF (default after reset)	00100 = 25 pF + 5 pF
00001 = 5 pF + 5 pF	01000 = 50 pF + 5 pF
00010 = 15 pF + 5 pF	10000 = 150 pF + 5 pF

Note that any combination of these  $C_F$  settings is also supported by setting multiple bits to '1'. For example, to obtain  $C_F = 100$  pF, set D[7:3] = 01111.

**Bits D[2:0] RF\_LED[2:0]: Program  $R_F$  for LEDs**

000 = 500 k $\Omega$	100 = 25 k $\Omega$
001 = 250 k $\Omega$	101 = 10 k $\Omega$
010 = 100 k $\Omega$	110 = 1 M $\Omega$
011 = 50 k $\Omega$	111 = None

**LEDCNTRL: LED Control Register (Address = 22h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	LEDCUR OFF	1	LED2[7:0]			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2[7:0]						LED1[7:0]					

This register sets the LED current range and the LED2 and LED1 drive current.

**Bits D[23:18] Must be '0'**

**Bit D17 LEDCUROFF: Turns the LED current source on or off**

0 = On (50 mA)

1 = Off

**Bit D16 Must be '1'**

**Bits D[15:8] LED2[7:0]: Program LED current for LED2 signal**

Use these register bits to specify the LED current setting for LED2 (default after reset is 00h).

The nominal value of the LED current is given by [Equation 3](#), where the full-scale LED current is 75 mA.

**Bits D[7:0] LED1[7:0]: Program LED current for LED1 signal**

Use these register bits to specify the LED current setting for LED1 (default after reset is 00h).

The nominal value of LED current is given by [Equation 4](#), where the full-scale LED current is 75 mA.

$$\frac{\text{LED2}[7:0]}{256} \times \text{Full-Scale Current} \quad (3)$$

$$\frac{\text{LED1}[7:0]}{256} \times \text{Full-Scale Current} \quad (4)$$

**CONTROL2: Control Register 2 (Address = 23h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	1	0	0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TXBRG MOD	0	XTAL DIS	1	0	0	0	0	0	PDNTX	PDNRX	PDNAFE

This register controls the LED transmitter, crystal, and the AFE, transmitter, and receiver power modes.

**Bits D[23:18] Must be '0'**

**Bit D17 Must be '1'**

**Bits D[16:12] Must be '0'**

**Bit D11 TXBRGMOD: Tx bridge mode**

0 = LED driver is configured as an H-bridge (default after reset)

1 = LED driver is configured as a push-pull

**Bit D10 Must be '0'**

**Bit D9 XTALDIS: Crystal disable mode**

0 = The crystal module is enabled; the 8-MHz crystal must be connected to the XIN and XOUT pins

1 = The crystal module is disabled; an external 8-MHz clock must be applied to the XIN pin

**Bit D8 Must be '1'**

**Bits D[7:3] Must be '0'**

**Bit D2 PDN\_TX: Tx power-down**

0 = The Tx is powered up (default after reset)

1 = Only the Tx module is powered down

**Bit D1 PDN\_RX: Rx power-down**

0 = The Rx is powered up (default after reset)

1 = Only the Rx module is powered down

**Bit D0 PDN\_AFE: AFE power-down**

0 = The AFE is powered up (default after reset)

1 = The entire AFE is powered down (including the Tx, Rx, and diagnostics blocks)

**SPARE2: SPARE2 Register For Future Use (Address = 24h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

**Bits D[23:0] Must be '0'**

**SPARE3: SPARE3 Register For Future Use (Address = 25h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

**Bits D[23:0] Must be '0'**

**SPARE4: SPARE4 Register For Future Use (Address = 26h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

**Bits D[23:0] Must be '0'**

**RESERVED1: RESERVED1 Register For Factory Use Only (Address = 27h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is reserved for factory use. Readback values vary between devices.

**Bits D[23:0] Must be '0'**

**RESERVED2: RESERVED2 Register For Factory Use Only (Address = 28h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is reserved for factory use. Readback values vary between devices.

**Bits D[23:0] Must be '0'**



**ALARM: Alarm Register (Address = 29h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	ALMPIN CLKEN	0	0	0	0	0	0	0

This register controls the Alarm pin functionality.

**Bits D[23:8] Must be '0'**

**Bit D7 ALMPINCLKEN: Alarm pin clock enable**

0 = Disables the monitoring of internal clocks; the PD\_ALM and LED\_ALM pins function as diagnostic fault alarm output pins (default after reset)

1 = Enables the monitoring of internal clocks; these clocks can be brought out on PD\_ALM and LED\_ALM selectively (depending on the value of the CLKALMPIN[2:0] register bits).

**Bits D[6:0] Must be '0'**

**LED2VAL: LED2 Digital Sample Value Register (Address = 2Ah, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED2VAL[23:0]											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2VAL[23:0]											

**Bits D[23:0] LED2VAL[23:0]: LED2 digital value**

This register contains the digital value of the latest LED2 sample converted by the ADC. The ADC\_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

**ALED2VAL: Ambient LED2 Digital Sample Value Register (Address = 2Bh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
ALED2VAL[23:0]											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2VAL[23:0]											

**Bits D[23:0] ALED2VAL[23:0]: LED2 ambient digital value**

This register contains the digital value of the latest LED2 ambient sample converted by the ADC. The ADC\_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

**LED1VAL: LED1 Digital Sample Value Register (Address = 2Ch, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED1VAL[23:0]											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1VAL[23:0]											

**Bits D[23:0] LED1VAL[23:0]: LED1 digital value**

This register contains the digital value of the latest LED1 sample converted by the ADC. The ADC\_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

**ALED1VAL: Ambient LED1 Digital Sample Value Register (Address = 2Dh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
ALED1VAL[23:0]											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1VAL[23:0]											

**Bits D[23:0] ALED1VAL[23:0]: LED1 ambient digital value**

This register contains the digital value of the latest LED1 ambient sample converted by the ADC. The ADC\_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

**LED2-ALED2VAL: LED2-Ambient LED2 Digital Sample Value Register (Address = 2Eh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED2-ALED2VAL[23:0]											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2-ALED2VAL[23:0]											

**Bits D[23:0] LED2-ALED2VAL[23:0]: (LED2 – LED2 ambient) digital value**

This register contains the digital value of the LED2 sample after the LED2 ambient is subtracted. The host processor must readout this register before the next sample is converted by the AFE.

**LED1-ALED1VAL: LED1-Ambient LED1 Digital Sample Value Register (Address = 2Fh, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED1-ALED1VAL[23:0]											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1-ALED1VAL[23:0]											

**Bits D[23:0] LED1-ALED1VAL[23:0]: (LED1 – LED1 ambient) digital value**

This register contains the digital value of the LED1 sample after the LED1 ambient is subtracted from it. The host processor must readout this register before the next sample is converted by the AFE.

**DIAG: Diagnostics Flag Register (Address = 30h, Reset Value = 0000h)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	LED_ ALM
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PD_ ALM	LED1 OPEN	LED2 OPEN	LEDSC	OUTPSH GND	OUTNSH GND	PDOC	PDSC	INNSC GND	INPSC GND	INNSC LED	INPSC LED

This register is read only. This register contains the status of all diagnostic flags at the end of the diagnostics sequence. The end of the diagnostics sequence is indicated by the signal going high on DIAG\_END pin.

**Bits D[23:13]      Read only**
**Bit D12            LED\_ALM: LED alarm status diagnostic flag**

This bit indicates the status of LED\_ALM (and the LED\_ALM pin).  
 0 = No fault (default after reset)  
 1 = Fault present

**Bit D11            PD\_ALM: Power-down alarm status diagnostic flag**

This bit indicates the status of PD\_ALM (and the PD\_ALM pin).  
 0 = No fault (default after reset)  
 1 = Fault present

**Bit D10            LED1OPEN: LED1 open diagnostic flag**

This bit indicates that LED1 is open.  
 0 = No fault (default after reset)  
 1 = Fault present

**Bit D9             LED2OPEN: LED2 open diagnostic flag**

This bit indicates that LED2 is open.  
 0 = No fault (default after reset)  
 1 = Fault present

**Bit D8             LEDSC: LED short diagnostic flag**

This bit indicates an LED short.  
 0 = No fault (default after reset)  
 1 = Fault present

**Bit D7             OUTPSHGND: OUTP to GND diagnostic flag**

This bit indicates that OUTP is shorted to the GND cable.  
 0 = No fault (default after reset)  
 1 = Fault present

**Bit D6             OUTNSHGND: OUTN to GND diagnostic flag**

This bit indicates that OUTN is shorted to the GND cable.  
 0 = No fault (default after reset)  
 1 = Fault present

**Bit D5             PDOC: PD open diagnostic flag**

This bit indicates that PD is open.  
 0 = No fault (default after reset)  
 1 = Fault present

**Bit D4             PDSC: PD short diagnostic flag**

This bit indicates a PD short.  
 0 = No fault (default after reset)  
 1 = Fault present

- Bit D3**                    **INNSCGND: INN to GND diagnostic flag**  
This bit indicates a short from the INN pin to the GND cable.  
0 = No fault (default after reset)  
1 = Fault present
- Bit D2**                    **INPSCGND: INP to GND diagnostic flag**  
This bit indicates a short from the INP pin to the GND cable.  
0 = No fault (default after reset)  
1 = Fault present
- Bit D1**                    **INNSCLED: INN to LED diagnostic flag**  
This bit indicates a short from the INN pin to the LED cable.  
0 = No fault (default after reset)  
1 = Fault present
- Bit D0**                    **INPSCLED: INP to LED diagnostic flag**  
This bit indicates a short from the INP pin to the LED cable.  
0 = No fault (default after reset)  
1 = Fault present

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
AFE4400RHAR	PREVIEW	VQFN	RHA	40	2500	TBD	Call TI	Call TI	
AFE4400RHAT	PREVIEW	VQFN	RHA	40	250	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

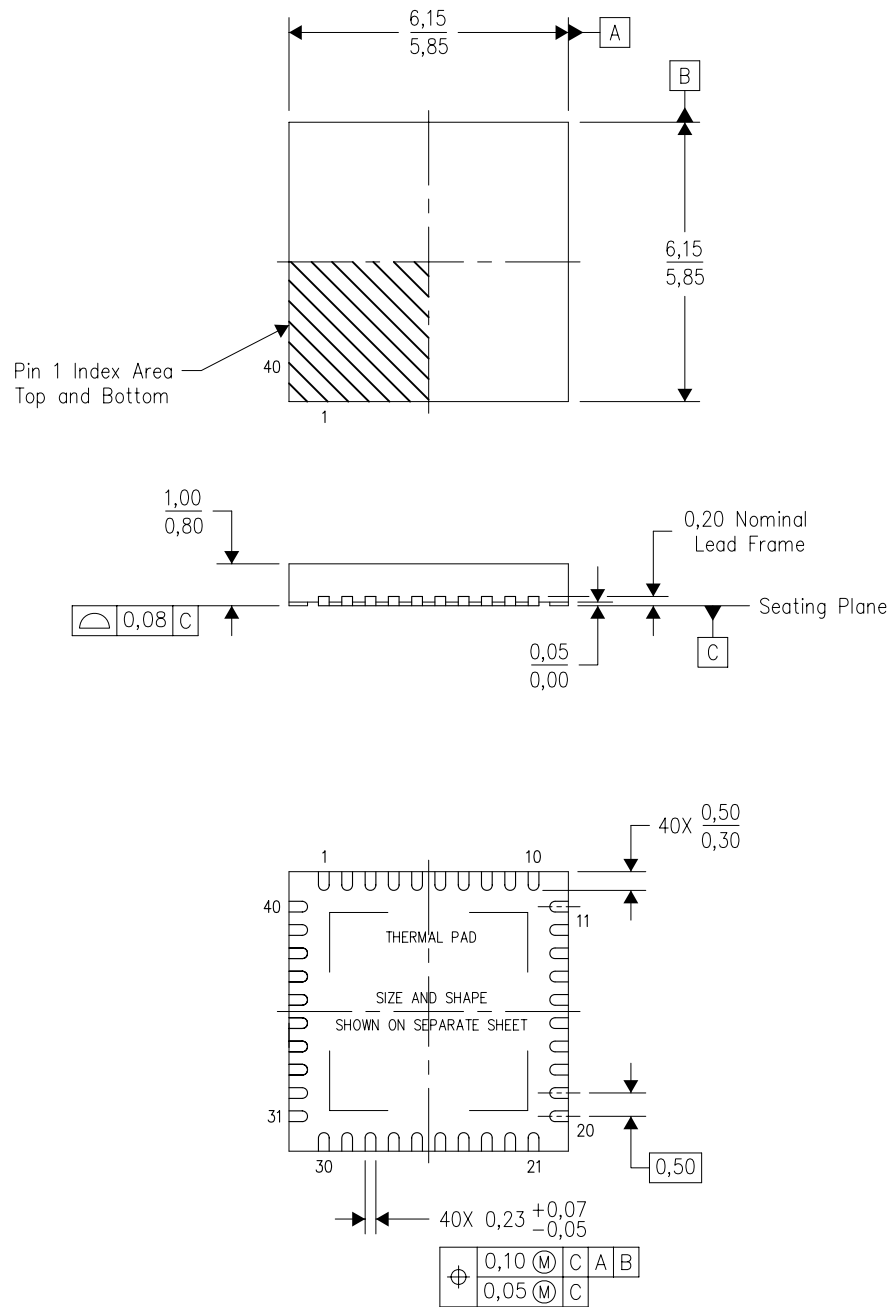
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4204276/E 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Package complies to JEDEC MO-220 variation VJJD-2.

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