

**0.5 Micron CMOS Pad Library
Datasheets
AMI500HXPM 3.3 Volt
Section 4
Revision 1.1**

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Pad
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Pad
Logic

DATASHEETS

Description

IDCI3 is an inverting, CMOS-level input buffer piece.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> </tr> </tbody> </table>	PADM	QC	L	H	H	L	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	PADM	4.90 pF
PADM	QC											
L	H											
H	L											
	Load											
PADM	4.90 pF											

HDL Syntax

Verilog IDCI3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCI3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	16.522	nA
EQL_{pd}	12.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	t_{PLH}	0.724	0.867	1.009	1.133	1.267
			t_{PHL}	0.945	1.102	1.258	1.378	1.486

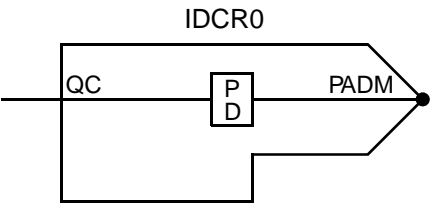
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Pad Logic

AMI500HXPM 0.5 micron CMOS Pad Library

Description

IDCR0 is a non-buffered, resistive analog interface input piece with ESD protection.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	PADM	4.90 pF
PADM	QC											
L	L											
H	H											
	Load											
PADM	4.90 pF											

HDL Syntax

Verilog IDCR0 *inst_name* (QC, PADM);
 VHDL *inst_name*: IDCR0 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	4.265	nA
EQL_{pd}	2.1	Eq-load

See page 2-13 for power equation.

Note: This special purpose, "resistive input" pad is not intended for use as a general input pad.

AMI500HXPM 0.5 micron CMOS Pad Library

Description

IDCS3 is a non-inverting, CMOS-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	PADM	4.90 pF
PADM	QC											
L	L											
H	H											
	Load											
PADM	4.90 pF											

HDL Syntax

Verilog IDCS3 *inst_name* (QC, PADM);

VHDL *inst_name*: IDCS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	15.963	nA
EQL_{pd}	17.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	t_{PLH}	1.499	1.634	1.806	1.973	2.165
			t_{PHL}	1.079	1.245	1.390	1.524	1.680

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXP 0.5 micron CMOS Pad Library

Description

IDCXx is a family of non-inverting, CMOS-level input buffer pieces.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H
PADM	QC						
L	L						
H	H						

HDL Syntax

Verilog IDCXx *inst_name* (QC, PADM);

VHDL *inst_name*: IDCXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCX3	IDCX6
PADM (pF)	4.90	4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
IDCX3	0.0	15.832	10.4
IDCX6	0.0	18.757	18.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

IDCX3	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: PADM	t _{PLH}	0.883	1.055	1.195	1.305	1.417
To: QC	t _{PHL}	0.654	0.834	0.977	1.080	1.169	
IDCX6	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: PADM	t _{PLH}	0.774	0.825	0.897	0.971	1.060
To: QC	t _{PHL}	0.632	0.710	0.793	0.869	0.951	

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPM 0.5 micron CMOS Pad Library

Description

IDPX3 is a non-inverting, PCI-level input buffer piece. IDPX3 is for the 33MHz PCI ODPSXE16 piece.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H
PADM	QC						
L	L						
H	H						

HDL Syntax

Verilog IDPX3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDPX3 port map (QC, PADM);

Pin Loading

Pin Name	Load
PADM (pF)	IDPX3 4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
IDPX3	0.0	15.774	12.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

IDPX3	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: PADM	t _{PLH}	0.795	0.948	1.106	1.227	1.331
	To: QC	t _{PHL}	0.893	1.068	1.230	1.370	1.517

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPM 0.5 micron CMOS Pad Library

Description

IDQC0 is a non-buffered, resistive crystal oscillator input receiver piece with ESD protection.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QO</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QO	L	L	H	H	<table border="1"> <thead> <tr> <th colspan="2">Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>	Load		PADM	4.90 pF
PADM	QO											
L	L											
H	H											
Load												
PADM	4.90 pF											

HDL Syntax

Verilog IDQC0 *inst_name* (QO, PADM);
 VHDL..... *inst_name*: IDQC0 port map (QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I _{DD} (T _J = 85°C)	4.265	nA
EQL _{pd}	2.1	Eq-load

See page 2-13 for power equation.

Design Notes:

The IDQC0 cell is for backward compatibility with existing oscillator methodologies.

Pad Logic

AMI500HXPM 0.5 micron CMOS Pad Library

Description

IDQC3 is a crystal oscillator input receiver pad piece with a non-inverting, CMOS-level clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

<p>Logic Symbol</p>	<p>The Possible Logic Schematic Combinations</p>													
<p>Truth Table</p> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th>PADM</th> <th>QC</th> <th>QO</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	QO	L	L	L	H	H	H	<p>Pin Loading</p> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	PADM	4.90 pF
PADM	QC	QO												
L	L	L												
H	H	H												
	Load													
PADM	4.90 pF													

Pad Logic

HDL Syntax

Verilog IDQC3 *inst_name* (QC, QO, PADM);
 VHDL..... *inst_name*: IDQC3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ C$)	15.832	nA
EQL_{pd}	11.4	Eq-load

See page 2-13 for power equation.

AMI500HXPM 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	t_{PLH}	0.904	1.070	1.204	1.319	1.447
			t_{PHL}	0.685	0.833	0.965	1.084	1.216
PADM		QO	t_{PLH}	0.000				
			t_{PHL}	0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

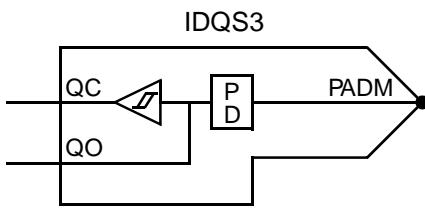
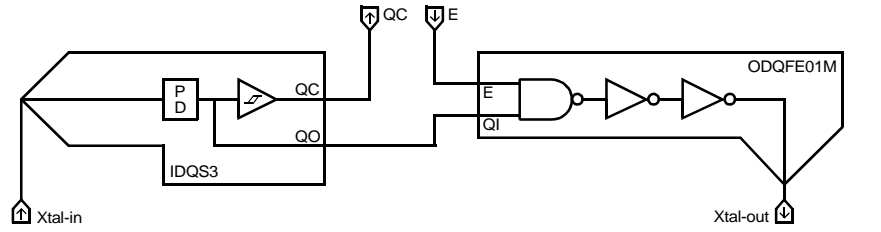
Design Notes:

The IDQC3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

AMI500HXPM 0.5 micron CMOS Pad Library

Description

IDQS3 is a crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS-level schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

Logic Symbol 	Logic Schematic 															
Truth Table <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th>PADM</th> <th>QC</th> <th>QO</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	QO	L	L	L	H	H	H	Pin Loading <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th></th> <th colspan="2">Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90</td> <td>pF</td> </tr> </tbody> </table>		Load		PADM	4.90	pF
PADM	QC	QO														
L	L	L														
H	H	H														
	Load															
PADM	4.90	pF														

HDL Syntax

Verilog IDQS3 *inst_name* (QC, QO, PADM);

VHDL..... *inst_name*: IDQS3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	15.963	nA
EQL_{pd}	18.0	Eq-load

See page 2-13 for power equation.

AMI500HXPM 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	t_{PLH}	1.533	1.648	1.806	1.966	2.154
			t_{PHL}	1.093	1.299	1.451	1.568	1.683
PADM		QO	t_{PLH}	0.000				
			t_{PHL}	0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes:

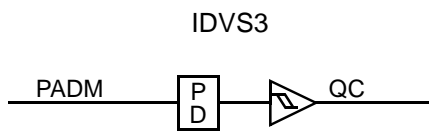
The IDQS3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

3.3

AMI500HXPM 0.5 micron CMOS Pad Library

Description

IDVS3 is a non-inverting, LVTTTL-level Schmitt input buffer piece.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H	<table border="1"> <thead> <tr> <th>PADM(pF)</th> <th>Load</th> </tr> </thead> <tbody> <tr> <td></td> <td>4.90</td> </tr> </tbody> </table>	PADM(pF)	Load		4.90
PADM	QC											
L	L											
H	H											
PADM(pF)	Load											
	4.90											

HDL Syntax

Verilog IDVS3 *inst_name*(QC, PADM);

VHDL *inst_name*: IDVS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	15.750	nA
EQL_{pd}	16.5	eqI

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

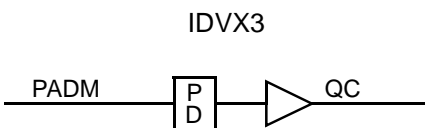
From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	t_{PLH}	1.096	1.281	1.419	1.529	1.641
			t_{PHL}	1.154	1.313	1.526	1.693	1.816

Pad Loading

AMI500HXPM 0.5 micron CMOS Pad Library

Description

IDVX3 is a non-inverting, LVTTTL-level input buffer piece

Logic Symbol	Truth Table	Pin Loading										
 <p style="text-align: center;">IDVX3</p>	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H	<table border="1"> <thead> <tr> <th>PADM(pF)</th> <th>Load</th> </tr> </thead> <tbody> <tr> <td></td> <td>4.90</td> </tr> </tbody> </table>	PADM(pF)	Load		4.90
PADM	QC											
L	L											
H	H											
PADM(pF)	Load											
	4.90											

HDL Syntax

Verilog IDVX3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDVX3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I _{DD} (T _J = 85°C)	15.630	nA
EQL _{pd}	10.4	eql

Propagation Delays

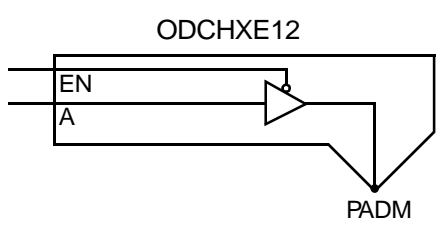
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	t _{PLH}	0.721	0.858	1.011	1.143	1.279
			t _{PHL}	0.651	0.833	0.971	1.078	1.185

Pad Logic

Description

ODCHXE12 is a high performance, 12 mA, non-inverting, CMOS-level, tristate output buffer piece with active low enable.

Logic Symbol	Truth Table	Pin Loading																				
	<table border="1"> <thead> <tr> <th>EN</th> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>Z</td> </tr> </tbody> </table>	EN	A	PADM	L	L	L	L	H	H	H	X	Z	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>3.5 eqI</td> </tr> <tr> <td>EN</td> <td>6.5 eqI</td> </tr> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	A	3.5 eqI	EN	6.5 eqI	PADM	4.90 pF
EN	A	PADM																				
L	L	L																				
L	H	H																				
H	X	Z																				
	Load																					
A	3.5 eqI																					
EN	6.5 eqI																					
PADM	4.90 pF																					

HDL Syntax

Verilog ODCHXE12 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCHXE12 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	59.501	nA
EQL_{pd}	263.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Capacitive Load (pF)				
				15	50	100	200	300 (max)
A		PADM	t_{PLH}	1.648	2.715	4.234	7.290	10.369
			t_{PHL}	1.555	2.355	3.494	5.783	8.089
EN		PADM	t_{HZ}	1.119				
			t_{LZ}	1.245				
			t_{ZH}	1.389	2.437	3.986	7.081	10.105
			t_{ZL}	1.526	2.343	3.501	5.804	8.096

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Pad
Logic

ODCHXX12



AMI500HXPM 0.5 micron CMOS Pad Library

Description

ODCHXX12 is a high performance, 12 mA, non-inverting, TTL-level output buffer piece.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H	<table border="1"> <thead> <tr> <th>A</th> <th>Load</th> </tr> </thead> <tbody> <tr> <td></td> <td>14.5 eqI</td> </tr> </tbody> </table>	A	Load		14.5 eqI
A	PADM											
L	L											
H	H											
A	Load											
	14.5 eqI											

HDL Syntax

Verilog ODCHXX12 *inst_name* (PADM, A);
 VHDL..... *inst_name*: ODCHXX12 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	51.517	nA
EQL_{pd}	216.6	Eq-load

See page 2-13 for power equation.

Output Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

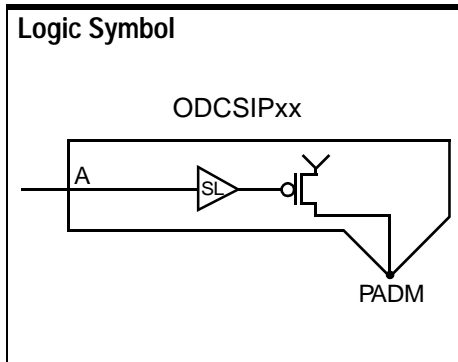
Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	PADM	t_{PLH}	0.954	2.018	3.535	6.591	9.669
		t_{PHL}	1.072	1.863	2.988	5.279	7.606

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Pad Logic

Description

ODCSIPxx is a family of 4 to 12 mA, inverting, CMOS-level output buffer pieces with P-channel open-drains (pull-up) and controlled slew rate outputs.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>Z</td> </tr> </tbody> </table> <p>Z = High Impedance</p>	A	PADM	L	H	H	Z
A	PADM						
L	H						
H	Z						

HDL Syntax

Verilog ODCSIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSIPxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCSIP04	ODCSIP08	ODCSIP12
A (eq-load)	4.1	4.1	4.1
PADM (pF)	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
ODCSIP04	4	56.824	198.7
ODCSIP08	8	56.824	211.8
ODCSIP12	12	56.824	219.2

a. See page 2-13 for power equation.

AMI500HXPM 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

Cell	Capacitive Load (pF)		15	50	100	200	300 (max)
	ODCSIP04	From: A To: PADM	t_{ZH}	3.833	9.167	16.769	31.979
ODCSIP08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZH}	2.510	5.198	9.015	16.743	24.433
ODCSIP12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZH}	2.218	4.390	7.451	13.567	19.728

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

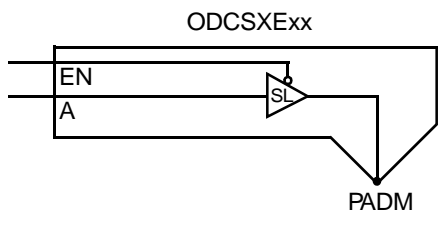
Tristate Timing

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

From	Delay (ns) To	Parameter	Cell		
			ODCSIP04	ODCSIP08	ODCSIP12
A	PADM	t_{HZ}	0.899	1.107	1.226

Description

ODCSXExx is a family of 4 to 12 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol	Truth Table												
	<table border="1"> <thead> <tr> <th>EN</th> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>Z</td> </tr> </tbody> </table>	EN	A	PADM	L	L	L	L	H	H	H	X	Z
EN	A	PADM											
L	L	L											
L	H	H											
H	X	Z											

HDL Syntax

Verilog ODCSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODCSXE04	ODCSXE08	ODCSXE12
A (eq-load)	2.3	2.3	2.3
EN (eq-load)	6.9	6.9	6.9
PADM (pF)	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
ODCSXE04	4	58.395	227.1
ODCSXE08	8	58.395	247.8
ODCSXE12	12	58.395	262.0

a. See page 2-13 for power equation.

AMI500HXPM 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
	ODCSXE04	From: A	t_{PLH}	4.541	9.915	17.616	32.583
To: PADM		t_{PHL}	4.178	8.978	15.756	29.374	43.118
From: EN		t_{ZH}	3.991	9.466	17.172	32.072	46.531
	To: PADM	t_{ZL}	3.890	8.649	15.503	29.198	42.818
ODCSXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	t_{PLH}	2.870	5.547	9.427	17.170	24.828
	To: PADM	t_{PHL}	2.997	5.405	8.852	15.769	22.705
	From: EN	t_{ZH}	2.810	5.512	9.383	17.099	24.783
	To: PADM	t_{ZL}	2.687	5.151	8.634	15.552	22.500
ODCSXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	t_{PLH}	2.987	5.147	8.208	14.337	20.488
	To: PADM	t_{PHL}	2.640	4.287	6.577	11.150	15.778
	From: EN	t_{ZH}	2.626	4.787	7.854	13.985	20.128
	To: PADM	t_{ZL}	2.354	4.012	6.301	10.869	15.510

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

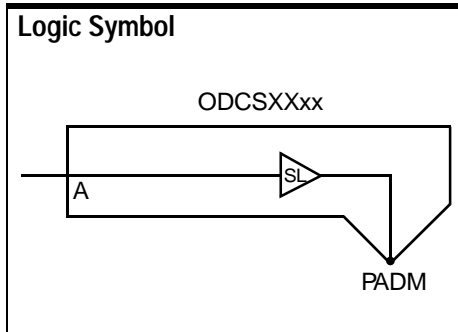
Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

From	Delay (ns) To	Parameter	Cell		
			ODCSXE04	ODCSXE08	ODCSXE12
EN	PADM	t_{HZ}	0.957	1.166	1.284
		t_{LZ}	1.176	1.332	1.465

AMI500HXPM 0.5 micron CMOS Pad Library

Description

ODCSXXxx is a family of 4 to 12 mA, non-inverting, CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H
A	PADM						
L	L						
H	H						

HDL Syntax

Verilog ODCSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCSXX04	ODCSXX08	ODCSXX12
A (eq-load)	9.3	9.3	9.3

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
ODCSXX04	4	54.738	206.8
ODCSXX08	8	54.738	227.5
ODCSXX12	12	54.738	241.7

a. See page 2-13 for power equation.

AMI500HXP 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

ODCSXX04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	t_{PLH}	3.265	8.669	16.296	31.000	45.222
To: PADM	t_{PHL}	3.164	7.909	14.798	28.504	42.071	
ODCSXX08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	t_{PLH}	2.116	4.746	8.610	16.334	23.985
To: PADM	t_{PHL}	2.083	4.439	7.906	14.879	21.763	
ODCSXX12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	t_{PLH}	1.911	4.029	7.069	13.194	19.359
To: PADM	t_{PHL}	1.709	3.296	5.623	10.242	14.786	

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPM 0.5 micron CMOS Pad Library

Description

ODCXIPxx is a family of 1 to 12 mA, inverting, CMOS-level, output buffer pieces with P-channel, open-drains (pull-up).

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>Z</td> </tr> </tbody> </table> <p>Z = High Impedance</p>	A	PADM	L	H	H	Z
A	PADM						
L	H						
H	Z						

HDL Syntax

Verilog ODCXIPxx *inst_name* (PADM, A);
 VHDL *inst_name*: ODCXIPxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12
A (eq-load)	2.8	2.8	2.8	3.9	3.9
PADM (pF)	4.90	4.90	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics ^a	
		Static IDD (T _J = 85°C) (nA)	EQLpd (Eq-load)
ODCXIP01	1	46.245	158.6
ODCXIP02	2	46.764	163.4
ODCXIP04	4	47.309	172.7
ODCXIP08	8	48.374	188.7
ODCXIP12	12	49.438	198.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXIP01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A	To: PADM	t _{ZH}	6.676	9.841	12.971	17.584

Pad Logic

AMI500HXPM 0.5 micron CMOS Pad Library

ODCXIP02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	t_{ZH}	3.684	8.992	12.789	16.590	24.205
ODCXIP04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZH}	2.426	5.089	8.873	16.445	24.040
ODCXIP08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZH}	1.700	3.077	5.021	8.875	12.703
ODCXIP12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZH}	1.626	2.770	4.315	7.366	12.703

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

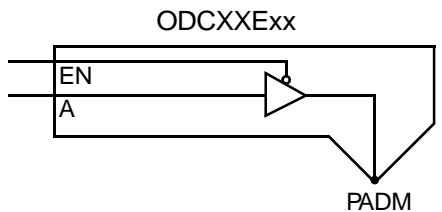
Tristate Timing

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

From	Delay (ns) To	Parameter	Cell				
			ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12
APADM		t_{HZ}	1.125	0.999	1.198	1.410	1.420

Description

ODCXEXx is a family of 1 to 12 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol	Truth Table												
	<table border="1"> <thead> <tr> <th>EN</th> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>Z</td> </tr> </tbody> </table>	EN	A	PADM	L	L	L	L	H	H	H	X	Z
EN	A	PADM											
L	L	L											
L	H	H											
H	X	Z											

HDL Syntax

Verilog ODCXEXx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXEXx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODCXEX01	ODCXEX02	ODCXEX04	ODCXEX08	ODCXEX12
A (eq-load)	5.6	7.9	7.9	2.3	2.3
EN (eq-load)	4.0	5.3	5.3	5.5	5.5
PADM (pF)	4.90	4.90	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
ODCXEX01	1	47.619	164.6
ODCXEX02	2	49.110	174.0
ODCXEX04	4	49.110	185.5
ODCXEX08	8	55.615	232.0
ODCXEX12	12	55.615	246.7

a. See page 2-13 for power equation.

AMI500HXP 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
	ODCXE01	From: A	t_{PLH}	6.577	9.663	12.752	17.366
To: PADM		t_{PHL}	6.416	9.178	11.922	16.004	22.847
From: EN		t_{ZH}	6.795	9.880	12.963	17.578	25.240
	To: PADM	t_{ZL}	6.366	9.202	11.918	15.946	22.855
ODCXE02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A	t_{PLH}	3.512	8.880	12.693	16.496	24.080
	To: PADM	t_{PHL}	3.377	8.217	11.666	15.086	21.848
	From: EN	t_{ZH}	3.689	9.158	12.993	16.790	24.305
	To: PADM	t_{ZL}	3.615	8.288	11.722	15.153	21.955
ODCXE04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	t_{PLH}	2.466	5.059	8.797	16.425	23.969
	To: PADM	t_{PHL}	2.415	4.824	8.221	15.040	21.900
	From: EN	t_{ZH}	2.434	5.105	8.901	16.481	24.062
	To: PADM	t_{ZL}	2.401	4.791	8.248	15.130	21.902
ODCXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	t_{PLH}	2.493	3.871	5.795	9.636	13.493
	To: PADM	t_{PHL}	2.118	3.334	5.071	8.542	12.011
	From: EN	t_{ZH}	2.133	3.503	5.414	9.250	13.121
	To: PADM	t_{ZL}	1.904	3.128	4.864	8.331	11.799
ODCXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	t_{PLH}	2.459	3.604	5.146	8.192	11.278
	To: PADM	t_{PHL}	1.929	2.779	3.953	6.260	8.542
	From: EN	t_{ZH}	2.165	3.260	4.729	7.759	10.916
	To: PADM	t_{ZL}	1.782	2.655	3.836	6.142	8.435

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

Delay (ns)		Parameter	Cell				
From	To		ODCXE01	ODCXE02	ODCXE04	ODCXE08	ODCXE12
EN	PADM	t_{HZ}	1.630	1.378	1.852	1.256	1.419
		t_{LZ}	0.514	0.457	0.612	1.262	1.460

AMI500HXPM 0.5 micron CMOS Pad Library

Description

ODCXXXxx is a family of 1 to 12 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H
A	PADM						
L	L						
H	H						

HDL Syntax

Verilog ODCXXXxx inst_name (PADM, A);

VHDL inst_name: ODCXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCXXX01	ODCXXX02	ODCXXX04	ODCXXX08	ODCXXX12
A (eq-load)	4.3	4.3	6.2	8.3	8.2

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
ODCXXX01	1	46.179	159.3
ODCXXX02	2	46.179	164.8
ODCXXX04	4	47.216	176.3
ODCXXX08	8	48.303	198.8
ODCXXX12	12	48.303	213.5

a. See page 2-13 for power equation.

AMI500HXPM 0.5 micron CMOS Pad Library

Propagation Delays (ns)

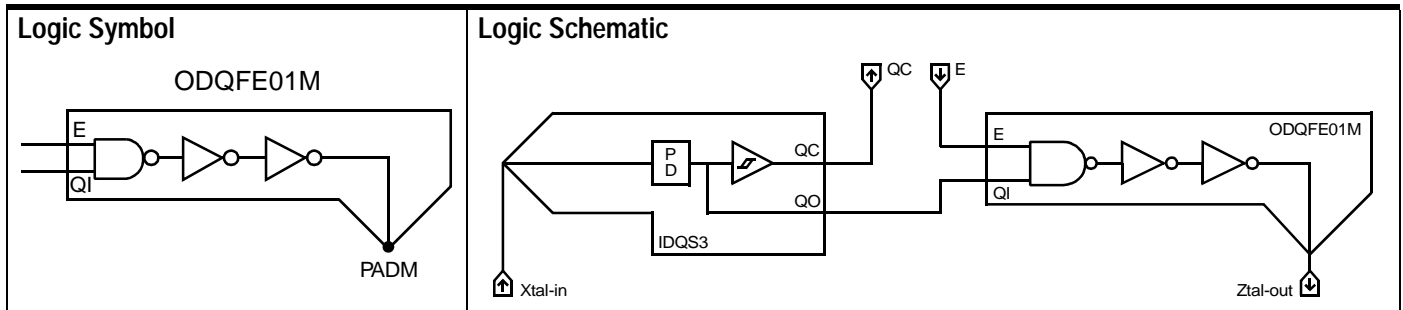
Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

ODCXXXxx	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A	t_{PLH}	6.354	9.415	12.470	17.059	24.747
To: PADM	t_{PHL}	5.866	8.738	11.544	15.647	22.285	
ODCXXX02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A	t_{PLH}	3.605	8.894	12.704	16.516	24.114
To: PADM	t_{PHL}	3.268	8.023	11.425	14.840	21.701	
ODCXXX04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	t_{PLH}	2.069	4.720	8.531	16.129	23.682
To: PADM	t_{PHL}	2.090	4.463	7.905	14.753	21.525	
ODCXXX08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	t_{PLH}	1.280	2.880	4.868	8.645	12.548
To: PADM	t_{PHL}	1.514	2.751	4.515	8.003	11.434	
ODCXXX12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	t_{PLH}	1.547	2.592	4.071	7.056	10.066
To: PADM	t_{PHL}	1.445	2.273	3.345	5.453	7.572	

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODQFE01M is a fundamental mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 32 kHz - 1 MHz. QI is the input from IDQCS3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.



<p>Truth Table</p> <table border="1"> <thead> <tr> <th>PADM</th> <th>E</th> <th>QI</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>X</td> </tr> </tbody> </table>	PADM	E	QI	L	H	H	H	H	L	H	L	X	<p>Pin Loading</p> <table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>E</td> <td>4.0 eql</td> </tr> <tr> <td>QI</td> <td>3.2 eql</td> </tr> </tbody> </table>		Load	E	4.0 eql	QI	3.2 eql
PADM	E	QI																	
L	H	H																	
H	H	L																	
H	L	X																	
	Load																		
E	4.0 eql																		
QI	3.2 eql																		

HDL Syntax

Verilog ODQFE01M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE01M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	47.039	nA
EQL_{pd}	161.5	Eq-load

See page 2-13 for power equation.

Pad
Logic

ODQFE01M



AMI500HXPM 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Capacitive Load (pF)				
				15	25	35	50	75 (max)
E		PADM	t_{PLH}	6.965	10.095	13.178	17.745	25.248
			t_{PHL}	7.304	10.028	12.752	16.847	23.697
QI		PADM	t_{PLH}	7.002	10.066	13.130	17.726	25.398
			t_{PHL}	7.549	10.288	13.027	17.129	23.947

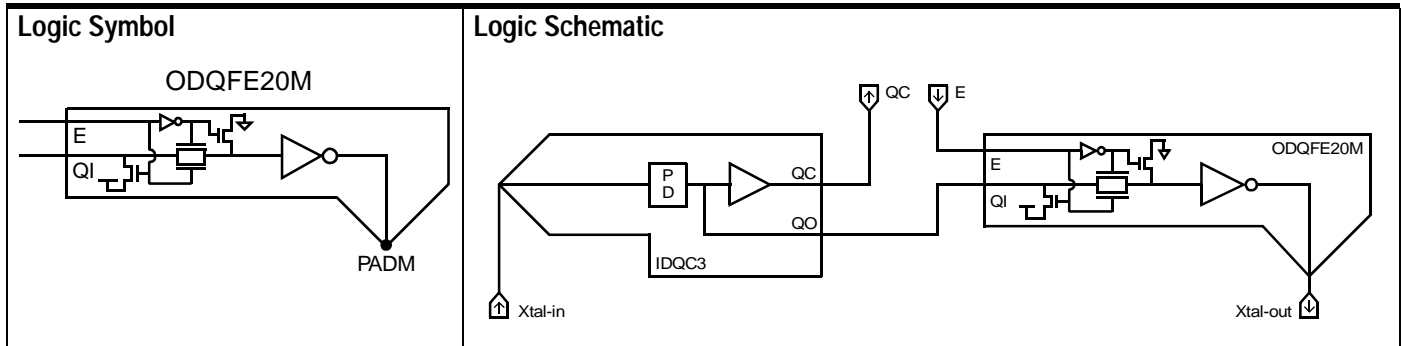
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes:

The ODQFE01M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQS3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

Description

ODQFE20M is a fundamental mode, enabled crystal oscillator, output buffer pad piece that runs over a frequency range of 1 MHz - 20 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to the Xtal-out.



Truth Table			Pin Loading	
PADM	E	QI		Load
H	L	X	E	6.5 eqI
H	H	L	QI	5.5 eqI
L	H	H		

HDL Syntax

Verilog ODQFE20M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE20M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I _{DD} (T _J = 85°C)	46.401	nA
EQL _{pd}	175.2	Eq-load

See page 2-13 for power equation.

Pad
Logic

ODQFE20M



AMI500HXPM 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Capacitive Load (pF)				
				15	50	75	100	150 (max)
E		PADM	t_{PLH}	4.655	10.034	13.867	17.675	25.222
			t_{PHL}	3.246	8.030	11.452	14.871	21.692
QI		PADM	t_{PLH}	3.328	8.644	12.442	16.241	23.840
			t_{PHL}	3.165	8.082	11.480	14.856	21.725

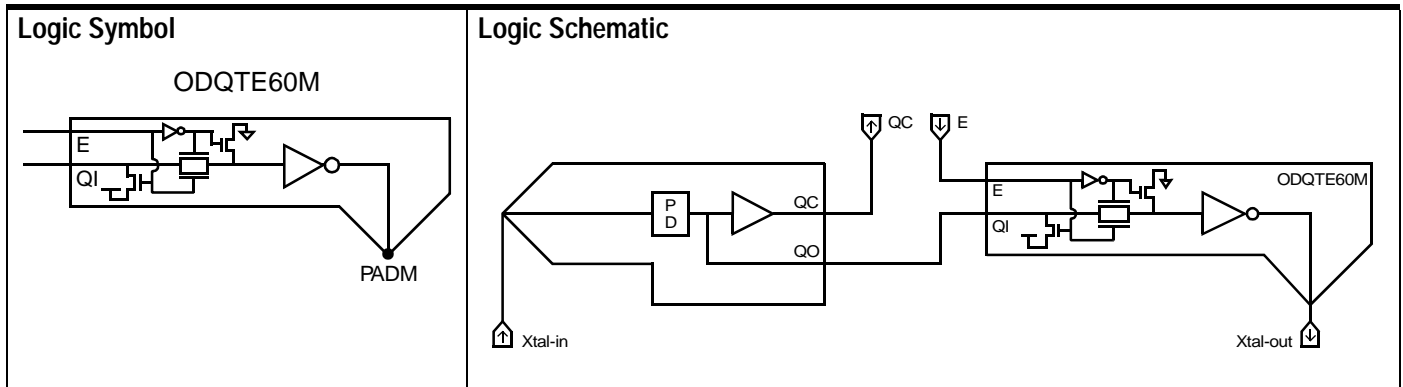
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes:

The ODQFE20M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

Description

ODQTE60M is an enabled crystal oscillator, output driver pad piece that runs over a frequency range of 20 - 60 MHz. QI is the input from the IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.



Truth Table			Pin Loading	
PADM	E	QI		Load
H	L	X	E	6.5 eqL
H	H	L	QI	5.5 eqL
L	H	H		

HDL Syntax

Verilog ODQTE60M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQTE60M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I _{DD} (T _J = 85°C)	46.401	nA
EQL _{pd}	186.8	Eq-load

See page 2-13 for power equation.

Pad
Logic

AMI500HXPM 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Capacitive Load (pF)				
				15	50	100	200	300 (max)
E		PADM	t_{PLH}	3.677	6.364	10.165	17.744	25.321
			t_{PHL}	2.101	4.494	7.907	14.734	21.568
QI		PADM	t_{PLH}	2.022	4.722	8.536	16.100	23.615
			t_{PHL}	2.178	4.568	7.967	14.802	21.609

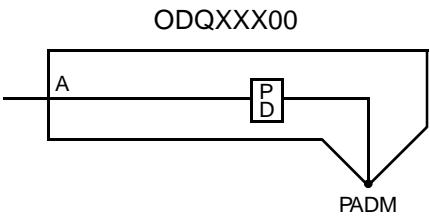
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes:

The ODQTE60M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

Description

ODQXXX00 is a non-buffered, resistive analog crystal oscillator output pad piece with ESD protection.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H	<table border="1"> <thead> <tr> <th>A</th> <th>Load</th> </tr> </thead> <tbody> <tr> <td></td> <td>2.4 eqI</td> </tr> </tbody> </table>	A	Load		2.4 eqI
A	PADM											
L	L											
H	H											
A	Load											
	2.4 eqI											

HDL Syntax

Verilog ODQXXX00 *inst_name* (PADM, A);
 VHDL..... *inst_name*: ODQXXX00 port map (PADM, A);

Power Characteristics

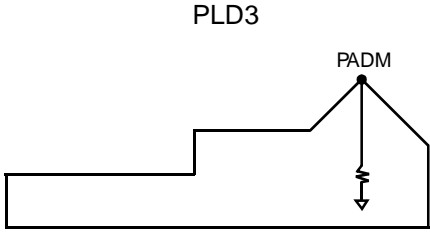
Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	45.048	nA
EQL_{pd}	148.8	Eq-load

See page 2-13 for power equation.

AMI500HXPM 0.5 micron CMOS Pad Library

Description

PLD3 is an active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
	N/A	N/A

Pad Logic

HDL Syntax

Verilog PLD3 *inst_name* (PADM);
 VHDL..... *inst_name*: PLD3 port map (PADM);

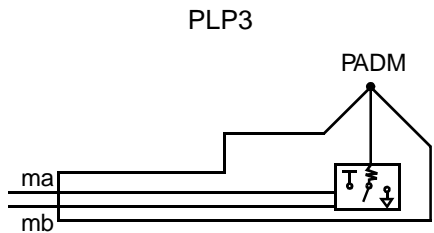
Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	13.883	nA
EQL_{pd}	149.6	Eq-load

See page 2-13 for power equation.

Description

PLP3 is a programmable pull-up/pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading																					
	<table border="1"> <thead> <tr> <th>MA</th> <th>MB</th> <th>PADM Function</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>Pull-down</td> </tr> <tr> <td>H</td> <td>H</td> <td>Pull-up</td> </tr> <tr> <td>H</td> <td>L</td> <td>Tristate</td> </tr> <tr> <td>L</td> <td>H</td> <td>Tristate</td> </tr> </tbody> </table>	MA	MB	PADM Function	L	L	Pull-down	H	H	Pull-up	H	L	Tristate	L	H	Tristate	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>MA</td> <td>2.1 eqI</td> </tr> <tr> <td>MB</td> <td>1.8 eqI</td> </tr> </tbody> </table>		Load	MA	2.1 eqI	MB	1.8 eqI
MA	MB	PADM Function																					
L	L	Pull-down																					
H	H	Pull-up																					
H	L	Tristate																					
L	H	Tristate																					
	Load																						
MA	2.1 eqI																						
MB	1.8 eqI																						

HDL Syntax

Verilog PLP3 *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLP3 port map (PADM, MA, MB);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	13.883	nA
EQL_{pd}	146.6	Eq-load

See page 2-13 for power equation.

PLU3

AMI500HXPM 0.5 micron CMOS Pad Library

Description

PLU3 is an active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
<p>The logic symbol for PLU3 is a buffer with a pull-up resistor. The input is on the left, and the output is on the right. A pull-up resistor is connected to the output node, labeled PADM. The resistor is connected to a supply voltage source (VDD).</p>	<p>N/A</p>	<p>N/A</p>

HDL Syntax

Verilog PLU3 *inst_name* (PADM);
 VHDL..... *inst_name*: PLU3 port map (PADM);

Power Characteristics

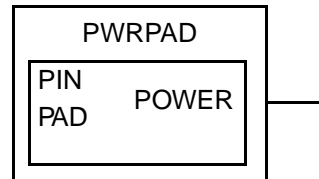
Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	13.892	nA
EQL_{pd}	149.5	Eq-load

See page 2-13 for power equation.
 Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Pad Logic

Description

PWRPAD is a generic power pad used to define the connection of a chip power pin to logical buses in the device. For more information on power and ground buses, as well as PWRPAD usage see "Interconnect Load Estimation" on page 2-15.



PWRPAD has the following parameters:

- LVDD: this parameter receives a string value that defines the name of the power supply that PWRPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that PWRPAD connects to.

Verilog Syntax

```
defparam SUPPLY_5V.LVDD = "PAD_5V",
        SUPPLY_5V.CONTACT = "IPWR,OPWR1";
PWRPAD SUPPLY_5V (.PADM(VDD_5V));
```

VHDL syntax

```
SUPPLY_5V : PWRPAD generic map (LVDD => "PAD_5V", CONTACT => "IPWR,OPWR1")
port map (PADM => VDD_5V);
```

Bolt syntax

```
PWRPAD/SUPPLY_5V VDD_5V (LVDD='PAD_5V' CONTACT="IPWR,OPWR1");
```

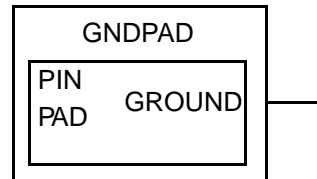
where:

- SUPPLY_5V is the instance name for PWRPAD
- PAD_5V is the name of the supply
- IPWR, OPWR1 are logical buses (see section ...)
- VDD_5V is the chip port name

AMI500HXP 0.5 micron CMOS Pad Library

Description

GNDPAD is a generic ground pad used to define the connection of a chip ground pin to logical buses in the device. For more information on power and ground buses, as well as GNDPAD usage see "Interconnect Load Estimation" on page 2-15.



GNDPAD has the following parameters:

- LVSS: this parameter receives a string value that defines the name of the ground that GNDPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that GNDPAD connects to.

Verilog syntax

```
defparam GROUND1.LVSS = "VSS",  
         GROUND1.CONTACT = "CGND,OGND";  
GNDPAD GROUND1 (.PADM(VSS1));
```

VHDL syntax

```
GROUND1 : GNDPAD generic map (LVSS => "VSS", CONTACT => "CGND,OGND")  
port map (PADM => VSS1);
```

Bolt syntax

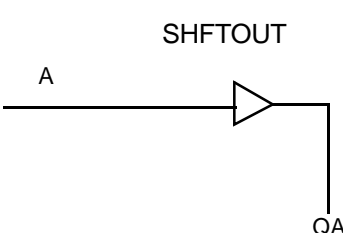
```
.GNDPAD/GROUND1 VSS1 (LVSS='VSS' CONTACT="CGND,OGND");
```

where:

- GROUND1 is the instance name for GNDPAD
- VSS is the name of the supply
- CGND,OGND are logical buses (see section ...)
- VSS1 is the chip port name

Description

SHFTOUT is a mixed voltage single output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>A</th> <th>QA</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	QA	L	L	H	H	<table border="1"> <thead> <tr> <th>A</th> <th>Load</th> </tr> </thead> <tbody> <tr> <td></td> <td>4.1</td> </tr> </tbody> </table>	A	Load		4.1
A	QA											
L	L											
H	H											
A	Load											
	4.1											

HDL Syntax

Verilog SHFTOUT *inst_name* (QA, A);

VHDL..... *inst_name*: SHFTOUT port map (QA, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	12.309	nA
EQL_{pd}	8.3	eql

Propagation Delays

*See note at beginning of section to compute total delay.

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 2.5\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	3	6	10	13 (max)
A		QA	t_{PLH}	0.28	0.33	0.40	0.48	0.54
			t_{PHL}	0.21	0.23	0.27	0.31	0.34

Pad
Logic

SHFTOUTT

AMI500HXP 0.5 micron CMOS Pad Library

Description

SHFTOUTT is a mixed voltage dual output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol	Truth Table	Pin Loading																										
	<table border="1"> <thead> <tr> <th>A</th> <th>EN</th> <th>QA</th> <th>QEN</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>X</td> <td>L</td> <td>X</td> </tr> <tr> <td>H</td> <td>X</td> <td>H</td> <td>X</td> </tr> <tr> <td>X</td> <td>L</td> <td>X</td> <td>L</td> </tr> <tr> <td>X</td> <td>H</td> <td>X</td> <td>H</td> </tr> </tbody> </table>	A	EN	QA	QEN	L	X	L	X	H	X	H	X	X	L	X	L	X	H	X	H	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>A(eql)</td> <td>3.0</td> </tr> <tr> <td>EN(eql)</td> <td>3.2</td> </tr> </tbody> </table>		Load	A(eql)	3.0	EN(eql)	3.2
A	EN	QA	QEN																									
L	X	L	X																									
H	X	H	X																									
X	L	X	L																									
X	H	X	H																									
	Load																											
A(eql)	3.0																											
EN(eql)	3.2																											

HDL Syntax

Verilog SHFTOUTT *inst_name* (QA, QEN, A, EN);

VHDL..... *inst_name*: SHFTOUTT port map (QA, QEN, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	13.217	nA
EQL_{pd}	10.6	eql

Propagation Delays

*See note at beginning of section to compute total delay.

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 2.5\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	2	4	6	8 (max)
A		QA	t_{PLH}	0.34	0.38	0.46	0.54	0.63
			t_{PHL}	0.24	0.26	0.31	0.35	0.40
EN		QEN	t_{PLH}	0.35	0.39	0.48	0.56	0.65
			t_{PHL}	0.24	0.27	0.32	0.36	0.40

Pad Logic