1 Introduction

The C504 is a modified and extended version of the C503 Microcontroller. Its enhanced functionality, especially the capture compare unit (CCU), allows to use the MCU in motor control applications. Further, the C504 is compatible with the SAB 80C52/C501 microcontrollers and can replace it in existing applications.

The C504-2R contains a non-volatile 16K×8 read-only program memory, a volatile on-chip 512×8 read/write data memory, four 8-bit wide ports, three 16-bit timers/counters, a 16-bit capture/ compare unit, a 10-bit compare timer, a twelve source, two priority level interrupt structure, a serial port, versatile fail save mechanisms, on-chip emulation support logic, and a genuine 10-bit A/D converter. The C504-L is identical to the C504-2R, except that it lacks the on-chip program memory. Therefore, the term C504 refers to all versions within this documentation unless otherwise noted.

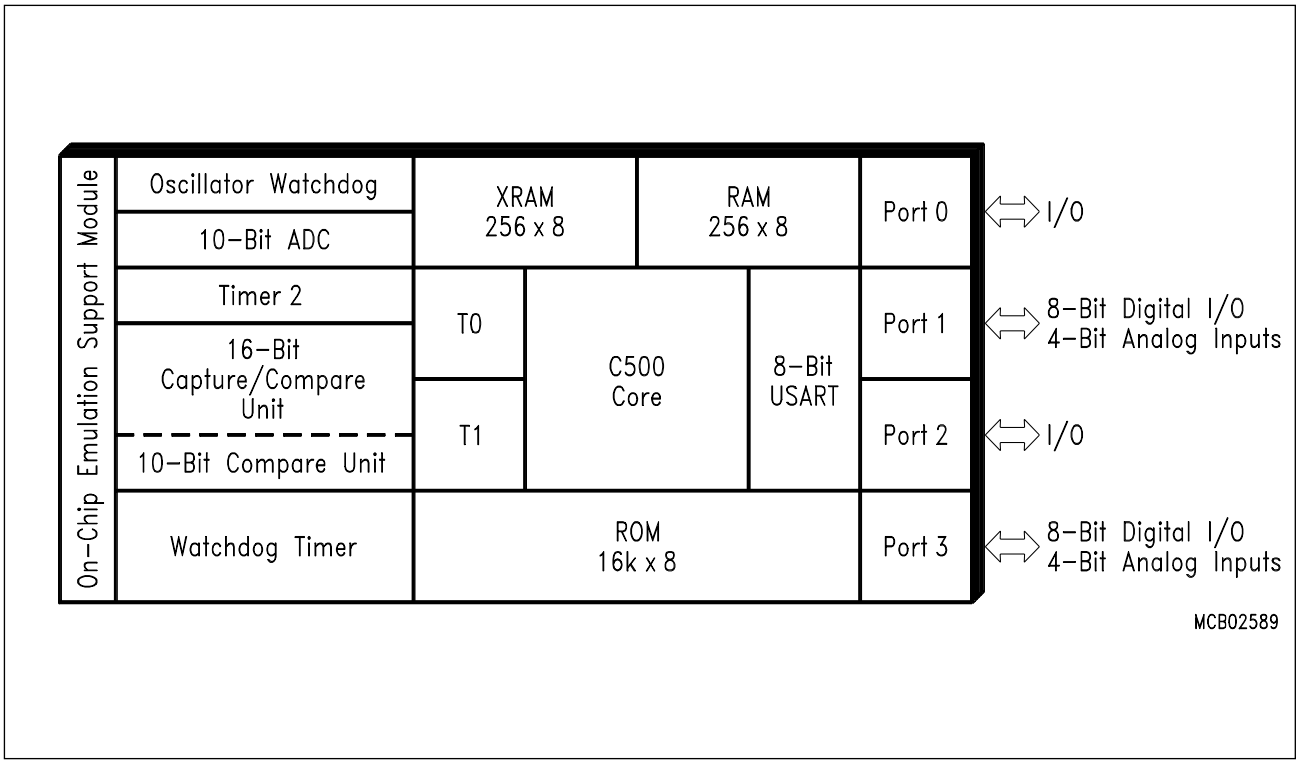

Figure 1-1
C504 Functional Units

Listed below is a summary of the main features of the C504:

- Fully compatible to standard 8051 microcontroller
- Up to 40 MHz external operating frequency
- 16 K×8 ROM (C504-2R only)
- 256×8 RAM
- 256×8 XRAM
- Four 8-bit ports, (2 ports with mixed analog/digital I/O capability)
- Three 16-bit timers/counters (timer 2 with up/down counter feature)
- Capture/compare unit for PWM signal generation and signal capturing
  - 3-channel, 16-bit capture/compare unit
  - 1-channel, 10-bit compare unit
- USART
- 10-bit A/D Converter with 8 multiplexed inputs
- Twelve interrupt sources with two priority levels
- On-chip emulation support logic (Enhanced Hooks Technology ™)
- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast Power On Reset
- Power Saving Modes
- M-QFP-44 package
- Temperature ranges:
  - SAB-C504 T_A : 0 to 70°C
  - SAF-C504 T_A : – 40 to 85°C
  - SAH-C504 T_A : – 40 to 110°C (max. operating frequency.: TBD)
  - SAK-C504 T_A : – 40 to 125°C (max. operating frequency.: 12 MHz)

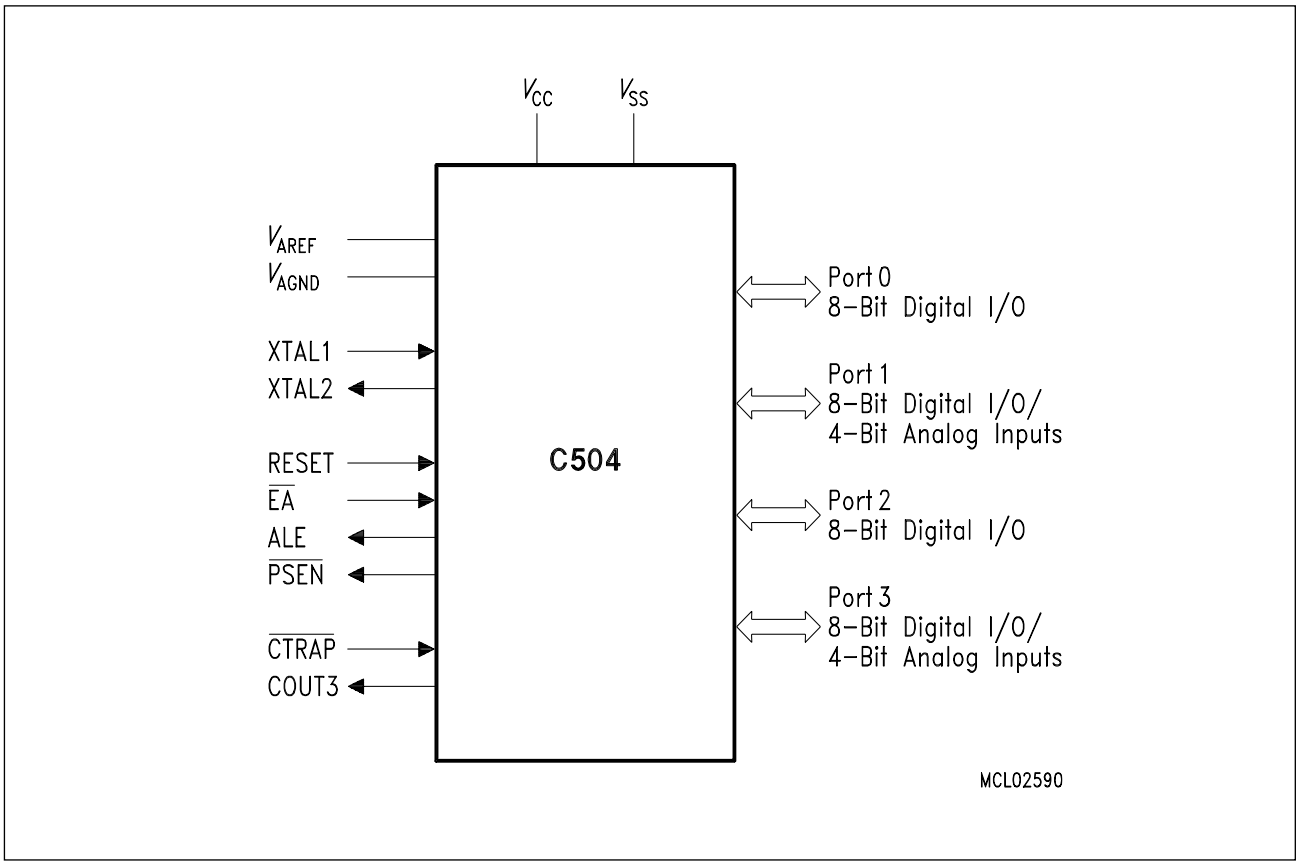

Figure 1-2
Logic Symbol

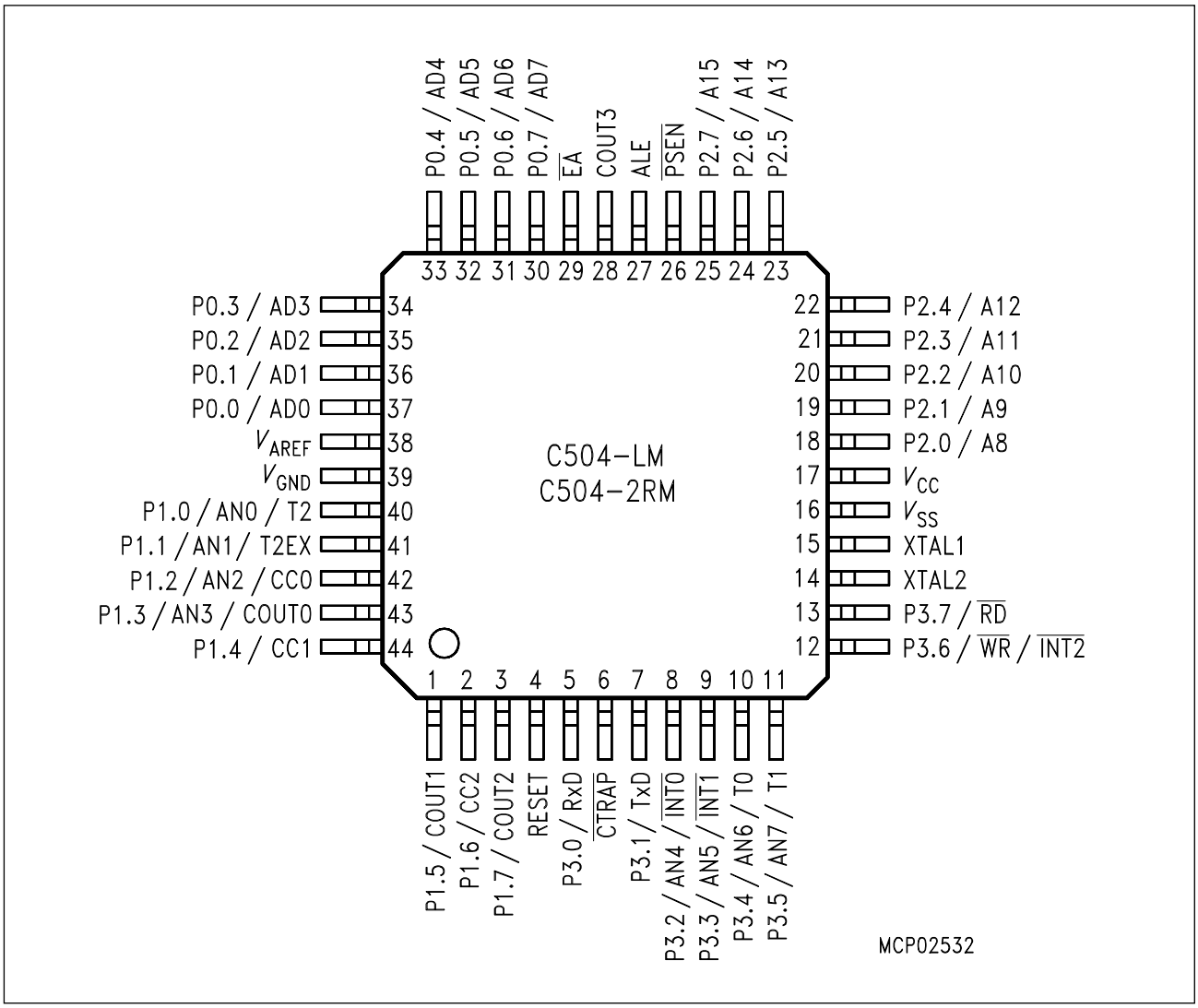

Figure 1-3
Pin Configuration (top view)

Table 1-1
Pin Definitions and Functions

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
P1.0-P1.7	40-44, 1-3	I/O	**Port 1** is an 8-bit bidirectional port. Port pins can be used for digital input/output. P1.0 - P1.3 can also be used as analog inputs of the A/D-converter. As secondary digital functions, port 1 contains the timer 2 pins and the capture/compare inputs/outputs. Port 1 pins are assigned to be used as analog inputs via the register P1ANA. The functions are assigned to the pins of port 1 as follows:
	40		P1.0 / AN0 / T2 — Analog input channel 0 / input to counter 2
	41		P1.1 / AN1 / T2EX — Analog input channel 1 / capture/reload trigger of timer 2 / up-down count
	42		P1.2 / AN2 / CC0 — Analog input channel 2 / input/output of capture/compare channel 0
	43		P1.3 / AN3 / COUT0 — Analog input channel 3 / output of capture/compare channel 0
	44		P1.4 / CC1 — Input/output of capture/compare channel 1
	1		P1.5 / COUT1 — Output of capture/compare channel 1
	2		P1.6 / CC2 — Input/output of capture/compare channel 2
	3		P1.7 / COUT2 — Output of capture/compare channel 2
RESET	4	I	**RESET** A high level on this pin for one machine cycle while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.

*) I = Input
O = Output

Table 1-1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
P3.0-P3.7	5, 7-13	I/O	**Port 3** is an 8-bit bidirectional port. P3.0 (R×D) and P3.1 (T×D) operate as defined for the C501. P3.2 to P3.7 contain the external interrupt inputs, timer inputs, input and as an additional optinal function four of the analog inputs of the A/D-converter. Port 3 pins are assigned to be used as analog inputs by the bits of SFR P3ANA. P3.6/$\overline{WR}$ can be assigned as a third interrupt input. The functions are assigned to the pins of port 3 as follows:
	5		P3.0 / RxD — Receiver data input (asynch.) or data input/output (synch.) of serial interface
	7		P3.1 / TxD — Transmitter data output (asynch.) or clock output (synch.) of serial interface
	8		P3.2 / AN4 / $\overline{INT0}$ — Analog input channel 4 / external interrupt 0 input / timer 0 gate control input
	9		P3.3 / AN5 / $\overline{INT1}$ — Analog input channel 5 / external interrupt 1 input / timer 1 gate control input
	10		P3.4 / AN6 / T0 — Analog input channel 6 / timer 0 counter input
	11		P3.5 / AN7 / T1 — Analog input channel 7 / timer 1 counter input
	12		P3.6 / $\overline{WR}$ / $\overline{INT2}$ — $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory / external interrupt 2 input
	13		P3.7 / $\overline{RD}$ — $\overline{RD}$ control output; enables the external data memory
$\overline{CTRAP}$	6	I	**CCU Trap Input** With $\overline{CTRAP}$ = low the compare outputs of the CAPCOM unit are switched to the logic level as defined in the COINI register (if they are enabled by the bits in SFR TRCON). $\overline{CTRAP}$ is an input pin with an internal pullup resistor. For power saving reasons, the signal source which drives the $\overline{CTRAP}$ input should be at high or floating level during power-down mode.

*) I = Input
O = Output

Table 1-1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
XTAL2	14	–	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	15	–	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
P2.0-P2.7	18-25	I/O	**Port 2** is a bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	26	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
ALE	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access. When instructions are executed from internal ROM ($\overline{\text{EA}}$=1) the ALE generation can be disabled by bit EALE in SFR SYSCON.

*) I = Input
O = Output

Table 1-1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
COUT3	28	O	**10-Bit compare channel output** This pin is used for the output signal of the 10-bit compare timer 2 unit. COUT3 can be disabled and set to a high or low state.
$\overline{EA}$	29	I	**$\overline{External\ Access}$ Enable** When held at high level, instructions are fetched from the internal ROM (C504-2R only) when the PC is less than 4000_H.When held at low level, the C504 fetches all instructions from external program memory. For the C504-L this pin must be tied low.
P0.0-P0.7	30-37	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impendance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup resistors when issuing 1 s. Port 0 also outputs the code bytes during program verification in the C504-2R. External pullup resistors are required during program (ROM) verification.
V_{AREF}	38	–	**Reference voltage** for the A/D converter.
V_{AGND}	39	–	**Reference ground** for the A/D converter.
V_{SS}	16	–	**Ground** (0V)
V_{CC}	17	–	**Power Supply** (+5V)

*) I = Input
O = Output

2 Fundamental Structure

The C504 basically is fully compatible to the architecture of the standard 8051 microcontroller family. Especially it is functionally upward compatible with the SAB 80C52/C501 microcontrollers. While maintaining all architectural and operational characteristics of the SAB 80C52/C501, the C504 incorporates a genuine 10-bit A/D Converter, a capture/compare unit, a XRAM data memory as well as some enhancements in the Timer 2 and Fail Save Mechanism Unit. **Figure 2-1** shows a block diagram of the C504.

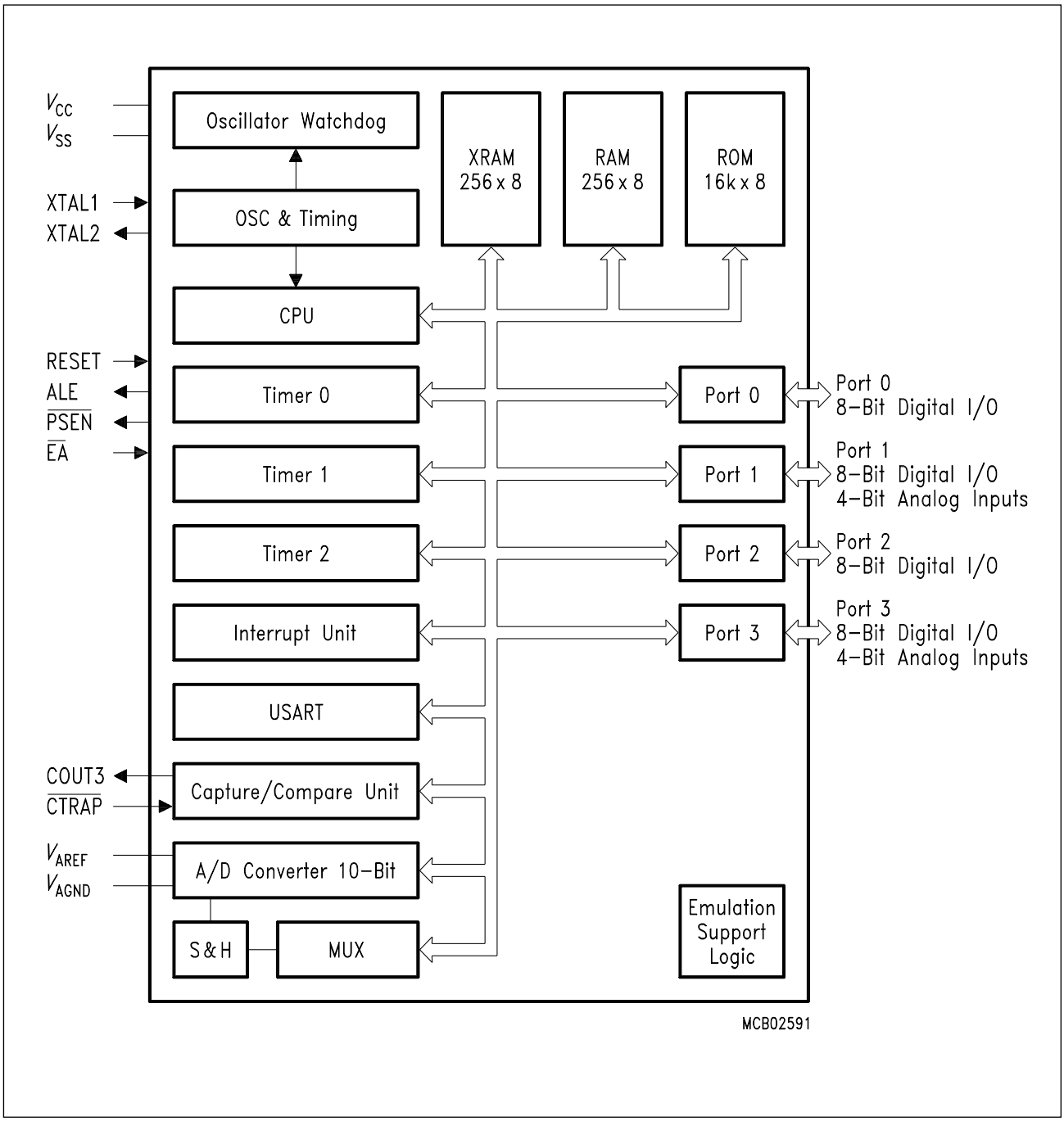

Figure 2-1
Block Diagram of the C504

2.1 CPU

The C504 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12-MHz crystal, 58% of the instructions execute in 1.0 µs (40 MHz: 300 ns).
The CPU (Central Processing Unit) of the C504 consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.
The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), an A register, B register and PSW register.
The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, substract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)).
Also included is a Boolean processor performing the bit operations as set, clear, completement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (or its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.
The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

Accumulator

ACC is the symbol for the accumulator register. The mnemonics for accumulator-specific instructions, however, refer to the accumulator simply as A.

Program Status Word

The Program Status Word (PSW) contains several status bits that reflect the current state of the CPU.

Special Function Register PSW (Address $D0_H$) **Reset Value : 00_H**

Bit No.	MSB							LSB	
	$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag Used by arithmetic instruction.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

OV	Overflow Flag Used by arithmetic instruction.
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

B Register

The B register is used during multiply and divide and serves as both source and destination. For other instructions it can be treated as another scratch pad register.

Stack Pointer

The stack pointer (SP) register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions and decremented after data is popped during a POP and RET (RETI) execution, i.e. it always points to the last valid stack byte. While the stack may reside anywhere in the on-chip RAM, the stack pointer is initialized to 07_H after a reset. This causes the stack to begin a location = 08_H above register bank zero. The SP can be read or written under software control.

2.2 CPU Timing

A machine cycle consists of 6 states (12 oscillator periods). Each state is divided into a phase 1 half, during which the phase 1 clock is active, and a phase 2 half, during which the phase 2 clock is active. Thus, a machine cycle consists of 12 oscillator periods, numbered S1P1 (state 1, phase 1) through S6P2 (state 6, phase 2). Each state lasts for two oscillator periods. Typically, arithmetic and logically operations take place during phase 1 and internal register-to-register transfers take place during phase 2.

The diagrams in **figure 2-2** show the fetch/execute timing related to the internal states and phases. Since these internal clock signals are not user-accessible, the XTAL2 oscillator signals and the ALE (address latch enable) signal are shown for external reference. ALE is normally activated twice during each machine cycle: once during S1P2 and S2P1, and again during S4P2 and S5P1.

Executing of a one-cycle instruction begins at S1P2, when the op-code is latched into the instruction register. If it is a two-byte instruction, the second reading takes place during S4 of the same machine cycle. If it is a one-byte instruction, there is still a fetch at S4, but the byte read (which would be the next op-code) is ignored (discarded fetch), and the program counter is not incremented. In any case, execution is completed at the end of S6P2.

Figures 2-2 (a) and **(b)** show the timing of a 1-byte, 1-cycle instruction and for a 2-byte, 1-cycle instruction.

Most C504 instructions are executed in one cycle. MUL (multiply) and DIV (divide) are the only instructions that take more than two cycles to complete; they take four cycles. Normally two code bytes are fetched from the program memory during every machine cycle. The only exception to this is when a MOVX instruction is executed. MOVX is a one-byte, 2-cycle instruction that accesses external data memory. During a MOVX, the two fetches in the second cycle are skipped while the external data memory is being addressed and strobed. **Figure 2-2 (c)** and **(d)** show the timing for a normal 1-byte, 2-cycle instruction and for a MOVX instruction.

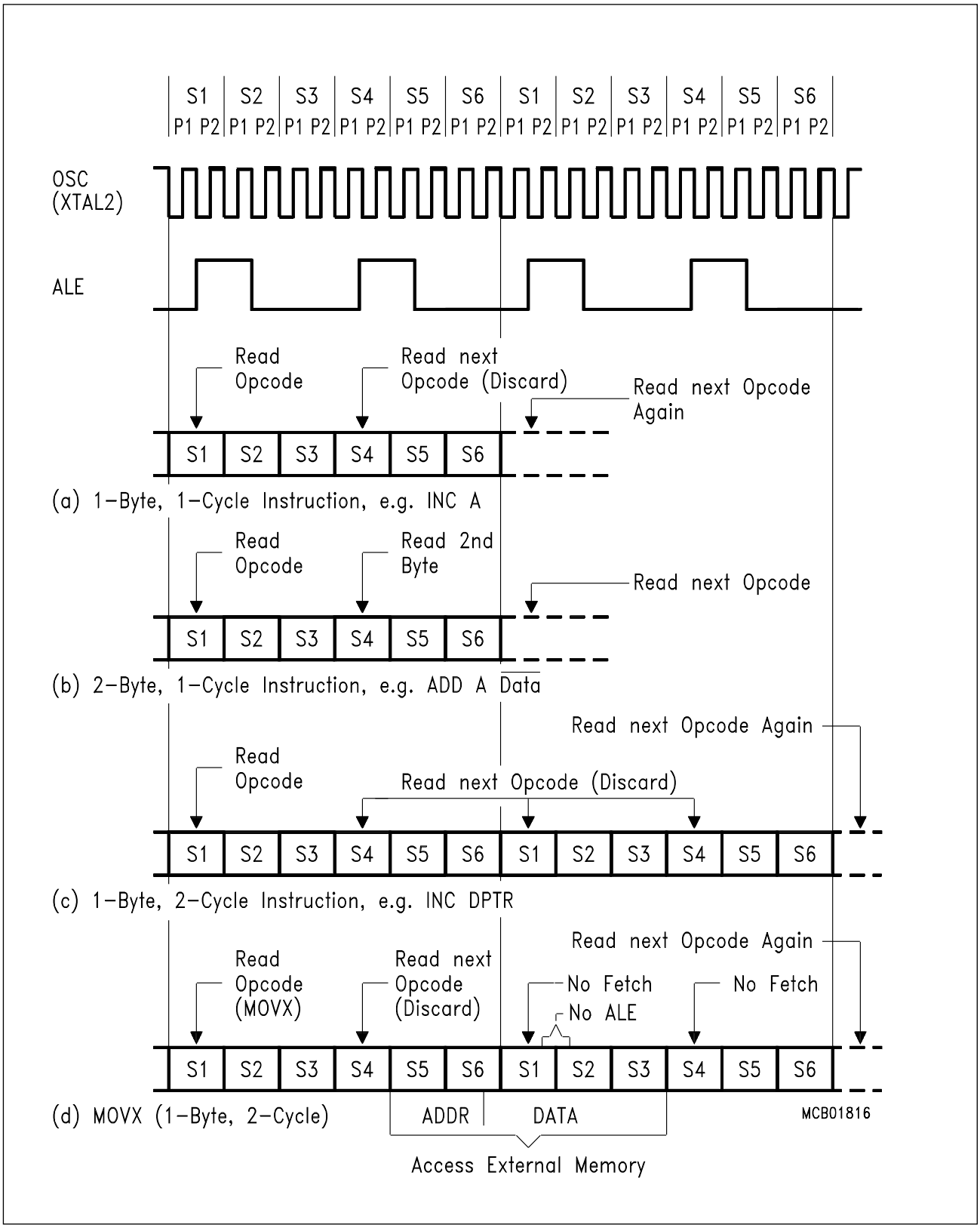

Figure 2-2
Fetch Execute Sequence