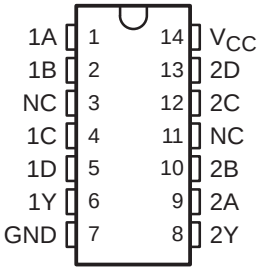
- **Qualification in Accordance With AEC-Q100†**
- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **ESD Protection Exceeds 1000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Buffered Inputs**
- **Typical Propagation Delay 8 ns at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . 15 LSTTL Loads**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **V_{CC} Voltage = 2 V to 6 V**
- **High Noise Immunity; N_{IL} or N_{IH} = 30% of V_{CC}, V_{CC} = 5 V**

† Contact factory for details. Q100 qualification data available on request.

D PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The CD74HC20 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates, with the low power consumption of standard CMOS integrated circuits. The device has the ability to drive 10 LSTTL loads.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Tape and reel	CD74HC20QDRQ1	HC20QQ1

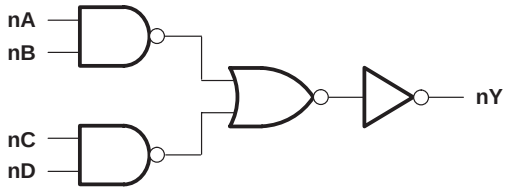
‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level, L = Low voltage level
X = Irrelevant

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} (V_I < –0.5 V or V_I > V_{CC} + 0.5 V) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < –0.5 V or V_O > V_{CC} + 0.5 V) . . . . . ±20 mA
Switch current per output pin, I_O (V_O > –0.5 V or V_O < V_{CC} + 0.5 V) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 86°C/W
Maximum junction temperature, T_J . . . . . 150°C
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . . 300°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are referenced to GND, unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6 V	0	400	
T_A	Operating free-air temperature		–40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I_O (mA)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
V_{OH}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	–0.02	2 V	1.9			1.9		V
			–0.02	4.5 V	4.4			4.4		
			–0.02	6 V	5.9			5.9		
		TTL loads	–4	4.5 V	3.98			3.7		
			–5.2	6 V	5.48			5.2		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	0.02	2 V			0.1		0.1	V
			0.02	4.5 V			0.1		0.1	
			0.02	6 V			0.1		0.1	
		TTL loads	4	4.5 V			0.26		0.4	
			5.2	6 V			0.26		0.4	
I_I	$V_I = V_{CC}$ or GND			6 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND		0	6 V			2		40	µA
C_{IN}							10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

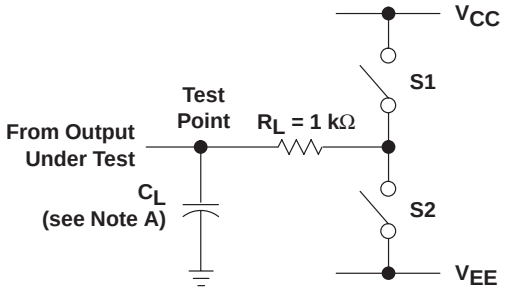
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
t_{pd}	A, B, C, D	Y	C_L = 50 pF	2 V			100		150	ns
				4.5 V			20		30	
				6 V			17		26	
			C_L = 15 pF	5 V		8				
t_t			C_L = 50 pF	2 V			75		110	ns
				4.5 V			15		22	
				6 V			13		19	

operating characteristics, V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance (see Note 4)	26	pF

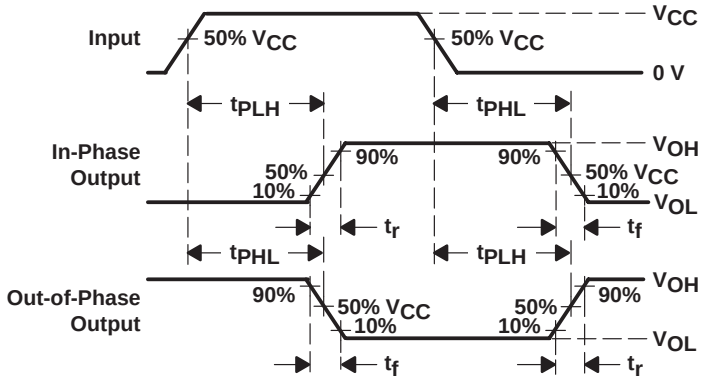
NOTE 4: C_{pd} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_I (C_{pd} + C_L)$
f_I = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

PARAMETER MEASUREMENT INFORMATION

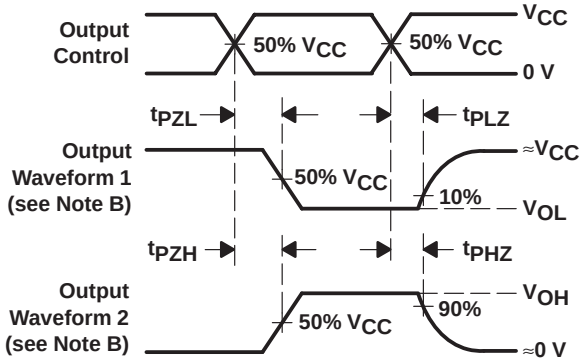


LOAD CIRCUIT

PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD74HC20QM96Q1	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

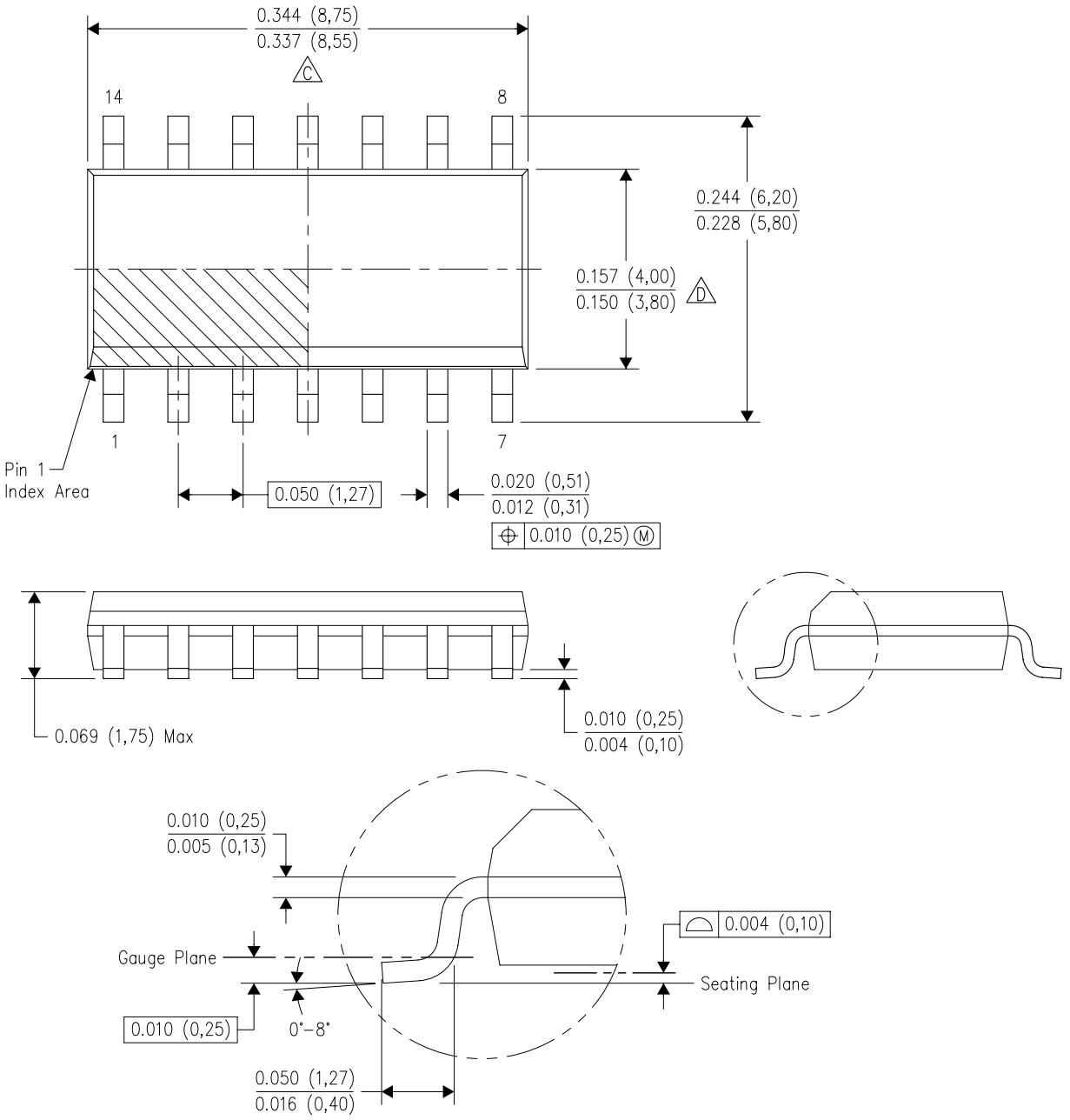
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF CD74HC20-Q1 :
- Catalog: CD74HC20
- Military: CD54HC20

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

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