

FEATURES

- ±15-kV Human-Body Model (HBM) ESD Protection on Card Side
- Logic-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Supplies
- Integrated Card-Detect Circuitry
- Integrated Pullup/Pulldown Resistors Save Board Space and Cost
- Matched Pinout With CompactFlash™ (CF) Connector Pin Configurations to Optimize PCB Layout
- Input-Disable Feature Allows Floating Input Conditions
- I_{off} Supports Partial-Power-Down Mode Operation
- Offered in 114-Ball LFBGA Package for Space-Constrained Applications
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance
 - ±15-kV HBM
 - ±4-kV IEC61000-4-2, Contact Discharge (Latch-Up Immune)

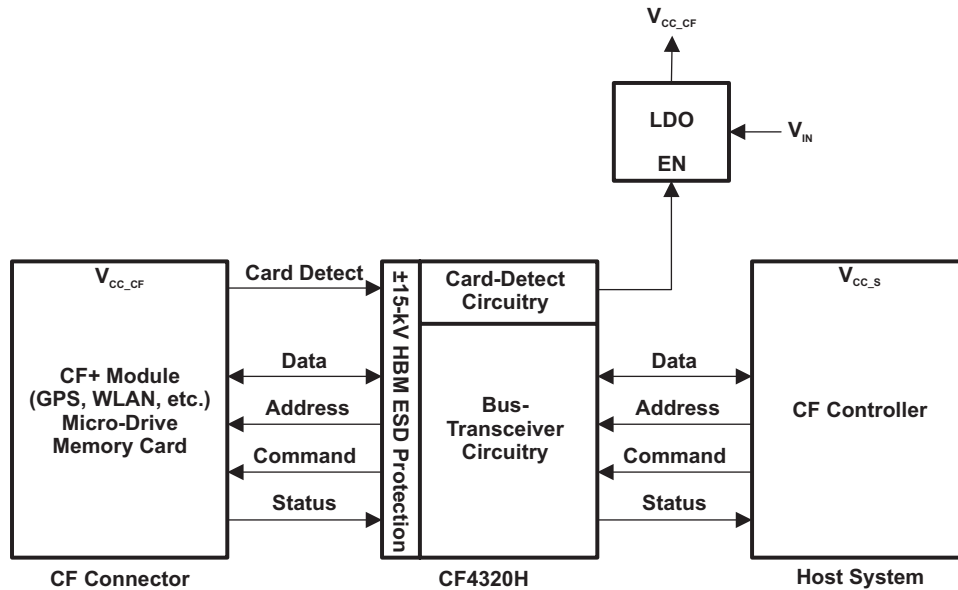
TARGET APPLICATIONS

- GPS PDAs
- PDA Phones
- Industrial PDAs
- High-End Digital Cameras

DESCRIPTION/ORDERING INFORMATION

The CF4320H is a CompactFlash™ (CF) interface device designed to provide a single-chip solution for CF card interfaces. Separate V_{CC} rails for the system-bus side and the CF connector-bus side allow voltage-level shifting. This is helpful for interfacing between a core chipset that may operate from 3.3 V down to 1.65 V, and CF cards that operate from 3.3-V or 5-V supply voltages. All the input buffers feature the input-disable function, which allows conditional floating input signals. The input, output, and I/O buffers on the CF connector side have been defined to comply with CF+ and CF specification revisions 1.4 and 2.0.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

CompactFlash is a trademark of Sandisk Corporation.

CARD-DETECT CIRCUIT

The CF4320H has an integrated card-detect circuit that generates a LOW card-detect signal when a CF card is plugged into the socket. This circuit is supplied by a separate power-supply pin, V_{CC_SD} , which operates from 1.65 V to 5.5 V. The card-detect signal can be used to control a voltage regulator, which may power the CF slot and the CF side of the CF4320H. The inputs to this circuitry ($\overline{CD1}$ and $\overline{CD2}$) have internal pullup resistors to pull them to a HIGH logic state if there is no card in the CF slot. V_{CC_SD} is particularly helpful when the core processor operates at a low V_{CC} , but the regulator needs a higher control-signal voltage.

CARD-DETECT SIGNALS

| INPUTS | | OUTPUT \overline{SCD} |
|------------------|------------------|----------------------------|
| $\overline{CD1}$ | $\overline{CD2}$ | |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | LFBGA – GKF | Tape and reel | CF4320HGKFR | CF4320 |
| | LFBGA – ZKF | Tape and reel | CF4320HZKFR | CF4320 |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

BUS-TRANSCEIVER CIRCUIT

Command and Status Bits

Most CF controllers are embedded in processors or microcontrollers and use GPIOs to send command signals and receive status signals from the card to manage operation. The CF interface consists of eight control signals and six status signals. The CF standard requires that each of these signals have a 100-k Ω pullup resistor. The CF4320H includes an internal 100-k Ω pullup resistor on the input of each of these signals, which saves board real estate and lowers overall system cost

COMMAND LINE BUFFERS⁽¹⁾ ($\overline{BVD1}$, $\overline{BVD2}$, \overline{INPACK} , \overline{OE} , \overline{IORD} , \overline{IOWR} , \overline{READY} , \overline{REG} , $\overline{CE1}$, $\overline{CE2}$, \overline{WAIT} , \overline{WE} , \overline{WP})

| INPUTS | | | OUTPUT |
|-------------------------|----------------------|-------|--|
| $\overline{MASTER_EN}$ | $\overline{BUF_EN}$ | INPUT | |
| L | L | H | H |
| L | L | L | L |
| L | H | X | Z, Command line buffer inputs can float. |
| H | X | X | Z, low-power mode |

(1) X = H or L

RESET⁽¹⁾

| INPUTS | | OUTPUT RESET |
|-------------------------|---------------------|-------------------|
| $\overline{MASTER_EN}$ | \overline{SRESET} | |
| L | H | H |
| L | L | L |
| H | X | Z, low-power mode |

(1) X = H or L

Data Bits

The CF4320H has 16 data lines organized as two groups of 8 bits each. The $\overline{\text{ENL}}$ signal controls the lower 8 bits (D07–D00), while the $\overline{\text{ENH}}$ signal controls the upper 8 bits (D15–D08).

LOWER 8-BIT DATA BUS TRANSCEIVERS⁽¹⁾ (D07–D00, SD07–SD00)

| INPUTS | | | OPERATION |
|--------------------------------|-------------------------|---|--|
| $\overline{\text{MASTER_EN}}$ | $\overline{\text{ENL}}$ | DIR ($\overline{\text{S}}/\text{CF}$) | |
| L | L | H | SD data to D bus |
| L | L | L | D data to SD bus |
| L | H | X | Isolation. D07–D00 and SD07–SD00 inputs can float. |
| H | X | X | Isolation, low-power mode |

(1) X = H or L

UPPER 8-BIT DATA BUS TRANSCEIVERS⁽¹⁾ (D15–D08, SD15–SD08)

| INPUTS | | | OPERATION |
|--------------------------------|-------------------------|---|--|
| $\overline{\text{MASTER_EN}}$ | $\overline{\text{ENH}}$ | DIR ($\overline{\text{S}}/\text{CF}$) | |
| L | L | H | SD data to D bus |
| L | L | L | D data to SD bus |
| L | H | X | Isolation. D15–D08 and SD15–SD08 inputs can float. |
| H | X | X | Isolation, low-power mode |

(1) X = H or L

Address Bits

The CF4320H has 11 unidirectional address bits flowing from the system to the CF card.

ADDRESS BUS BUFFERS⁽¹⁾

| INPUTS | | | OUTPUT A |
|--------------------------------|-----------------------------|----|-------------------------|
| $\overline{\text{MASTER_EN}}$ | $\overline{\text{BUF_EN}}$ | SA | |
| L | L | H | H |
| L | L | L | L |
| L | H | X | Z, SA inputs can float. |
| H | X | X | Z, low-power mode |

(1) X = H or L

Direction Signal Bit

The DIR(\overline{S}/CF) input controls the data direction between the system bus and the CF card. The CF4320H has circuitry to generate a DIR_OUT signal using the \overline{SOE} and \overline{SIORD} signals. DIR(\overline{S}/CF) and DIR_OUT are placed adjacent to each other, which is convenient for connecting DIR(\overline{S}/CF) and DIR_OUT, if DIR_OUT is used. This saves an additional signal from the system controller to control the data direction. When either \overline{SOE} or \overline{SIORD} is low, the data direction is from the CF card side to the system side (DIR_OUT = L).

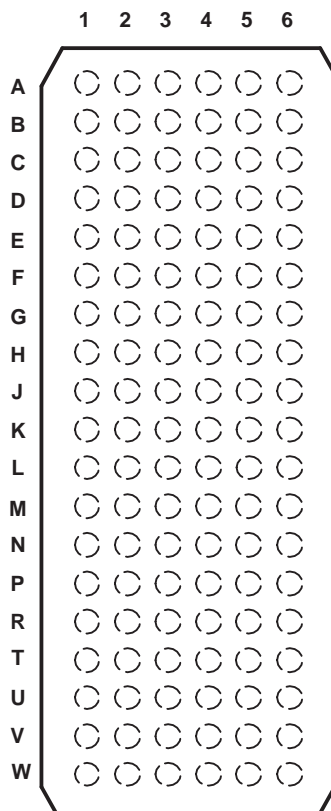
DIR_OUT⁽¹⁾

| INPUTS | | | | OUTPUT DIR_OUT |
|--------|-----------|-----|-------|-------------------|
| BUF_EN | MASTER_EN | SOE | SIORD | |
| L | L | L | L | L |
| L | L | L | H | L |
| L | L | H | L | L |
| L | L | H | H | H |
| H | L | X | X | L |
| X | H | X | X | Z, low-power mode |

(1) X = H or L

BOARD-OPTIMIZED PIN CONFIGURATION

GKF OR ZKF PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|------------------|-------------------|---------------------|--------------------------|--------------------|--------------------|
| A | D12 | D04 | D03 | SD14 | SD12 | SD11 |
| B | D13 | D05 | D11 | SD13 | SD10 | SD09 |
| C | D14 | D06 | SD15 | SINPACK | SD08 | SD07 |
| D | D15 | D07 | V _{CC_C} F | V _{CC_S} | SD06 | SD05 |
| E | $\overline{CE2}$ | $\overline{CE1}$ | GND | GND | SD04 | SD03 |
| F | \overline{OE} | A10 | V _{CC_C} F | V _{CC_S} | SD02 | SD01 |
| G | A09 | \overline{IORD} | GND | GND | SD00 | $\overline{SCE1}$ |
| H | A08 | \overline{IOWR} | V _{CC_C} F | V _{CC_S} | ENL | ENH |
| J | A07 | \overline{WE} | GND | GND | MASTER_EN | BUF_EN |
| K | A06 | READY | A05 | $\overline{SCE2}$ | \overline{SOE} | \overline{SIORD} |
| L | A04 | RESET | GND | GND | \overline{SWE} | \overline{SIOWR} |
| M | A03 | \overline{WAIT} | V _{CC_C} F | V _{CC_S} | SREADY | SRESET |
| N | A02 | INPACK | GND | GND | \overline{SWAIT} | \overline{SREG} |
| P | A01 | \overline{REG} | V _{CC_C} F | GND | SBVD2 | SBVD1 |
| R | A00 | BVD2 | V _{CC_C} F | V _{CC_S} | SA10 | SWP |
| T | D00 | BVD1 | V _{CC_SD} | DIR(\overline{S} /CF) | SA08 | SA09 |
| U | D01 | D08 | $\overline{CD1}$ | DIR_OUT | SA06 | SA07 |
| V | D02 | D09 | $\overline{CD2}$ | SA00 | SA04 | SA05 |
| W | WP | D10 | \overline{SCD} | SA01 | SA02 | SA03 |

TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION | REFERENCED TO | I/O ⁽¹⁾ |
|----------|---------------------|--|--------------------|--------------------|
| NO. | NAME | | | |
| A1 | D12 | Data bit 12 connected to card | V _{CC_CF} | I/O |
| B1 | D13 | Data bit 13 connected to card | V _{CC_CF} | I/O |
| C1 | D14 | Data bit 14 connected to card | V _{CC_CF} | I/O |
| D1 | D15 | Data bit 15 connected to card | V _{CC_CF} | I/O |
| E1 | $\overline{CE2}$ | Card enable connected to card | V _{CC_CF} | O |
| F1 | \overline{OE} | Output enable connected to card | V _{CC_CF} | O |
| G1 | A09 | Address bit 9 connected to card | V _{CC_CF} | O |
| H1 | A08 | Address bit 8 connected to card | V _{CC_CF} | O |
| J1 | A07 | Address bit 7 connected to card | V _{CC_CF} | O |
| K1 | A06 | Address bit 6 connected to card | V _{CC_CF} | O |
| L1 | A04 | Address bit 4 connected to card | V _{CC_CF} | O |
| M1 | A03 | Address bit 3 connected to card | V _{CC_CF} | O |
| N1 | A02 | Address bit 2 connected to card | V _{CC_CF} | O |
| P1 | A01 | Address bit 1 connected to card | V _{CC_CF} | O |
| R1 | A00 | Address bit 0 connected to card | V _{CC_CF} | O |
| T1 | D00 | Data bit 0 connected to card | V _{CC_CF} | I/O |
| U1 | D01 | Data bit 1 connected to card | V _{CC_CF} | I/O |
| V1 | D02 | Data bit 2 connected to card | V _{CC_CF} | I/O |
| W1 | WP | Write protect connected to card. Pulled up to V _{CC_CF} through 100 kΩ. | V _{CC_CF} | I |
| A2 | D04 | Data bit 4 connected to card | V _{CC_CF} | I/O |
| B2 | D05 | Data bit 5 connected to card | V _{CC_CF} | I/O |
| C2 | D06 | Data bit 6 connected to card | V _{CC_CF} | I/O |
| D2 | D07 | Data bit 7 connected to card | V _{CC_CF} | I/O |
| E2 | $\overline{CE1}$ | Card enable connected to card | V _{CC_CF} | O |
| F2 | A10 | Address bit 10 connected to card | V _{CC_CF} | O |
| G2 | \overline{IORD} | I/O read connected to card | V _{CC_CF} | O |
| H2 | \overline{IOWR} | I/O write connected to card | V _{CC_CF} | O |
| J2 | \overline{WE} | Write enable connected to card | V _{CC_CF} | O |
| K2 | READY | Ready connected to card. Pulled up to V _{CC_CF} through 100 kΩ. | V _{CC_CF} | I |
| L2 | RESET | Reset connected to card | V _{CC_CF} | O |
| M2 | \overline{WAIT} | Wait connected to card. Pulled up to V _{CC_CF} through 100 kΩ. | V _{CC_CF} | I |
| N2 | \overline{INPACK} | Input acknowledge connected to card. Pulled up to V _{CC_CF} through 100 kΩ. | V _{CC_CF} | I |
| P2 | \overline{REG} | Register connected to card | V _{CC_CF} | O |
| R2 | BVD2 | BVD2 connected to card. Pulled up to V _{CC_CF} through 100 kΩ. | V _{CC_CF} | I |
| T2 | BVD1 | BVD1 connected to card. Pulled up to V _{CC_CF} through 100 kΩ. | V _{CC_CF} | I |
| U2 | D08 | Data bit 8 connected to card | V _{CC_CF} | I/O |
| V2 | D09 | Data bit 9 connected to card | V _{CC_CF} | I/O |
| W2 | D10 | Data bit 10 connected to card | V _{CC_CF} | I/O |
| A3 | D03 | Data bit 3 connected to card | V _{CC_CF} | I/O |
| B3 | D11 | Data bit 11 connected to card | V _{CC_CF} | I/O |
| C3 | SD15 | Data bit 15 connected to controller | V _{CC_S} | I/O |
| D3 | V _{CC_CF} | Card-side supply voltage. V _{CC_CF} powers all card-side inputs, outputs, and I/Os. | | Power |
| E3 | GND | Ground | | |
| F3 | V _{CC_CF} | Card-side supply voltage. V _{CC_CF} powers all card-side inputs, outputs, and I/Os. | | Power |
| G3 | GND | Ground | | |

(1) I = input, O = output, I/O = input/output

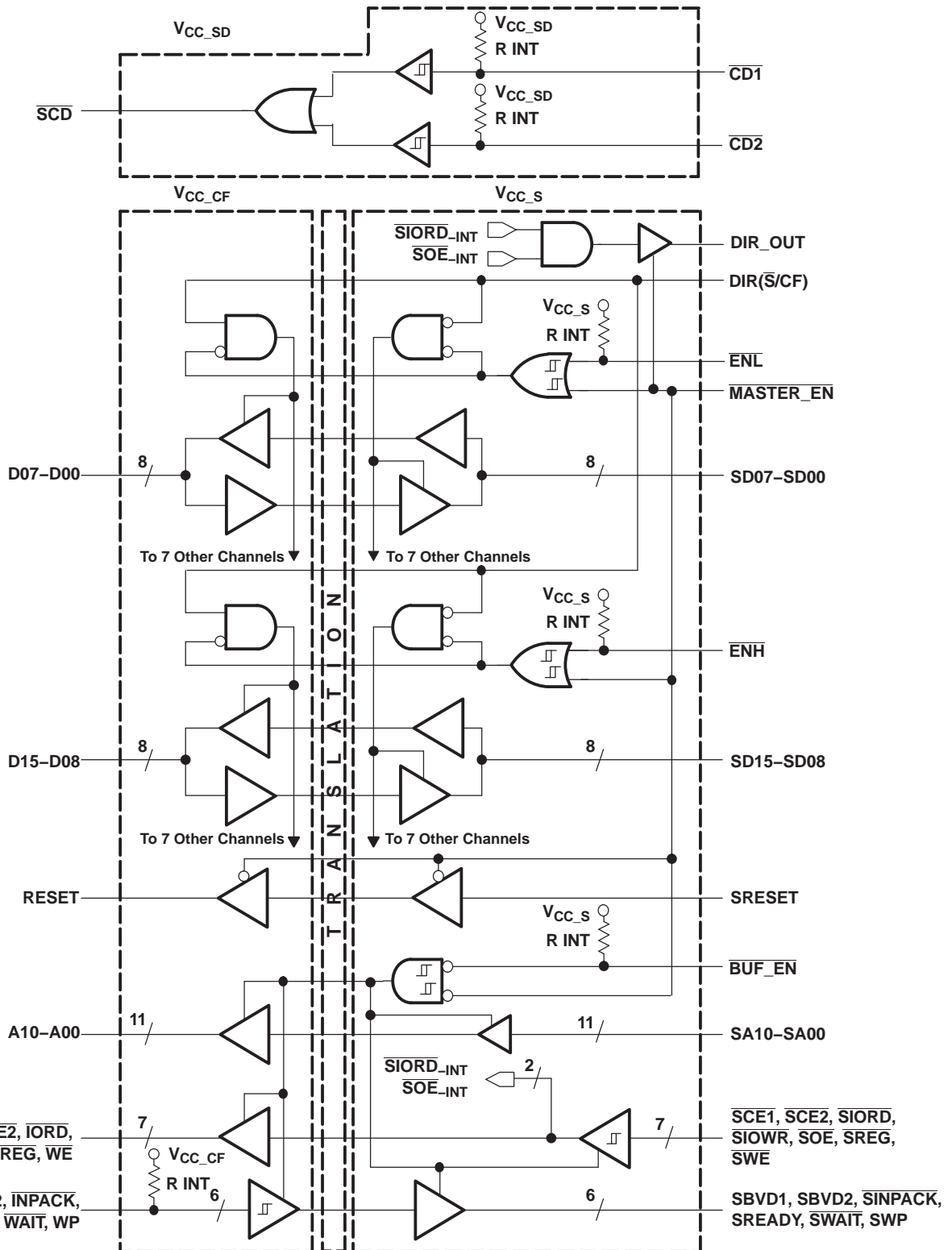
TERMINAL FUNCTIONS (continued)

| TERMINAL | | DESCRIPTION | REFERENCED TO | I/O ⁽¹⁾ |
|----------|--------------------------|---|--------------------|--------------------|
| NO. | NAME | | | |
| H3 | V _{CC_Cf} | Card-side supply voltage. V _{CC_Cf} powers all card-side inputs, outputs, and I/Os. | | Power |
| J3 | GND | Ground | | |
| K3 | A05 | Address bit 5 connected to card | V _{CC_Cf} | O |
| L3 | GND | Ground | | |
| M3 | V _{CC_Cf} | Card-side supply voltage. V _{CC_Cf} powers all card-side inputs, outputs, and I/Os. | | Power |
| N3 | GND | Ground | | |
| P3 | V _{CC_Cf} | Card-side supply voltage. V _{CC_Cf} powers all card-side inputs, outputs, and I/Os. | | Power |
| R3 | V _{CC_Cf} | Card-side supply voltage. V _{CC_Cf} powers all card-side inputs, outputs, and I/Os. | | Power |
| T3 | V _{CC_SD} | Card-detect supply voltage. V _{CC_SD} powers the card-detect circuitry. | | Power |
| U3 | $\overline{CD1}$ | Card detect connected to card. Pulled up to V _{CC_Cf} through 100 k Ω . | V _{CC_SD} | I |
| V3 | $\overline{CD2}$ | Card detect connected to card. Pulled up to V _{CC_Cf} through 100 k Ω . | V _{CC_SD} | I |
| W3 | \overline{SCD} | Card detect connected to controller | V _{CC_SD} | O |
| A4 | SD14 | Data bit 14 connected to controller | V _{CC_s} | I/O |
| B4 | SD13 | Data bit 13 connected to controller | V _{CC_s} | I/O |
| C4 | $\overline{SINPACK}$ | Input acknowledge connected to controller | V _{CC_s} | I/O |
| D4 | V _{CC_s} | Controller-side supply voltage. V _{CC_s} powers all controller-side inputs, outputs, and I/Os. | | Power |
| E4 | GND | Ground | | |
| F4 | V _{CC_s} | Controller-side supply voltage. V _{CC_s} powers all controller-side inputs, outputs, and I/Os. | | Power |
| G4 | GND | Ground | | |
| H4 | V _{CC_s} | Controller-side supply voltage. V _{CC_s} powers all controller-side inputs, outputs, and I/Os. | | Power |
| J4 | GND | Ground | | |
| K4 | $\overline{SCE2}$ | Card enable connected to controller | V _{CC_s} | I |
| L4 | GND | Ground | | |
| M4 | V _{CC_s} | Controller-side supply voltage. V _{CC_s} powers all controller-side inputs, outputs, and I/Os. | | Power |
| N4 | GND | Ground | | |
| P4 | GND | Ground | | |
| R4 | V _{CC_s} | Controller-side supply voltage. V _{CC_s} powers all controller-side inputs, outputs, and I/Os. | | Power |
| T4 | DIR(\overline{S}/CF) | Direction controls flow of data from system to CF and vice-versa | V _{CC_s} | I |
| U4 | DIR_OUT | Data direction generated by CF4320H. Can be connected to DIR(\overline{S}/CF). | V _{CC_s} | O |
| V4 | SAO0 | Address bit 0 connected to controller | V _{CC_s} | I |
| W4 | SAO1 | Address bit 1 connected to controller | V _{CC_s} | I |
| A5 | SD12 | Data bit 12 connected to controller | V _{CC_s} | I/O |
| B5 | SD10 | Data bit 10 connected to controller | V _{CC_s} | I/O |
| C5 | SD08 | Data bit 8 connected to controller | V _{CC_s} | I/O |
| D5 | SD06 | Data bit 6 connected to controller | V _{CC_s} | I/O |
| E5 | SD04 | Data bit 4 connected to controller | V _{CC_s} | I/O |
| F5 | SD02 | Data bit 2 connected to controller | V _{CC_s} | I/O |
| G5 | SD00 | Data bit 0 connected to controller | V _{CC_s} | I/O |
| H5 | \overline{ENL} | Enable for data bits 0–7. Pulled up to V _{CC_s} through 100 k Ω . | V _{CC_s} | I |
| J5 | $\overline{MASTER_EN}$ | Enable for all transceivers and buffers except the card-detect circuitry | V _{CC_s} | I |
| K5 | \overline{SOE} | Output enable connected to controller | V _{CC_s} | I |
| L5 | \overline{SWE} | Write enable connected to controller | V _{CC_s} | I |
| M5 | SREADY | Ready connected to controller | V _{CC_s} | O |

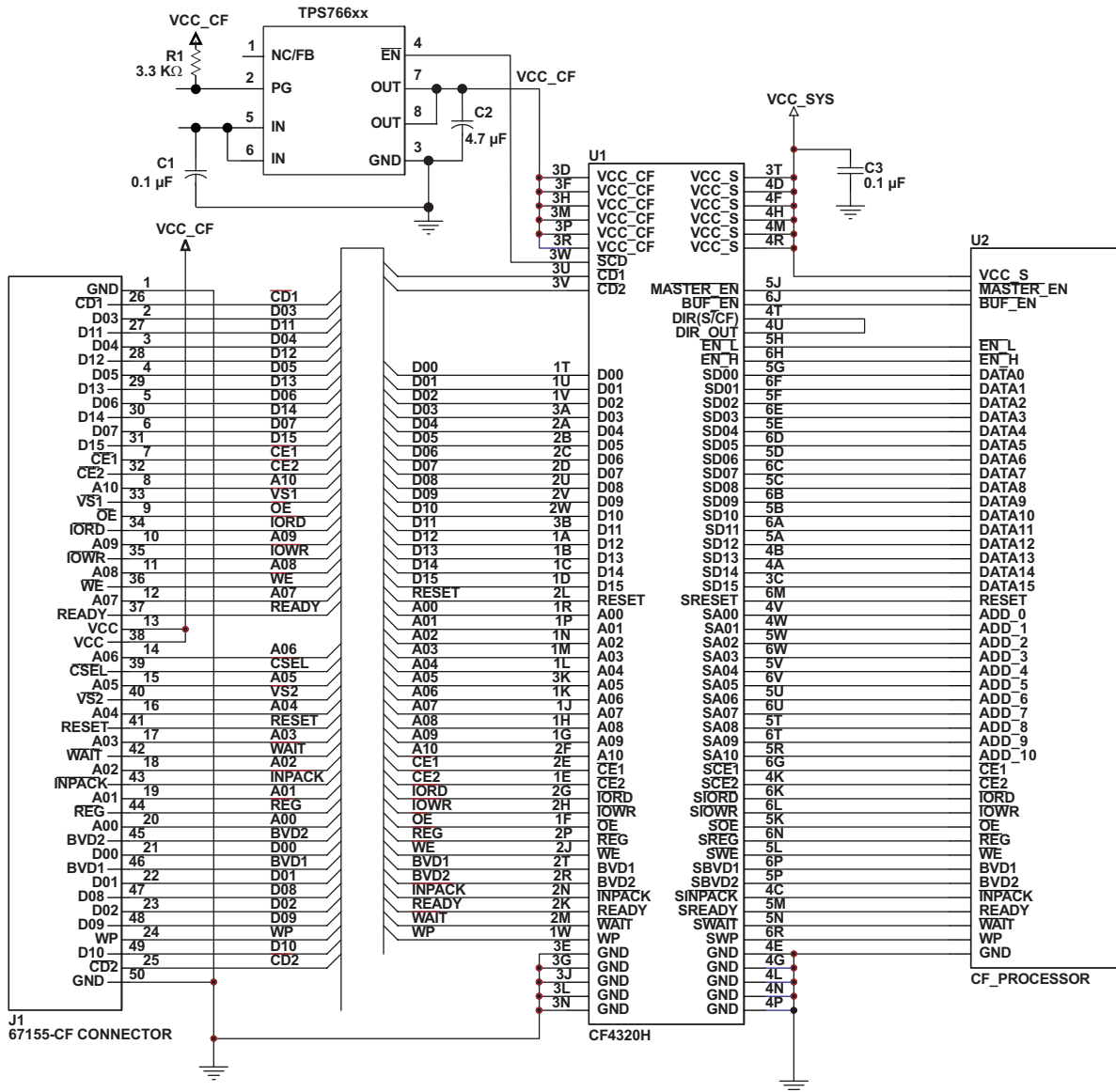
TERMINAL FUNCTIONS (continued)

| TERMINAL | | DESCRIPTION | REFERENCED TO | I/O ⁽¹⁾ |
|----------|-----------------------------|---|-------------------|--------------------|
| NO. | NAME | | | |
| N5 | $\overline{\text{SWAIT}}$ | Wait connected to controller | V _{CC_S} | O |
| P5 | SBVD2 | BVD2 connected to controller | V _{CC_S} | O |
| R5 | SA10 | Address bit 10 connected to controller | V _{CC_S} | I |
| T5 | SA08 | Address bit 8 connected to controller | V _{CC_S} | I |
| U5 | SA06 | Address bit 6 connected to controller | V _{CC_S} | I |
| V5 | SA04 | Address bit 4 connected to controller | V _{CC_S} | I |
| W5 | SA02 | Address bit 2 connected to controller | V _{CC_S} | I |
| A6 | SD11 | Data bit 11 connected to controller | V _{CC_S} | I/O |
| B6 | SD09 | Data bit 9 connected to controller | V _{CC_S} | I/O |
| C6 | SD07 | Data bit 7 connected to controller | V _{CC_S} | I/O |
| D6 | SD05 | Data bit 5 connected to controller | V _{CC_S} | I/O |
| E6 | SD03 | Data bit 3 connected to controller | V _{CC_S} | I/O |
| F6 | SD01 | Data bit 1 connected to controller | V _{CC_S} | I/O |
| G6 | $\overline{\text{SCE1}}$ | Card enable connected to controller | V _{CC_S} | I |
| H6 | $\overline{\text{ENH}}$ | Enable for data bits 8–15. Pulled up to V _{CC_S} through 100 kΩ. | V _{CC_S} | I |
| J6 | $\overline{\text{BUF_EN}}$ | Enable for address and control/status lines. Pulled up to V _{CC_S} through 100 kΩ. | V _{CC_S} | I |
| K6 | $\overline{\text{SIORD}}$ | I/O read connected to controller | V _{CC_S} | I |
| L6 | $\overline{\text{SIOWR}}$ | I/O write connected to controller | V _{CC_S} | I |
| M6 | SRESET | Reset connected to controller | V _{CC_S} | I |
| N6 | $\overline{\text{SREG}}$ | Register connected to controller | V _{CC_S} | I |
| P6 | SBVD1 | BVD1 connected to controller | V _{CC_S} | O |
| R6 | SWP | Write protect connected to controller | V _{CC_S} | O |
| T6 | SA09 | Address bit 9 connected to controller | V _{CC_S} | I |
| U6 | SA07 | Address bit 7 connected to controller | V _{CC_S} | I |
| V6 | SA05 | Address bit 5 connected to controller | V _{CC_S} | I |
| W6 | SA03 | Address bit 3 connected to controller | V _{CC_S} | I |

LOGIC DIAGRAM



NOTE: R INT \geq 100 k Ω



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT | |
|---------------|---|-------------|---|--------------------|------|----|
| V_{CC_S} | Supply voltage range | | -0.5 | 4.6 | V | |
| V_{CC_CF} | | | -0.5 | 6.5 | | |
| V_{CC_SD} | | | | | | |
| V_I | Input voltage range | I/O ports | SD, SA ⁽²⁾ | -0.5 | 4.6 | V |
| | | | D, A | -0.5 | 6.5 | |
| | | Input ports | SCE1, SCE2, SIORD, SIOWR, SOE, SREG, SWE | -0.5 | 4.6 | |
| | | | BVD1, BVD2, READY, INPACK, WAIT, WP | -0.5 | 6.5 | |
| Control ports | DIR(\bar{S}/CF), MASTER_EN, ENL, ENH | -0.5 | 4.6 | | | |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | System port | -0.5 | 4.6 | V | |
| | | CF port | -0.5 | 6.5 | | |
| V_O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | System port | -0.5 | $V_{CC_S} + 0.5$ | V | |
| | | CF port | -0.5 | $V_{CC_CF} + 0.5$ | | |
| I_{IK} | Input clamp current | $V_I < 0$ | | -50 | mA | |
| I_{OK} | Output clamp current | $V_O < 0$ | | -50 | mA | |
| I_O | Continuous output current | | | ±50 | mA | |
| | Continuous current through each V_{CC_S} , V_{CC_CF} , V_{CC_SD} , or GND | | | ±100 | mA | |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | | | 36 | °C/W | |
| T_{stg} | Storage temperature range | | | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 6.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾

| | | | V _{CCI} | V _{CCO} | MIN | MAX | UNIT |
|--------------------|----------------------------|---|------------------|------------------|---------------------------|--------------------|------|
| V _{CC_SD} | Card-detect supply voltage | | | | 1.65 | 5.5 | V |
| V _{CC_S} | System-side supply voltage | | | | 1.65 | V _{CC_CF} | V |
| V _{CC_CF} | CF-side supply voltage | | | | 3 | 5.5 | V |
| V _{IH} | High-level input voltage | Card-detect inputs (CD1, CD2) | 1.65 V to 5.5 V | | V _{CC_SD} × 0.65 | | V |
| V _{IL} | Low-level input voltage | Card-detect inputs (CD1, CD2) | 1.65 V to 5.5 V | | V _{CC_SD} × 0.35 | | V |
| V _{IH} | High-level input voltage | System port (SD, SA, SRESET) | 1.65 V to 1.95 V | | V _{CC_S} × 0.65 | | V |
| | | | 1.95 V to 2.7 V | | 1.7 | | |
| | | | 2.7 V to 3.6 V | | 2 | | |
| V _{IL} | Low-level input voltage | System port (SD, SA, SRESET) | 1.65 V to 1.95 V | | V _{CC_S} × 0.35 | | V |
| | | | 1.95 V to 2.7 V | | 0.7 | | |
| | | | 2.7 V to 3.6 V | | 0.8 | | |
| V _{IH} | High-level input voltage | Control inputs (DIR, MASTER_EN, ENL, ENH, BUF_EN) | 1.65 V to 1.95 V | | V _{CC_S} × 0.65 | | V |
| | | | 1.95 V to 2.7 V | | 1.7 | | |
| | | | 2.7 V to 3.6 V | | 2 | | |
| V _{IL} | Low-level input voltage | Control inputs (DIR, MASTER_EN, ENL, ENH, BUF_EN) | 1.65 V to 1.95 V | | V _{CC_S} × 0.35 | | V |
| | | | 1.95 V to 2.7 V | | 0.7 | | |
| | | | 2.7 V to 3.6 V | | 0.8 | | |
| V _{IH} | High-level input voltage | CF port (D, A) | 3 V to 3.6 V | | 2 | | V |
| | | | 4.5 V to 5.5 V | | V _{CC_CF} × 0.7 | | |
| V _{IL} | Low-level input voltage | CF port (D, A) | 3 V to 3.6 V | | 0.8 | | V |
| | | | 4.5 V to 5.5 V | | V _{CC_CF} × 0.3 | | |
| V _O | Card-detect output voltage | | | | 0 | V _{CC_SD} | V |
| | System-side output voltage | | | | 0 | V _{CC_S} | |
| | CF-side output voltage | | | | 0 | V _{CC_CF} | |
| I _{OH} | High-level output current | Card detect | 1.65 V to 1.95 V | | –2 | | mA |
| | | | 1.95 V to 2.7 V | | –4 | | |
| | | | 2.7 V to 3.6 V | | –8 | | |
| | | | 4.5 V to 5.5 V | | –12 | | |
| I _{OL} | Low-level output current | Card detect | 1.65 V to 1.95 V | | 2 | | mA |
| | | | 1.95 V to 2.7 V | | 4 | | |
| | | | 2.7 V to 3.6 V | | 8 | | |
| | | | 4.5 V to 5.5 V | | 12 | | |
| I _{OH} | High-level output current | System port | 1.65 V to 1.95 V | | 2 | | mA |
| | | | 1.95 V to 2.7 V | | 6 | | |
| | | | 2.7 V to 3.6 V | | 12 | | |
| I _{OL} | Low-level output current | System port | 1.65 V to 1.95 V | | 2 | | mA |
| | | | 1.95 V to 2.7 V | | 6 | | |
| | | | 2.7 V to 3.6 V | | 12 | | |
| I _{OH} | High-level output current | CF port | 3 V to 3.6 V | | 12 | | mA |
| | | | 4.5 V to 5.5 V | | 16 | | |
| I _{OL} | Low-level output current | CF port | 3 V to 3.6 V | | 12 | | mA |
| | | | 4.5 V to 5.5 V | | 16 | | |

(1) V_{CCI} is the V_{CC} associated with the input port.(2) V_{CCO} is the V_{CC} associated with the output port.(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions (continued)

| | | V _{CCI} | V _{CCO} | MIN | MAX | UNIT |
|---------------------|------------------------------------|------------------|------------------|-----|-----|------|
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 1.65 V to 2.7 V | | | >20 | ns/V |
| | | 2.7 V to 3.6 V | | >20 | | |
| | | 4.5 V to 5.5 V | | >20 | | |
| T _A | Operating free-air temperature | | | –40 | 85 | °C |

Electrical Characteristics

over recommended operating free-air temperature range (CF card-detect logic) (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC_SD} | T _A = 25°C | | | –40°C to 85°C | | UNIT |
|--------------------|---|--|-----------------------|--------------------------|-----|--------------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} | I _{OH} = –100 μA | 1.65 V to 5.5 V | V _{CC_SD} – 0.1 | | V _{CC_SD} – 0.2 | V | |
| | | I _{OH} = –2 mA | 1.65 V | 1.2 | | 1.2 | | |
| | | I _{OH} = –4 mA | 2.3 V | 2 | | 2 | | |
| | | I _{OH} = –6 mA | 2.7 V | 2.3 | | 2.3 | | |
| | | I _{OH} = –8 mA | 3 V | 2.4 | | 2.4 | | |
| | | I _{OH} = –12 mA | 4.5 V | 3.8 | | 3.8 | | |
| V _{OL} | V _I = V _{IL} | I _{OL} = 100 μA | 1.65 V to 5.5 V | | 0.1 | 0.2 | V | |
| | | I _{OL} = 2 mA | 1.65 V | | 0.2 | 0.2 | | |
| | | I _{OL} = 4 mA | 2.3 V | | 0.2 | 0.2 | | |
| | | I _{OL} = 6 mA | 2.7 V | | 0.3 | 0.3 | | |
| | | I _{OL} = 8 mA | 3 V | | 0.4 | 0.4 | | |
| | | I _{OL} = 12 mA | 4.5 V | | 0.5 | 0.5 | | |
| I _I | V _I = V _{CC_SD} | 1.65 V to 5.5 V | | ±0.5 | | ±1 | μA | |
| | V _I = 0 V | | | –55 | | –60 | | |
| I _{off} | V _I or V _O = 0 to 5.5 V | 0 V | | 55 | | 60 | μA | |
| R _{INT} | $\overline{CD1}$ = GND, $\overline{CD2}$ = GND | 1.65 V to 5.5 V | | 150 300 | | 100 300 | kΩ | |
| I _{CC_SD} | $\overline{CD1}$ and $\overline{CD2}$ = V _{CC_SD} , I _{O_SD} = 0 | 5.5 V | | 0.5 | | 1 | μA | |
| | $\overline{CD1}$ or $\overline{CD2}$ = GND, $\overline{CD2}$ or $\overline{CD1}$ = V _{CC_SD} , I _{O_SD} = 0 | | | 10 | | 10 | | |
| C ₁ | $\overline{CD1}$ or $\overline{CD2}$ | V _I = V _{CC_SD} or GND | 5.5 V | 9 | | | pF | |

Electrical Characteristics⁽¹⁾⁽²⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | V _{CC_S} | V _{CC_CF} | T _A = 25°C | | | –40°C to 85°C | | UNIT | | | |
|-------------------|---|----------------------------------|--|---------------------------|--------------------|-----------------------|----------------------------|----------------------------|---------------|------|------|-----|-----|-----|
| | | | | | | MIN | TYP | MAX | MIN | MAX | | | | |
| V _{T+} | SOE, SCE1, SCE2, SIORD, SIOWR, SWE, SREG | | | 1.65 V | 3 V to 5.5 V | | 0.95 | | 0.6 | 1.4 | V | | | |
| | | | | 2.3 V | | | 1.32 | | 0.9 | 1.8 | | | | |
| | | | | 2.7 V | | | 1.49 | | 1 | 2 | | | | |
| | | | | 3 V | | | 1.67 | | 1.2 | 2.2 | | | | |
| V _{T–} | SOE, SCE1, SCE2, SIORD, SIOWR, SWE, SREG | | | 1.65 V | 3 V to 5.5 V | | 0.66 | | 0.19 | 0.8 | V | | | |
| | | | | 2.3 V | | | 0.87 | | 0.39 | 1.15 | | | | |
| | | | | 2.7 V | | | 0.98 | | 0.49 | 1.32 | | | | |
| | | | | 3 V | | | 1.08 | | 0.59 | 1.5 | | | | |
| ΔV _T | SOE, SCE1, SCE2, SIORD, SIOWR, SWE, SREG | | | 1.65 V | 3 V to 5.5 V | | 0.31 | | 0.1 | 0.7 | V | | | |
| | | | | 2.3 V | | | 0.46 | | 0.25 | 0.7 | | | | |
| | | | | 2.7 V | | | 0.52 | | 0.3 | 0.9 | | | | |
| | | | | 3 V | | | 0.61 | | 0.4 | 0.9 | | | | |
| V _{T+} | BVD1, BVD2, READY, INPACK, WAIT | | | 1.65 V to 3.6 V | 3 V | | 1.67 | | 1.3 | 2.2 | V | | | |
| | | | | | 4.5 V | | 2.44 | | 1.9 | 3.1 | | | | |
| V _{T–} | BVD1, BVD2, READY, INPACK, WAIT, WP | | | 1.65 V to 3.6 V | 3 V | | 1.11 | | 0.6 | 1.5 | V | | | |
| | | | | | 4.5 V | | 1.43 | | 1 | 2 | | | | |
| ΔV _T | BVD1, BVD2, READY, INPACK, WAIT | | | 1.65 V to 3.6 V | 3 V | | 0.58 | | 0.35 | 1 | V | | | |
| | | | | | 4.5 V | | 1.02 | | 0.6 | 1.5 | | | | |
| V _{T+} | BUF_EN, ENH, ENL, MASTER_EN | | | 1.65 V | 3 V to 5.5 V | | 1 | | 0.6 | 1.4 | V | | | |
| | | | | 2.3 V | | | 1.37 | | 1.1 | 1.8 | | | | |
| | | | | 2.7 V | | | 1.54 | | 1.1 | 2 | | | | |
| | | | | 3 V | | | 1.72 | | 1.3 | 2.2 | | | | |
| V _{T–} | BUF_EN, ENH, ENL, MASTER_EN | | | 1.65 V | 3 V to 5.5 V | | 0.34 | | 0.15 | 1 | V | | | |
| | | | | 2.3 V | | | 0.63 | | 0.15 | 1.2 | | | | |
| | | | | 2.7 V | | | 0.75 | | 0.2 | 1.32 | | | | |
| | | | | 3 V | | | 0.88 | | 0.4 | 1.5 | | | | |
| ΔV _T | BUF_EN, ENH, ENL, MASTER_EN | | | 1.65 V | 3 V to 5.5 V | | 0.67 | | 0.08 | 1.1 | V | | | |
| | | | | 2.3 V | | | 0.76 | | 0.2 | 1.2 | | | | |
| | | | | 2.7 V | | | 0.8 | | 0.26 | 1.3 | | | | |
| | | | | 3 V | | | 0.86 | | 0.3 | 1.4 | | | | |
| V _{OH_S} | | V _I = V _{IH} | | I _{OH} = –100 μA | 1.65 V to 3.6 V | 3 V to 5.5 V | V _{CC_S} – 0.1 | V _{CC_S} – 0.2 | | | V | | | |
| | | | | I _{OH} = –2 mA | 1.65 V | | | | | | | 1.2 | 1.2 | |
| | | | | I _{OH} = –4 mA | 2.3 V | | | | | | | 2 | 2 | |
| | | | | I _{OH} = –6 mA | 2.7 V | | | | | | | 2.3 | 2.3 | |
| | | | | I _{OH} = –12 mA | 3 V | | | | | | | 2.4 | 2.4 | |
| V _{OL_S} | | V _I = V _{IL} | | I _{OL} = 100 μA | 1.65 V to 3.6 V | 3 V to 5.5 V | | | | | V | | | |
| | | | | I _{OL} = 2 mA | 1.65 V | | | | | | | | 0.1 | 0.2 |
| | | | | I _{OL} = 4 mA | 2.3 V | | | | | | | | 0.2 | 0.2 |
| | | | | I _{OL} = 6 mA | 2.7 V | | | | | | | | 0.2 | 0.2 |
| | | | | I _{OL} = 12 mA | 3 V | | | | | | | | 0.3 | 0.3 |
| | | | | | | | | | | | | | | |

(1) V_{CCI} is the V_{CC} associated with the input port.(2) V_{CCO} is the V_{CC} associated with the output port.

Electrical Characteristics⁽¹⁾⁽²⁾ (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC_S} | V _{CC_CF} | T _A = 25°C | | | –40°C to 85°C | | UNIT | |
|--------------------------------|---|--|--------------------|--|-----------------------------|-----|-----------------------------|--|-----|------|-----|
| | | | | | MIN | TYP | MAX | MIN | MAX | | |
| V _{OH_CF} | V _I = V _{IH} | I _{OH} = –100 μA | 1.65 V to 3.6 V | 3 V to 5.5 V | V _{CC_CF} – 0.1 | | V _{CC_CF} – 0.2 | | V | | |
| | | I _{OH} = 12 mA | | 3 V | | | | | | 2.4 | 2.4 |
| | | I _{OH} = 16 mA | | 5.5 V | | | | | | 3.8 | 3.8 |
| V _{OL_CF} | V _I = V _{IL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | 3 V to 5.5 V | | | | 0.1 | 0.2 | | |
| | | I _{OL} = 12 mA | | 3 V | | | | 0.5 | 0.5 | | |
| | | I _{OL} = 16 mA | | 5.5 V | | | | 0.5 | 0.5 | | |
| I _I | Inputs without pullup resistor | V _I = GND to V _{CC1} ⁽³⁾ | 1.65 V to 3.6 V | 3.6 V to 5.5 V | | | | ±0.5 | ±1 | | |
| | Inputs with pullup resistor | V _I = V _{CC1} ⁽³⁾ V _I = 0 V | | 3 V to 5.5 V | | | | ±0.5 | ±1 | | |
| I _{off} | S port | V _I or V _O = 0 to 5.5 V | 0 V | 0 to 5.5 V | | | | ±0.5 | ±1 | | |
| | CF port | | 0 to 3.6 V | 0 V | | | | ±0.5 | ±1 | | |
| I _{OZ} ⁽⁴⁾ | S or CF output ports | V _O = V _{CCO} or GND, V _I = V _{CC1} or GND | 3.6 V | 5.5 V | | | | ±0.5 | ±1 | | |
| | CF outputs | MASTER_EN = don't care | | 0 V | | | | ±0.5 | ±1 | | |
| I _{CC_S} | Inputs (SD15–SD00, SA10–SA00, SCE1, SCE2, SIORD, SIOWR, SOE, SREG, SWE) | V _I = V _{CC_S} or GND | 1.65 V to 3.6 V | 3.6 V to 5.5 V | | | | 1.5 | 3 | | |
| | Control inputs (ENL, ENH, BUF_EN) | ENL = ENH = BUF_EN = V _{CC_S} | | | | | | I _O = 0, ENL = V _{CC_S} , ENH = V _{CC_S} , BUF_EN = V _{CC_S} , DIR(S/CF) = V _{CC_S} | 1.5 | 3 | |
| | | One of ENL, ENH, BUF_EN = GND, Others = V _{CC_S} | | I _O = 0, DIR(S/CF) = V _{CC_S} , All other inputs = V _{CC_S} or GND | 36 | 36 | | | | | |

(1) V_{CC1} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) V_{CC1} = V_{CC_S} for DIR(S/CF), ENL, ENH, SD15–SD00, SA10–SA00, MASTER_EN, SRESET, SCE1, SCE2, SIORD, SIOWR, SOE, SREG, SWE, BUF_EN

V_{CC1} = V_{CC_CF} for D15–D00, BVD1, BVD2, INPACK, READY, WAIT, WP

(4) For I/O ports, the parameter I_{OZ} includes the input leakage current.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | V _{CC_S} | V _{CC_CF} | T _A = 25°C | | | –40°C to 85°C | | UNIT |
|--------------------|--|--|--|-------------------|--------------------|-----------------------|-----|-----|---------------|-----|------|
| | | | | | | MIN | TYP | MAX | MIN | MAX | |
| I _{CC_CF} | Input (D15–D00) | V _I = V _{CC_CF} or GND | I _O = 0, DIR(\overline{S}/CF) = GND, BVD1, BVD2, \overline{INPACK} , READY, \overline{WAIT} , WP = V _{CC_CF} | 1.65 V to 3.6 V | 3 V to 5.5 V | | | 1.5 | | 3 | μA |
| | Inputs (BVD1, BVD2, \overline{INPACK} , READY, \overline{WAIT} , WP) | BVD1 = BVD2 = \overline{INPACK} = V _{CC_CF} , READY, \overline{WAIT} = V _{CC_CF} , WP = V _{CC_CF} | I _O = 0, DIR(\overline{S}/CF) = GND, D15–D00 = V _{CC_CF} or GND | | | | | 1.5 | | 3 | |
| | | One of BVD1, BVD2, \overline{INPACK} , READY, \overline{WAIT} , WP = GND, All others = V _{CC_CF} | I _O = 0, DIR(\overline{S}/CF) = GND, D15–D00 = V _{CC_CF} or GND | | | | | 60 | | 60 | |
| R _{INT} | | | | 1.65 V to 3.6 V | 3 V to 5.5 V | | | 150 | 300 | 300 | kΩ |
| C _I | Control inputs | V _I = 3.3 V or GND | | 3.3 V | 3.3 V | | | 3 | | | pF |
| | S _{Axx} , \overline{SOE} , $\overline{SCE1}$, $\overline{SCE2}$, \overline{SIORD} , \overline{SIOWR} , \overline{SREG} , \overline{SWE} | | | | | | | 3 | | | |
| | A _{xx} , BVD1, BVD2, READY, \overline{INPACK} , \overline{WAIT} , WP | | | | | | | 9 | | | |
| C _{IO} | S I/O ports | V _O = 3.3 V or GND | | 3.3 V | 3.3 V | | | 7 | | | pF |
| | CF I/O ports | | | | | | | 12 | | | |

Switching Characteristics

over recommended operating free-air temperature range ($\overline{CD1}$, $\overline{CD2}$) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC_SD} | $T_A = 25^\circ\text{C}$ | | | $-40^\circ\text{C to } 85^\circ\text{C}$ | | UNIT |
|-----------|--------------------------------------|------------------|----------------------------------|--------------------------|-----|------|--|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| t_{pd} | $\overline{CD1}$ or $\overline{CD2}$ | \overline{SCD} | $1.8\text{ V} \pm 0.15\text{ V}$ | 3.1 | 7.1 | 13.5 | 1.8 | 15.5 | ns |
| | | | $2.5\text{ V} \pm 0.2\text{ V}$ | 2.7 | 4.6 | 7.1 | 1.6 | 9.1 | |
| | | | 2.7 V | 2.4 | 4 | 5.7 | 1.6 | 9.1 | |
| | | | $3.3\text{ V} \pm 0.3\text{ V}$ | 2 | 3.4 | 5.1 | 1.2 | 6.8 | |
| | | | $5\text{ V} \pm 0.5\text{ V}$ | 1.7 | 2.6 | 3.6 | 1 | 5.5 | |

Switching Characteristics

over recommended operating free-air temperature range (BVD1, BVD2, \overline{INPACK} , \overline{READY} , \overline{WAIT} , WP) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V_{CC_S} | V_{CC_CF} | $T_A = 25^\circ\text{C}$ | | | $-40^\circ\text{C to } 85^\circ\text{C}$ | | UNIT | | |
|---------------------------------|---------------------------------|-------------------------------|---|----------------------------------|----------------------------------|----------------------------------|---------------------------------|-------------------------------|--|----------|------|-------------------------------|----------------------------------|
| | | | | | | MIN | TYP | MAX | MIN | MAX | | | |
| t_{pd} | CF input | S output | $\overline{MASTER_EN} = \overline{BUF_EN} = V_{IL}$ | $1.8\text{ V} \pm 0.15\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 3.1 | 6 | 10.2 | 2.4 | 12.9 | ns | | |
| | | | | | | $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 2.9 | 5.6 | 9.6 | | 2.2 | 13.9 |
| | | | | | | | | $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | 2.5 | | 4.2 | 5.8 |
| | | | | | | $3.3\text{ V} \pm 0.3\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | | | 2.5 | | 4 | 5.6 |
| | | | | | | | | $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | 2.3 | | 3.6 | 4.9 |
| | | | | | | t_{en} | $\overline{MASTER_EN}$ | | | S output | | $\overline{BUF_EN} = V_{IL}$ | $1.8\text{ V} \pm 0.15\text{ V}$ |
| $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 11.1 | 19.3 | 30.9 | 8 | | | 35.6 | | | | | |
| | | $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | 9.9 | 12.9 | | | 17.4 | 6.9 | | 22.6 | | |
| $3.3\text{ V} \pm 0.3\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | | | 9.9 | 13.1 | | | 17.4 | 7 | | 22.6 | | |
| | | $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | 9.5 | 11.2 | | | 13.4 | 6.3 | | 18.3 | | |
| $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | | | 9.5 | 11.3 | | | 13.5 | 6.3 | | 18.2 | | |
| | | t_{dis} | $\overline{MASTER_EN}$ | S output | $\overline{BUF_EN} = V_{IL}$ | $1.8\text{ V} \pm 0.15\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 6.8 | 13.7 | 23.9 | 6 | 25.1 | ns |
| $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | | | | | | | 6.1 | 13.4 | 22 | 5.4 | 23.3 | |
| | | | | | | | | $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | 4.9 | 8.6 | 13.3 | |
| $3.3\text{ V} \pm 0.3\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | | | | | | | | | 4.6 | 8.5 | 13.6 | |
| | | | | | | | | $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | 5 | 8.1 | 12.2 | |
| $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | | | | | | | | | 4.5 | 8 | 12.2 | |
| | | t_{en} | $\overline{BUF_EN}$ | S output | $\overline{MASTER_EN} = V_{IL}$ | $1.8\text{ V} \pm 0.15\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 8.7 | 17.7 | 33.2 | 7.6 | 35.5 | ns |
| $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | | | | | | | 10.7 | 18.3 | 29.3 | 8.7 | 35.6 | |
| | | | | | | | | $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | 9.6 | 12.4 | 16.6 | |
| $3.3\text{ V} \pm 0.3\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | | | | | | | | | 9.6 | 12.6 | 16.7 | |
| | | | | | | | | $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | 9.2 | 10.9 | 13 | |
| $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | | | | | | | | | 9.2 | 10.9 | 13 | |
| | | t_{dis} | $\overline{BUF_EN}$ | S output | $\overline{MASTER_EN} = V_{IL}$ | $1.8\text{ V} \pm 0.15\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 6.9 | 12.9 | 22.3 | 5.9 | 24.2 | ns |
| $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | | | | | | | 5.4 | 12.4 | 20.5 | 4.8 | 22.8 | |
| | | | | | | | | $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | 4.4 | 8 | 12.7 | |
| $3.3\text{ V} \pm 0.3\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | | | | | | | | | 4.2 | 7.9 | 12.8 | |
| | | | | | | | | $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | 4.6 | 7.7 | 11.7 | |
| $5\text{ V} \pm 0.5\text{ V}$ | $5\text{ V} \pm 0.5\text{ V}$ | | | | | | | | | 4.1 | 7.6 | 11.7 | |

Switching Characteristics

over recommended operating free-air temperature range (data bus I/Os) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC_S} | V _{CC_CF} | T _A = 25°C | | | –40°C to 85°C | | UNIT |
|------------------|--------------------------------|----------------|---|-------------------|--------------------|-----------------------|------|------|------------------|------|------|
| | | | | | | MIN | TYP | MAX | MIN | MAX | |
| t _{pd} | D | SD | $\overline{\text{MASTER_EN}} =$ $\overline{\text{ENL}} = \overline{\text{ENH}} = V_{\text{IL}}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 4.2 | 7.2 | 11.8 | 3 | 13.7 | ns |
| | | | | | 5 V ± 0.5 V | 3.7 | 6.4 | 10.7 | 2.7 | 13.9 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 3.8 | 5.7 | 8 | 2.4 | 10 | |
| | | | | | 5 V ± 0.5 V | 3.3 | 4.9 | 6.8 | 2.1 | 12.4 | |
| | | | | 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 3.5 | 5.1 | 6.9 | 2.2 | 8.8 | |
| | | | | | 5 V ± 0.5 V | 3 | 4.3 | 5.7 | 1.8 | 7 | |
| | SD | D | | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 3.4 | 5.7 | 9.8 | 2.6 | 11.1 | |
| | | | | | 5 V ± 0.5 V | 3.1 | 5.4 | 9.6 | 2.4 | 9.6 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 2.8 | 4.3 | 6.2 | 1.9 | 8.2 | |
| | | | | | 5 V ± 0.5 V | 2.6 | 3.8 | 5.4 | 1.7 | 7 | |
| | | | | 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 2.5 | 3.7 | 5.2 | 1.5 | 7.2 | |
| | | | | | 5 V ± 0.5 V | 2.2 | 3.3 | 4.5 | 1.4 | 6 | |
| t _{en} | $\overline{\text{MASTER_EN}}$ | D | $\overline{\text{ENL}} = \overline{\text{ENH}} = V_{\text{IL}}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 13.7 | 18.2 | 24.4 | 9.4 | 27.9 | ns |
| | | | | | 5.5 V ± 0.5 V | 13.7 | 17.9 | 29.9 | 8 | 31 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 12.3 | 15.1 | 18.8 | 7.9 | 23 | |
| | | | | | 5.5 V ± 0.5 V | 12.3 | 14.8 | 17.6 | 8 | 21.8 | |
| | | | | 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 11.6 | 14 | 17.1 | 7.3 | 21.4 | |
| | | | | | 5.5 V ± 0.5 V | 11.6 | 13.7 | 15.9 | 7.4 | 20.3 | |
| | SD | D | | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 11.6 | 19.6 | 31.8 | 9.4 | 36.3 | |
| | | | | | 5.5 V ± 0.5 V | 11.7 | 20.1 | 32 | 9.5 | 36.2 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 10.3 | 13.4 | 18 | 7.2 | 22.6 | |
| | | | | | 5.5 V ± 0.5 V | 10.3 | 13.6 | 18.1 | 7.1 | 22.6 | |
| | | | | 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 9.8 | 11.6 | 14 | 6.4 | 18.3 | |
| | | | | | 5.5 V ± 0.5 V | 9.8 | 11.7 | 14 | 6.4 | 18.2 | |
| t _{dis} | $\overline{\text{MASTER_EN}}$ | D | $\overline{\text{ENL}} = \overline{\text{ENH}} = V_{\text{IL}}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 8.6 | 12.8 | 18.1 | 7.3 | 20.2 | ns |
| | | | | | 5.5 V ± 0.5 V | 7.6 | 11.5 | 16.4 | 6.3 | 17.8 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 7.8 | 10.8 | 14.7 | 6.4 | 16.4 | |
| | | | | | 5.5 V ± 0.5 V | 6.7 | 9.4 | 12.6 | 5.4 | 13.8 | |
| | | | | 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 7.2 | 9.9 | 13.4 | 5.9 | 15 | |
| | | | | | 5.5 V ± 0.5 V | 6.1 | 8.6 | 11.4 | 4.8 | 12.5 | |
| | SD | D | | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 6.9 | 12.9 | 21.7 | 6 | 24.2 | |
| | | | | | 5.5 V ± 0.5 V | 6.1 | 12.6 | 20.8 | 5.3 | 22.8 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 4.9 | 7.9 | 11.8 | 4.1 | 14.5 | |
| | | | | | 5.5 V ± 0.5 V | 4.7 | 7.8 | 11.7 | 3.9 | 14.2 | |
| | | | | 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 5 | 7.1 | 9.8 | 4 | 12 | |
| | | | | | 5.5 V ± 0.5 V | 4.7 | 7 | 9.8 | 3.8 | 18.2 | |

Switching Characteristics (continued)

over recommended operating free-air temperature range (data bus I/Os) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC_S} | V _{CC_CF} | T _A = 25°C | | | –40°C to 85°C | | UNIT |
|------------------|--|-------------|--|-------------------|--------------------|-----------------------|------|------|---------------|------|------|
| | | | | | | MIN | TYP | MAX | MIN | MAX | |
| t _{en} | $\overline{\text{ENL}}$ or $\overline{\text{ENH}}$ | D | $\overline{\text{MASTER_EN}} = V_{\text{IL}}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 9.4 | 17.6 | 23.4 | 8.3 | 27.2 | ns |
| | | | | | 5.5 V ± 0.5 V | 13.5 | 17.4 | 22.6 | 7.7 | 27.8 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 12.3 | 15 | 18.5 | 7.9 | 22.8 | |
| | | | | | 5.5 V ± 0.5 V | 12.3 | 14.7 | 17.4 | 8 | 21.6 | |
| | | | | 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 11.7 | 14.1 | 17 | 7.3 | 21.4 | |
| | | | | | 5.5 V ± 0.5 V | 11.6 | 13.7 | 16 | 7.4 | 20.3 | |
| | | SD | | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 9.5 | 18.7 | 30.5 | 9.1 | 35.5 | |
| | | | | | 5.5 V ± 0.5 V | 9.6 | 19.1 | 30.5 | 9.1 | 35.6 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 10 | 13 | 17.4 | 6.8 | 22.6 | |
| | | | | | 5.5 V ± 0.5 V | 10 | 13.2 | 17.4 | 6.8 | 22.6 | |
| | | | | 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 9.6 | 11.3 | 13.6 | 6.2 | 18.3 | |
| | | | | | 5.5 V ± 0.5 V | 9.6 | 11.4 | 13.6 | 6.3 | 18.2 | |
| t _{dis} | $\overline{\text{ENL}}$ or $\overline{\text{ENH}}$ | D | $\overline{\text{MASTER_EN}} = V_{\text{IL}}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 8.5 | 12.1 | 16.8 | 7.2 | 20.2 | ns |
| | | | | | 5.5 V ± 0.5 V | 7.7 | 10.8 | 15 | 6.3 | 16.6 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 7.6 | 10.4 | 13.8 | 6.2 | 16.4 | |
| | | | | | 5.5 V ± 0.5 V | 6.9 | 9.1 | 11.9 | 5.4 | 13.1 | |
| | | | | 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 7.3 | 9.7 | 12.9 | 5.9 | 15 | |
| | | | | | 5.5 V ± 0.5 V | 6.5 | 8.4 | 11 | 5.2 | 12 | |
| | | SD | | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 6.5 | 12 | 20 | 5.7 | 24.2 | |
| | | | | | 5.5 V ± 0.5 V | 5.7 | 11.8 | 19 | 5 | 22.8 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 4.6 | 7.4 | 11.1 | 3.8 | 14.5 | |
| | | | | | 5.5 V ± 0.5 V | 4.4 | 7.3 | 11.1 | 3.7 | 14.2 | |
| | | | | 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 4.9 | 6.8 | 9.3 | 4 | 12 | |
| | | | | | 5.5 V ± 0.5 V | 4.3 | 6.7 | 9.2 | 3.5 | 18.2 | |

Switching Characteristics

over recommended operating free-air temperature range (SA10–SA00, $\overline{\text{SCE1}}$, $\overline{\text{SCE2}}$, $\overline{\text{SIORD}}$, $\overline{\text{SIOWR}}$, $\overline{\text{SOE}}$, $\overline{\text{SREG}}$, $\overline{\text{SWE}}$) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V_{CC_S} | V_{CC_CF} | $T_A = 25^\circ\text{C}$ | | | $-40^\circ\text{C to } 85^\circ\text{C}$ | | UNIT |
|-----------|--------------------------------|----------------------------------|---|---|---------------------------------|--------------------------|------|------|--|------|------|
| | | | | | | MIN | TYP | MAX | MIN | MAX | |
| t_{pd} | S input | CF output (control) | $\overline{\text{MASTER_EN}} = \overline{\text{BUF_EN}} = V_{IL}$ | $1.8\text{ V} \pm 0.15\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 3.4 | 6.1 | 9.8 | 2.5 | 10.4 | ns |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 3 | 5.8 | 9.7 | 2.4 | 10.2 | |
| | | | | $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 2.6 | 4.5 | 6.7 | 1.8 | 8.4 | |
| | | $5\text{ V} \pm 0.5\text{ V}$ | | | 2.4 | 4.1 | 6 | 1.7 | 6.8 | | |
| | | $3.3\text{ V} \pm 0.3\text{ V}$ | | $3.3\text{ V} \pm 0.3\text{ V}$ | 2.2 | 3.9 | 5.8 | 1.4 | 7 | | |
| | | | | $5\text{ V} \pm 0.5\text{ V}$ | 2 | 3.5 | 5 | 1.3 | 5.8 | | |
| | CF output (A pins) | $1.8\text{ V} \pm 0.15\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | $\overline{\text{MASTER_EN}} = \overline{\text{BUF_EN}} = V_{IL}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 3.4 | 5.7 | 8.7 | 2.8 | 10.3 | |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 3.3 | 5.4 | 8.2 | 2.8 | 9.7 | |
| | | $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | | 2.9 | 4.3 | 6.2 | 1.9 | 8.4 | | |
| | | | $5\text{ V} \pm 0.5\text{ V}$ | | 2.7 | 3.9 | 5.4 | 1.9 | 6.8 | | |
| | | $3.3\text{ V} \pm 0.3\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | | 2.6 | 3.7 | 5.2 | 1.7 | 7 | | |
| | | | $5\text{ V} \pm 0.5\text{ V}$ | | 2.3 | 3.3 | 4.4 | 1.5 | 5.8 | | |
| t_{en} | $\overline{\text{MASTER_EN}}$ | CF output (control) | $\overline{\text{BUF_EN}} = V_{IL}$ | $1.8\text{ V} \pm 0.15\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 10.8 | 17.9 | 24.8 | 7.9 | 29.7 | ns |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 10.8 | 17.5 | 26.2 | 8.1 | 30.2 | |
| | | | | $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 9.4 | 14.2 | 19.4 | 6.4 | 23.3 | |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 9.4 | 14.1 | 19.3 | 6.6 | 23.1 | |
| | | | | $3.3\text{ V} \pm 0.3\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 8.7 | 13.1 | 17.8 | 5.8 | 21.4 | |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 8.7 | 13 | 17.5 | 6 | 21.2 | |
| t_{dis} | $\overline{\text{MASTER_EN}}$ | CF output (control) | $\overline{\text{BUF_EN}} = V_{IL}$ | $1.8\text{ V} \pm 0.15\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 7.3 | 13.8 | 22.5 | 6.2 | 25.8 | ns |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 6.8 | 12.1 | 19.7 | 5.9 | 26.3 | |
| | | | | $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 6.1 | 11.8 | 19.2 | 4.9 | 20.2 | |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 5.9 | 10 | 16.3 | 4.6 | 19.8 | |
| | | | | $3.3\text{ V} \pm 0.3\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 5.6 | 11 | 18.3 | 4.6 | 19.1 | |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 5.4 | 9.2 | 15.5 | 3.9 | 18 | |
| t_{en} | $\overline{\text{BUF_EN}}$ | CF output (A pins) | $\overline{\text{MASTER_EN}} = V_{IL}$ | $1.8\text{ V} \pm 0.15\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 12.9 | 17.5 | 23.7 | 7.7 | 29.7 | ns |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 13.3 | 17.8 | 24.4 | 9.4 | 30.2 | |
| | | | | $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 11.7 | 14.4 | 17.9 | 7.5 | 23.3 | |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 11.8 | 14.3 | 17.1 | 7.7 | 23.1 | |
| | | | | $3.3\text{ V} \pm 0.3\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 11 | 13.3 | 16.2 | 6.9 | 21.4 | |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 11.1 | 13.2 | 15.3 | 6.5 | 21.2 | |
| t_{dis} | $\overline{\text{BUF_EN}}$ | CF output (A pins) | $\overline{\text{MASTER_EN}} = V_{IL}$ | $1.8\text{ V} \pm 0.15\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 8.9 | 13.6 | 19.7 | 7.5 | 25.8 | ns |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 7.6 | 11.8 | 17.1 | 6.6 | 26.3 | |
| | | | | $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 8 | 11.6 | 16 | 6.6 | 20.1 | |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 6.7 | 9.7 | 13.2 | 5 | 19.8 | |
| | | | | $3.3\text{ V} \pm 0.3\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 7.7 | 10.6 | 14.7 | 6 | 18.2 | |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 6.1 | 8.9 | 11.9 | 4.9 | 18 | |
| t_{en} | $\overline{\text{BUF_EN}}$ | CF output (A pins) | $\overline{\text{MASTER_EN}} = V_{IL}$ | $1.8\text{ V} \pm 0.15\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 12.3 | 16.4 | 21.9 | 7.7 | 27.2 | ns |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 12.6 | 16.7 | 22.6 | 8.6 | 29.1 | |
| | | | | $2.5\text{ V} \pm 0.2\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 11.2 | 13.8 | 17 | 7.1 | 21.7 | |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 11.4 | 13.7 | 16.3 | 7.3 | 21.5 | |
| | | | | $3.3\text{ V} \pm 0.3\text{ V}$ | $3.3\text{ V} \pm 0.3\text{ V}$ | 10.7 | 12.9 | 15.6 | 6.7 | 19.5 | |
| | | | | | $5\text{ V} \pm 0.5\text{ V}$ | 10.8 | 12.8 | 14.8 | 6.5 | 19.6 | |

Switching Characteristics (continued)

over recommended operating free-air temperature range (SA10–SA00, SCE1, SCE2, SIORD, SIOWR, SOE, SREG, SWE)
(see Figure 1)

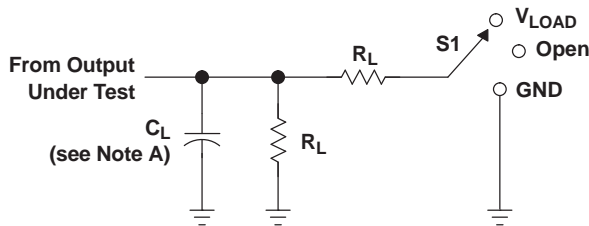
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC_S} | V _{CC_CF} | T _A = 25°C | | | –40°C to 85°C | | UNIT |
|------------------|--------------------------------|--------------------|---|-------------------|--------------------|-----------------------|------|------|---------------|------|------|
| | | | | | | MIN | TYP | MAX | MIN | MAX | |
| t _{dis} | $\overline{\text{BUF_EN}}$ | CF output (A pins) | $\overline{\text{MASTER_EN}} = V_{IL}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 8.4 | 13.9 | 21.2 | 7.2 | 23.2 | ns |
| | | | | | 5 V ± 0.5 V | 7.6 | 12.3 | 18.5 | 6.6 | 23.7 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 7.7 | 12.3 | 18.2 | 6.4 | 19.8 | |
| | | | | | 5 V ± 0.5 V | 6.7 | 10.6 | 15.3 | 5 | 18.4 | |
| 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 7.2 | 11.5 | 16.4 | 5.9 | 18 | | | | | |
| | 5 V ± 0.5 V | 6.4 | 10 | 14.3 | 4.9 | 17 | | | | | |
| t _{en} | $\overline{\text{BUF_EN}}$ | CF output | $\overline{\text{MASTER_EN}} = V_{IL}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 12.5 | 16.6 | 22.3 | 8.7 | 27.2 | ns |
| | | | | | 5 V ± 0.5 V | 12.8 | 17 | 23.1 | 8.8 | 29.1 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 11.4 | 14.1 | 17.5 | 7.3 | 21.7 | |
| | | | | | 5 V ± 0.5 V | 11.6 | 14 | 16.9 | 7.4 | 21.5 | |
| 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 10.9 | 13.2 | 16 | 6.8 | 20 | | | | | |
| | 5 V ± 0.5 V | 11 | 13.1 | 15.3 | 6.5 | 19.6 | | | | | |
| t _{dis} | $\overline{\text{BUF_EN}}$ | CF output | $\overline{\text{MASTER_EN}} = V_{IL}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 8.6 | 13.9 | 21.5 | 7.4 | 23.2 | ns |
| | | | | | 5 V ± 0.5 V | 7.7 | 12.1 | 19.8 | 6.6 | 23.7 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 7.9 | 12.3 | 18.5 | 6.5 | 19.8 | |
| | | | | | 5 V ± 0.5 V | 6.6 | 10.4 | 17.1 | 5 | 18.4 | |
| 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 7.4 | 11.7 | 17.5 | 6.1 | 18.9 | | | | | |
| | 5 V ± 0.5 V | 6.1 | 9.7 | 16.2 | 4.9 | 17 | | | | | |
| t _{en} | $\overline{\text{MASTER_EN}}$ | DIR_OUT | $\overline{\text{BUF_EN}} = V_{IL}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 6.1 | 14.2 | 29.6 | 4.9 | 32.8 | ns |
| | | | | | 5 V ± 0.5 V | 6 | 14.2 | 30 | 4.9 | 33.2 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 4.8 | 8.8 | 15.4 | 3.4 | 19.3 | |
| | | | | | 5 V ± 0.5 V | 4.8 | 8.8 | 15.5 | 3.4 | 19.3 | |
| 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 4.2 | 6.9 | 11.1 | 2.7 | 14.4 | | | | | |
| | 5 V ± 0.5 V | 4.2 | 6.9 | 11.1 | 2.6 | 14.4 | | | | | |
| t _{dis} | $\overline{\text{MASTER_EN}}$ | DIR_OUT | $\overline{\text{BUF_EN}} = V_{IL}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 5.4 | 10 | 16.6 | 4.2 | 32.6 | ns |
| | | | | | 5 V ± 0.5 V | 5.4 | 9.9 | 16.1 | 4.8 | 32.6 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 3.9 | 6.5 | 10.5 | 1.5 | 19.3 | |
| | | | | | 5 V ± 0.5 V | 3.9 | 6.6 | 10.4 | 1.7 | 19.3 | |
| 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 4.4 | 6.7 | 10.3 | 1.4 | 14.4 | | | | | |
| | 5 V ± 0.5 V | 4.3 | 6.7 | 10.1 | 1.5 | 14.4 | | | | | |
| t _{pd} | SIORD or SOE | DIR_OUT | $\overline{\text{BUF_EN}} = V_{IL}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 5 | 9.3 | 15.7 | 4 | 17.9 | ns |
| | | | | | 5 V ± 0.5 V | 5 | 9.3 | 15.7 | 4 | 17.9 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 3.9 | 6 | 8.5 | 2.8 | 11 | |
| | | | | | 5 V ± 0.5 V | 3.9 | 6 | 8.5 | 2.8 | 11 | |
| 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 3.3 | 4.7 | 6.2 | 2.2 | 8.2 | | | | | |
| | 5 V ± 0.5 V | 3.3 | 4.7 | 6.2 | 2.2 | 8.2 | | | | | |
| t _{pd} | $\overline{\text{BUF_EN}}$ | DIR_OUT | $\overline{\text{BUF_EN}} = V_{IL}$ | 1.8 V ± 0.15 V | 3.3 V ± 0.3 V | 8.9 | 19.5 | 35.9 | 7.1 | 39.2 | ns |
| | | | | | 5 V ± 0.5 V | 8.9 | 19.5 | 35.8 | 7 | 39.3 | |
| | | | | 2.5 V ± 0.2 V | 3.3 V ± 0.3 V | 6.8 | 11.9 | 19.1 | 5 | 22.8 | |
| | | | | | 5 V ± 0.5 V | 6.8 | 11.9 | 19.2 | 4.9 | 22.8 | |
| 3.3 V ± 0.3 V | 3.3 V ± 0.3 V | 5.8 | 9 | 13.3 | 4 | 15.8 | | | | | |
| | 5 V ± 0.5 V | 5.8 | 9 | 13.3 | 3.9 | 15.9 | | | | | |

Operating Characteristics

 V_{CCS} and $V_{CC_CF} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|------------|---|-----------------------------------|------------------|---------------------------------|------|
| C_{pds} | Power dissipation capacitance per transceiver | System-port input, CF-port output | Outputs enabled | $C_L = 0$, $f = 10\text{ MHz}$ | pF |
| | | | Outputs disabled | | |
| | CF-port input, system-port output | Outputs enabled | | | |
| | | Outputs disabled | | | |
| C_{pdCF} | Power dissipation capacitance per transceiver | System-port input, CF-port output | Outputs enabled | $C_L = 0$, $f = 10\text{ MHz}$ | pF |
| | | | Outputs disabled | | |
| | CF-port input, system-port output | Outputs enabled | | | |
| | | Outputs disabled | | | |

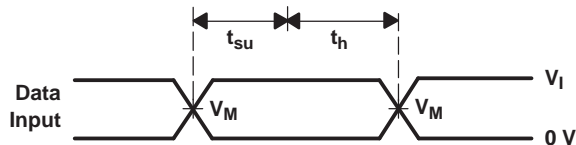
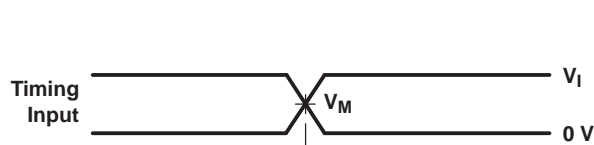
PARAMETER MEASUREMENT INFORMATION



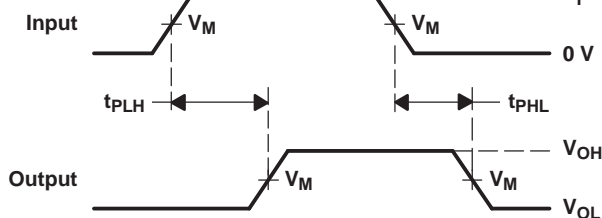
| TEST | S1 |
|-------------------|------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PHZ} | GND |

LOAD CIRCUIT

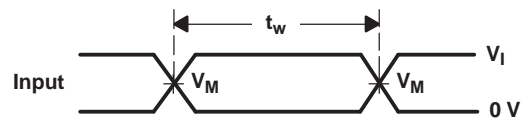
| V_{CC} | INPUT | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 2 k Ω | 0.15 V |
| $2.5 \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 2 k Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 2 k Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 2 k Ω | 0.3 V |
| $5.5\text{ V} \pm 0.5\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 2 k Ω | 0.5 V |



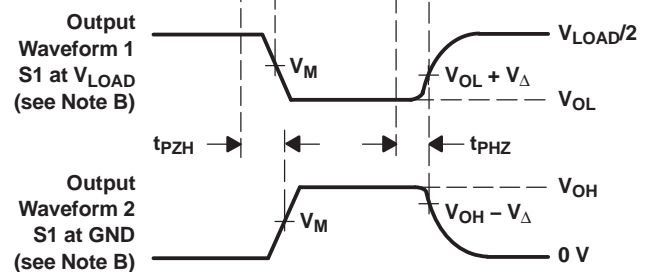
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_0 = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|-------------------|-----------------|------|-------------|----------------------------|------------------|------------------------------|
| CF4320HGKFR | NRND | BGA MI CROSTAR | GKF | 114 | 1000 | TBD | SNPB | Level-2-235C-1 YEAR |
| CF4320HZKFR | ACTIVE | LFBGA | ZKF | 114 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|---------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CF4320HGKFR | BGA MICROSTAR | GKF | 114 | 1000 | 330.0 | 24.4 | 5.8 | 16.3 | 1.8 | 8.0 | 24.0 | Q1 |
| CF4320HZKFR | LFBGA | ZKF | 114 | 1000 | 330.0 | 24.4 | 5.8 | 16.3 | 1.8 | 8.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

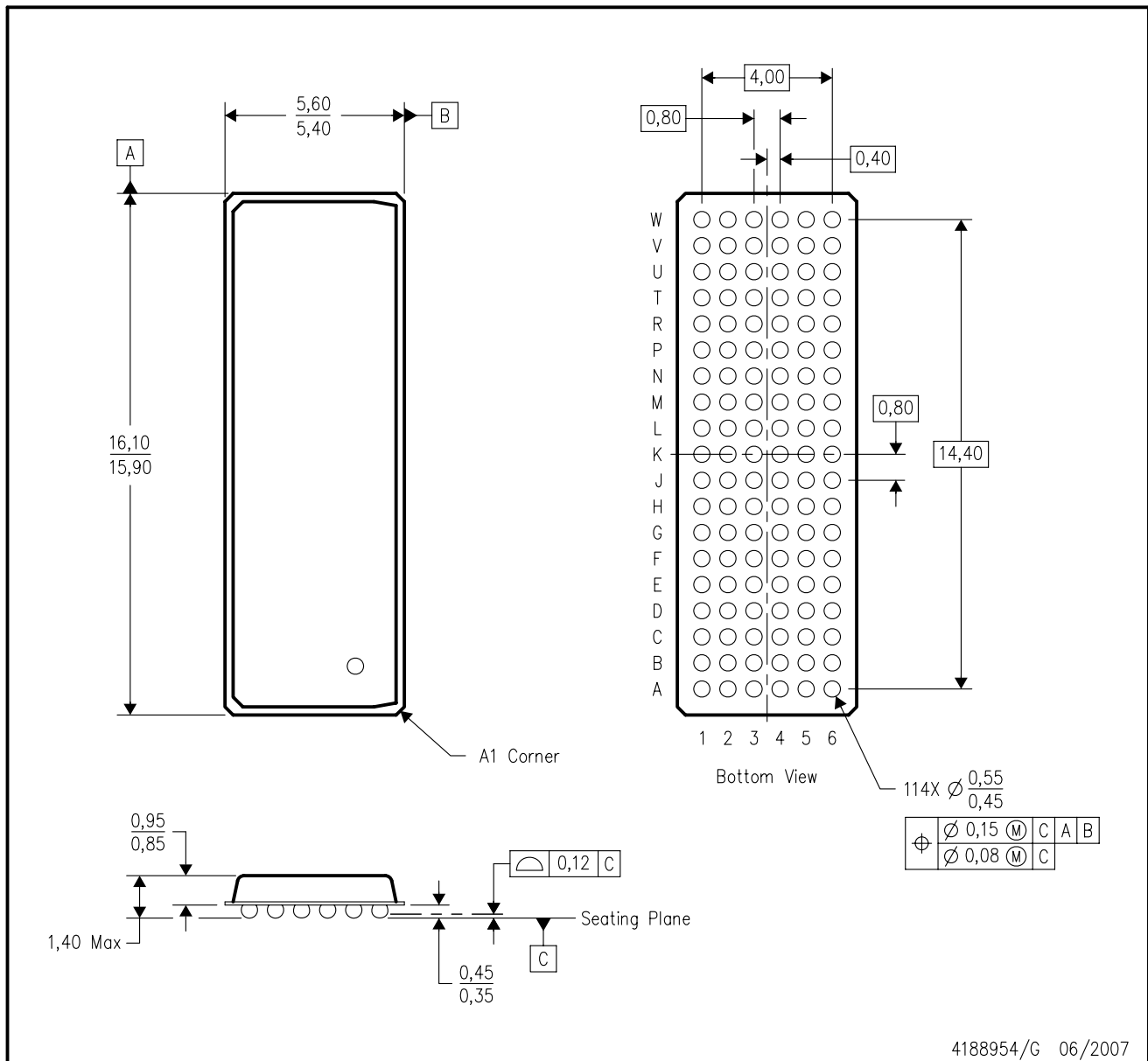


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|---------------|-----------------|------|------|-------------|------------|-------------|
| CF4320HGKFR | BGA MICROSTAR | GKF | 114 | 1000 | 333.2 | 345.9 | 31.8 |
| CF4320HZKFR | LFBGA | ZKF | 114 | 1000 | 333.2 | 345.9 | 31.8 |

GKF (R-PBGA-N114)

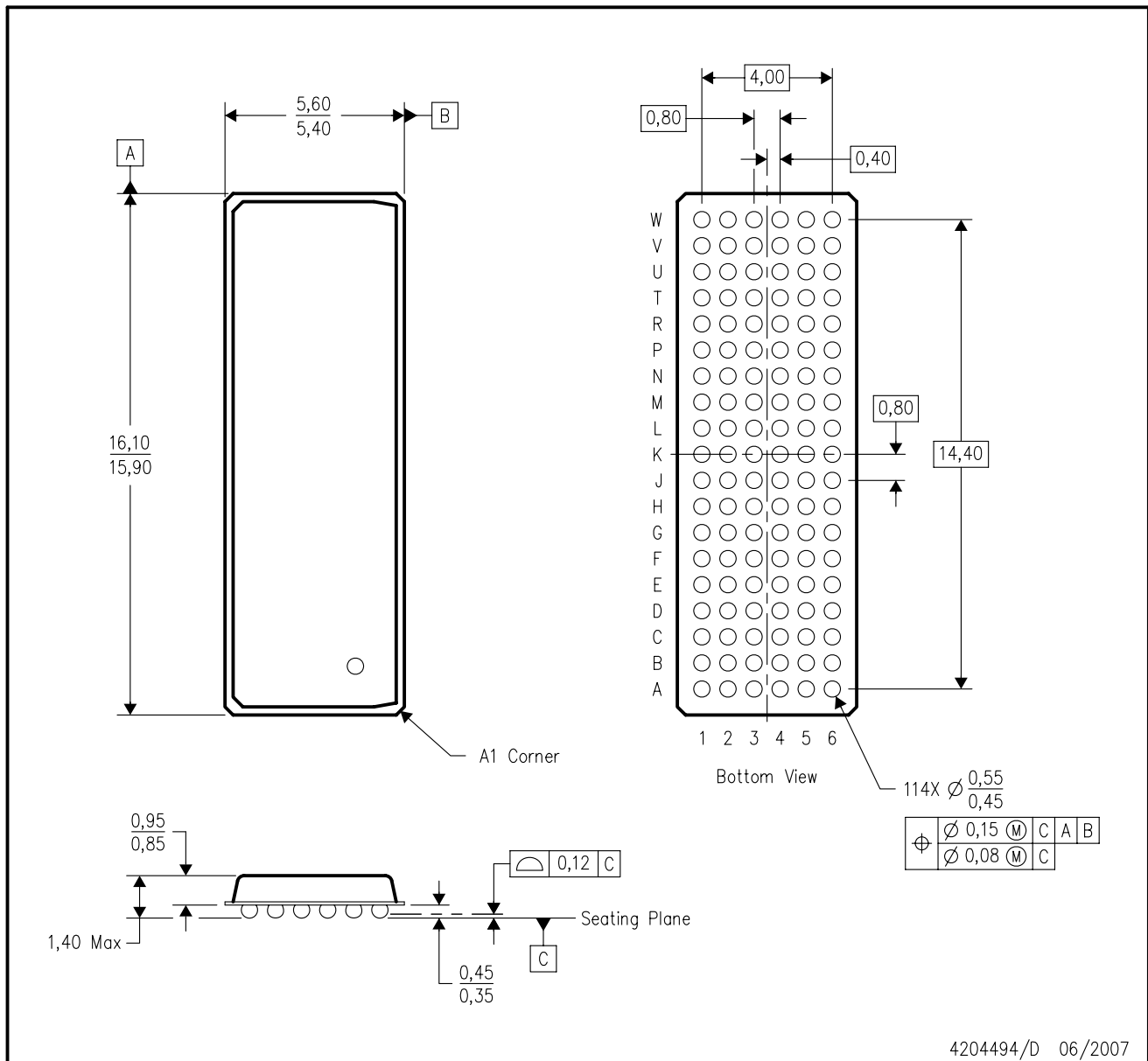
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation DC.
 - D. This package is tin-lead (SnPb). Refer to the 114 ZKF package (drawing 4204494) for lead-free.

ZKF (R-PBGA-N114)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation DC.
 - D. This package is lead-free. Refer to the 114 GKF package (drawing 4188954) for tin-lead (SnPb).

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