CLC409 Very Wideband, Low Distortion Monolithic Op Amp

Check for Samples: CLC409

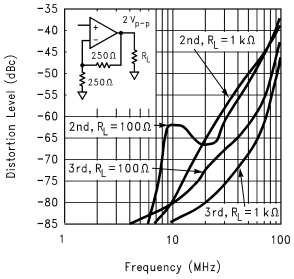
FEATURES

- **350MHz small signal bandwidth**
- **-65/−72dBc 2nd/3rd harmonics (20MHz)**
- **Low noise**
- **8ns settling to 0.1%**
- **1200V/µs slew rate**
- **13.5mA supply current (±5V)**
- **60mA output current**

APPLICATIONS

- **Flash A/D driver**
- **D/A transimpedance buffer**
- **Wide dynamic range IF amp**
- **Radar/communication receivers**
- **DDS post-amps**
- **Wideband inverting summer**
- **Line driver**

Figure 1. Harmonic Distortion vs. Load and Frequency



DESCRIPTION

The CLC409 is a very wideband, DC coupled monolithic operational amplifier designed specifically for wide dynamic range systems requiring exceptional signal fidelity. Benefiting from National's current feedback architecture, the CLC409 offers a gain range of ±1 to ±10 while providing stable, oscillation free operation without external compensation, even at unity gain.

With its 350MHz small signal bandwidth (V_{OUT} = $2V_{PP}$), 10-bit distortion levels through 20MHz (R_L = 100Ω), 8-bit distortion levels through 60MHz, 2.2nV/$\sqrt{Hz}$ input referred noise and 13.5mA supply current, the CLC409 is the ideal driver or buffer for high speed flash A/D and D/A converters.

Wide dynamic range systems such as radar and communication receivers requiring a wideband amplifier offering exceptional signal purity will find the CLC409's low input referred noise and low harmonic and intermodulation distortion make it an attractive high speed solution.

Constructed using an advanced, complimentary bipolar process and **National's** proven current feedback architecture, the CLC409 is available in several versions to meet a variety of requirements.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-92034

Space level versions also available.

For more information, visit http://www.national.com/mil

Connection Diagram

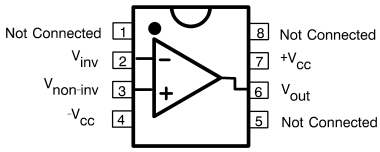


Figure 2. Pinout
DIP & SOIC

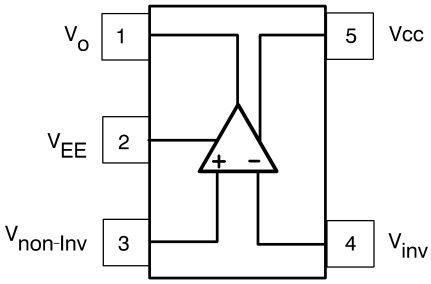


Figure 3. Pinout
SOT23-5

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	±7V
I_{OUT} Output is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed...	60mA
Common Mode Input Voltage	±V_{CC}
Differential Input Voltage	10V
Junction Temperature	+150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Solder Duration (+300°C)	10 sec
ESD rating (human body model)	1000V

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

Operating Ratings

Thermal Resistance		
Package	(θ_{JC})	(θ_{JA})
MDIP	95°C/W	115°C/W
SOIC	75°C/W	160°C/W
SOT23-5	115°C/W	185°C/W

Electrical Characteristics

A_V = +2, V_{CC} = ± 5V, R_L = 100Ω, R_f = 250Ω; unless specified

Symbol	Parameter	Conditions	Typ	Max/Min (1)			Units
Ambient Temperature		CLC409AJ	+25°C	−40°C	+25°C	+85°C	
Frequency Domain Performance							
SSBW	-3dB Bandwidth	V_{OUT} <2V_{PP}	350	>250	>250	>200	MHz
LSBW		V_{OUT} <5V_{PP}	110	>90	>90	>80	MHz
	Gain Flatness	V_{OUT} < 0.5V_{PP}					
GFPL	Peaking	DC to 75MHz	0	<0.4	<0.4	<0.4	dB
GFPH	Peaking	>75MHz	0	<0.8	<0.8	<0.8	dB
GFR1	Rolloff	DC to 125MHz	0.2	<1.0	<1.0	<1.0	dB
GFR2	Rolloff	@ 200MHz	1.0	<2.0	<2.2	<3.0	dB
LPD	Linear Phase Deviation	DC to 100MHz	0.3	<0.8	<0.8	<1.0	deg
DG1	Differential Gain	R_L =150Ω, 3.58MHz	0.03	<0.07	<0.06	<0.06	%
DG2		R_L =150Ω, 4.43MHz	0.03	<0.07	<0.06	<0.06	%
DP1	Differential Phase	R_L = 150Ω, 3.58MHz	0.01	<0.02	<0.02	<0.02	deg
DP2		R_L =150Ω, 4.43MHz	0.01	<0.02	<0.02	<0.02	deg
Time Domain Response							
TRS	Rise and Fall Time	2V Step	1.3	<1.6	<1.6	<1.6	ns
TRL		5V Step	3.5	<4.2	<4.2	<4.6	ns
TS	Settling Time to ±0.1%	2V Step	8	<12	<12	<12	ns
OS	Overshoot	2V Step	5	<15	<18	<18	%
SR	Slew Rate		1200	>1000	>1000	>1000	V/µs
Distortion And Noise Response							
HD2L	2nd Harmonic Distortion	2V_{PP}, 5MHz	−86	<−78	<−81	<−81	dBc
HD2		2V_{PP}, 20MHz	−65	<−56	<−56	<−56	dBc
HD2H		2V_{PP}, 60MHz	−49	<−41	<−44	<−44	dBc
HD3L	3rd Harmonic Distortion	2V_{PP}, 5MHz	−84	<−76	<−76	<−76	dBc
HD3		2V_{PP}, 20MHz	−72	<−65	<−65	<−65	dBc
HD3H		2V_{PP}, 60MHz	−59	<−52	<−52	<−52	dBc
	Equivalent Input Noise						
VN	Non-Inverting Voltage	>1MHz	2.2	<2.8	<2.8	<3.1	nV/$\sqrt{Hz}$
ICN	Inverting Current	>1MHz	14.3	<18	<18	<20	pA/$\sqrt{Hz}$
NCN	Non-Inverting Current	>1MHz	3.2	<4.0	<4.0	<4.5	pA/$\sqrt{Hz}$
SNF	Total Noise Floor	>1MHz	−157	<−155	<−155	<−154	dBm_{1Hz}
INV	Total Integrated Noise	1MHz to 150MHz	38	<47	<47	<52	µV
Static, DC Performance							
VIO	Input Offset Voltage (2)		0.5	<8.5	<4.5	<9.5	mV
DVIO	Average Temperature Coefficient		25	<50	-	<50	µV/°C
IBN	Input Bias Current (2)	Non Inverting	10	<44	<22	<22	µA
DIBN	Average Temperature Coefficient		100	<275	-	<125	nA/°C
IBI	Input Bias Current (2)	Inverting	10	<36	<20	<30	µA
DIBI	Average Temperature Coefficient		100	<200	-	<100	nA/°C
PSRR	Power Supply Rejection Ratio		50	>45	>45	>45	dB
CMRR	Common Mode Rejection Ratio		50	>45	>45	>45	dB
ICC	Supply Current (2)	No Load	13.5	<14.2	<14.2	<14.2	mA

(1) Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.
(2) AJ-level: spec. is 100% tested at +25°C.

Electrical Characteristics (continued)

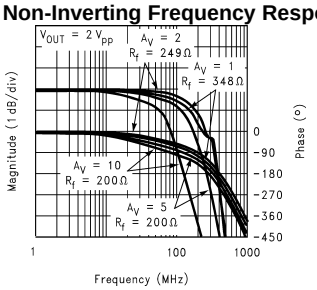
A_V = +2, V_{CC} = ± 5V, R_L = 100Ω, R_f = 250Ω; unless specified

Symbol	Parameter	Conditions	Typ	Max/Min (1)			Units
Miscellaneous Performance							
RIN	Non-Inverting Input Resistance		1000	>250	>500	>1000	kΩ
CIN	Non-Inverting Input Capacitance		1	<2	<2	<2	pF
RO	Output Impedance	DC	0.1	<0.3	<0.2	<0.2	Ω
VO	Output Voltage Range	R_L = 100Ω	±3.5	>±3.0	>±3.2	>±3.2	V
CMIR	Common Mode Input Range		±2.2	±1.5	±2.0	±2.0	V
IO	Output Current		60	36	50	50	mA

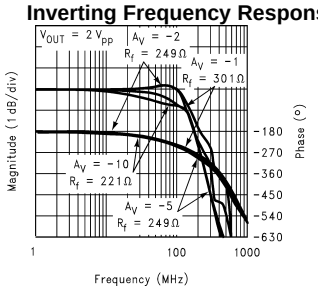
Typical Performance Characteristics

(T_A = 25°C, A_V = +6, V_{CC} = ±5V, R_L = 100Ω, R_f = 500Ω; Unless Specified).

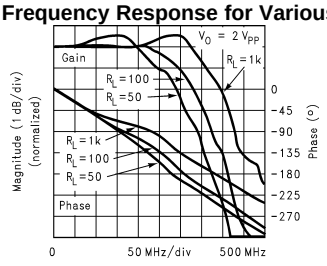
Non-Inverting Frequency Response



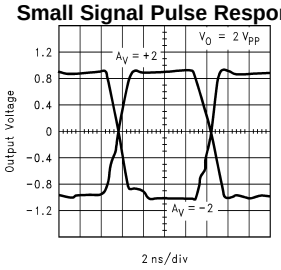
Inverting Frequency Response



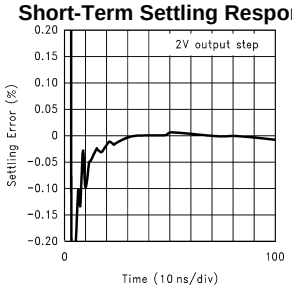
Frequency Response for Various R_LS



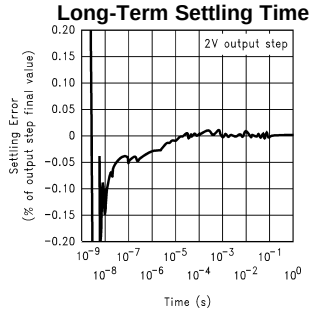
Small Signal Pulse Response



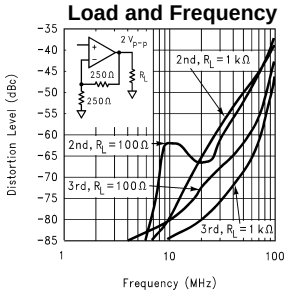
Short-Term Settling Response



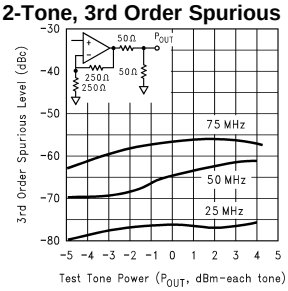
Long-Term Settling Time



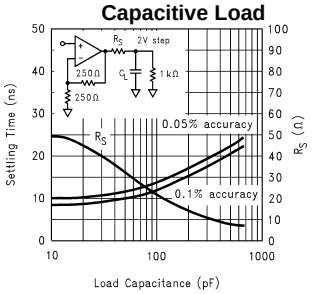
Harmonic Distortion vs. Load and Frequency



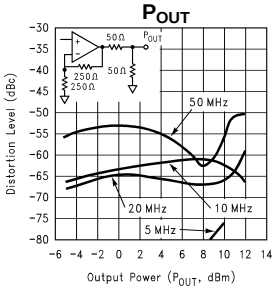
2-Tone, 3rd Order Spurious Levels



Settling Time vs. Capacitive Load



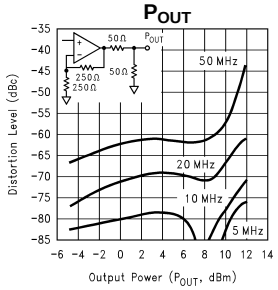
2nd Harmonic Distortion vs. P_{OUT}



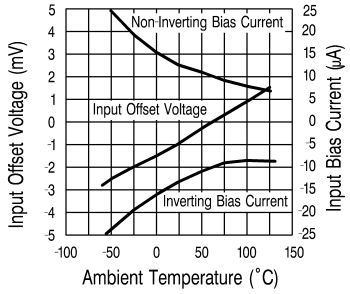
Typical Performance Characteristics (continued)

(T_A = 25°C, A_V = +6, V_{CC} = ±5V, R_L = 100Ω, R_f = 500Ω; Unless Specified).

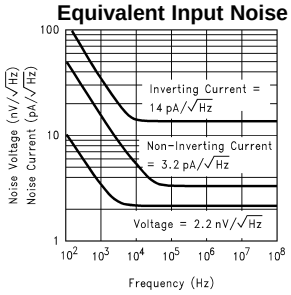
3rd Harmonic Distortion vs. P_{OUT}



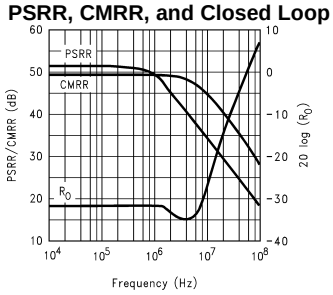
Typical D.C. Errors vs. Temperature



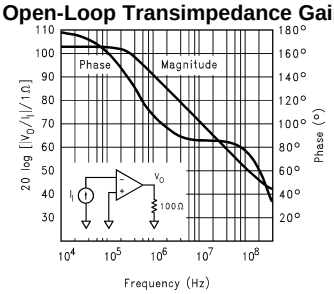
Equivalent Input Noise



PSRR, CMRR, and Closed Loop R_O



Open-Loop Transimpedance Gain, Z(s)



Application Division

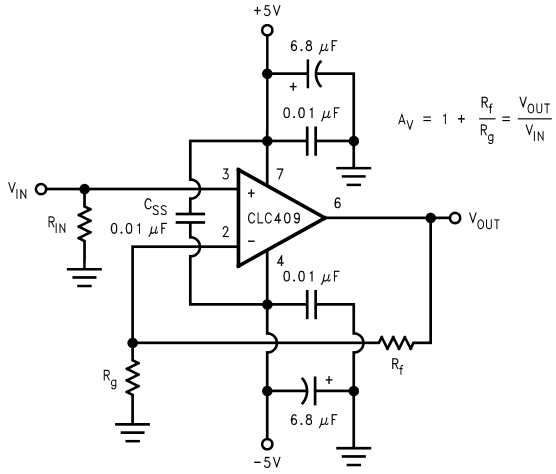


Figure 4. Recommended Non-Inverting Gain Circuit

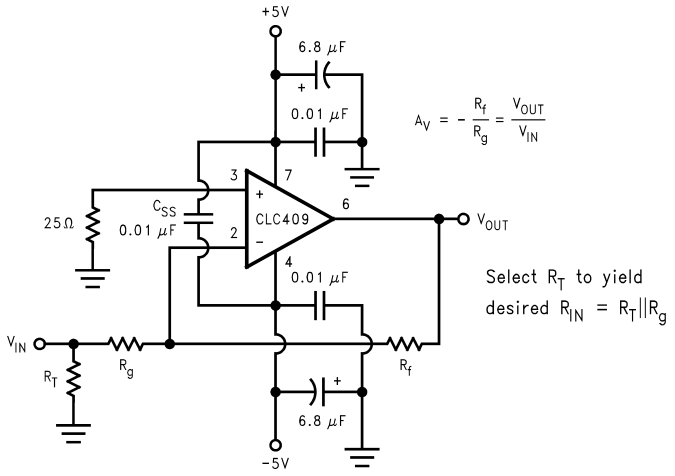


Figure 5. Recommended Inverting Gain Circuit

Feedback Resistor

The CLC409 achieves its excellent pulse and distortion performance by using the current feedback topology pioneered by Comlinear Corporation. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The CLC409 is optimized for use with a 250Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 discusses this in detail along with the occasions where a different R_f might be advantageous.

Harmonic Distortion

The CLC409 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high speed flash ADCs, the distortions introduced by the converter will dominate over the low CLC409 distortions shown on the plots on the previous page. The 0.01µF capacitor (C_{SS}) shown across the supplies in Figure 4 and Figure 5 is critical to achieving the lowest 2nd harmonic distortion.

The 2-tone, 3rd order spurious plot shows a relatively constant difference between the test power level and the spurious level with that difference depending on frequency. The CLC409 does not show an intercept type performance. (where the relative spurious levels change at a 2X rate vs. the test tone powers), due to an internal full power bandwidth enhancement circuit that boosts the performance as the output swing increases while dissipating negligible quiescent power under low output power conditions. This feature enhances the distortion performance and full power bandwidth to match that of much higher quiescent supply current parts.

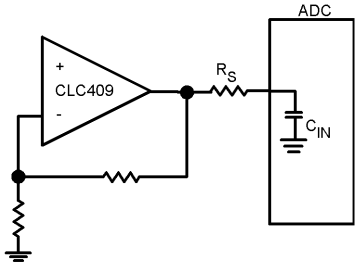


Figure 6. Input Amplifier to ADC

Figure 6 shows a typical application using the CLC409 to drive an ADC. The series resistor, R_S, between the amplifier output and the ADC input is critical to achieving best system performance. This load capacitance, if applied directly to the output pin, can quickly lead to unacceptable levels of ringing in the pulse response. The plot of R_S and settling time vs. C_L on the previous page is an excellent starting point for setting R_S. The value derived in that plot minimizes the step settling time into a fixed discrete capacitive load. Several additional constraints should be considered, however, in driving the capacitive input or an ADC.

There is an option to increase R_S, bandlimiting at the ADC input for either noise or Nyquist bandlimiting purposes. Increasing R_S too much, however, can induce an unacceptably large input glitch due to switching transients coupling through from the convert signal. Also, C_{in} is oftentimes a voltage dependent capacitance. This input impedance non-linearity will induce distortion terms that will increase as R_S is increased. Only slight adjustments up or down from the recommended R_S value should therefore be attempted in optimizing system performance.

DC Accuracy and Noise

The CLC409 offers an improved offset voltage over the pin compatible CLC400 low gain amplifier. The offset adjustment available on the CLC400 was therefore not included in this part. The Output Offset equation below shows the output offset computation equation for the non-inverting configuration with an example using the typical bias current and offset specifications for A_V = +2.

Output Offset

$V_O=(\pm I_{bn}R_{in}\pm V_{io})(1+R_f/R_g)\pm I_{bi}R_f$

Example Computation for A_V=+2, R_f=250Ω, R_{in}=25Ω:

$V_O=(\pm 10\mu A\ (25\Omega)\pm 0.5mV)2\pm 10\mu A\ (250\Omega)=\pm 3.25mV$

This low output offset voltage is a marked improvement over earlier very high speed amplifiers. Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-7.

The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. It is not possible, therefore, to cancel their effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices).

The total output noise is computed in a similar fashion to output offset voltage. Using the input noise voltage and two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See Application Note OA-12 for a full discussion of noise calculations for current feedback amplifiers.

Printed Circuit Layout

As with any high speed component, a careful attention to the board layout is necessary for optimum performance. Evaluation PC boards (CLC730013-DIP, CLC730027-SOIC, and CLC730068-SOT) for the CLC409 are available. This additional supply bypassing capacitor, C_{ss}, can easily be added to the board if desired. Further layout suggestions can be found in Application Note OA-15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265