SONY

CXA1845Q

I²C Bus-Compatible Audio/Video Switch

Description

The CXA1845Q is a 7-input, 3-output audio/video switch featuring I²C bus compatibility for TVs.

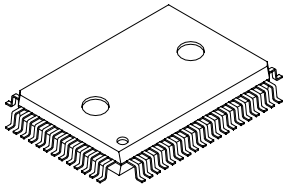
Features

- Serial control with I²C bus
- 7 inputs, 3 outputs
- Desired inputs can each be independently selected for 3 outputs
- Separate control of video and audio switches
- 6 dB amplifiers for both video and audio outputs
- Wideband video amplifier (20 MHz, –3 dB)
- Y/C mixer circuit
- Slave address can be changed (90H/92H)
- Audio muting from external pin
- High impedance maintained by I²C bus line (SDA, SCL) even when power is OFF.
- Wide audio dynamic range (3 Vrms typ.)

Applications

Audio/video switch featuring I²C bus compatibility for TVs.

64 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1000	mW

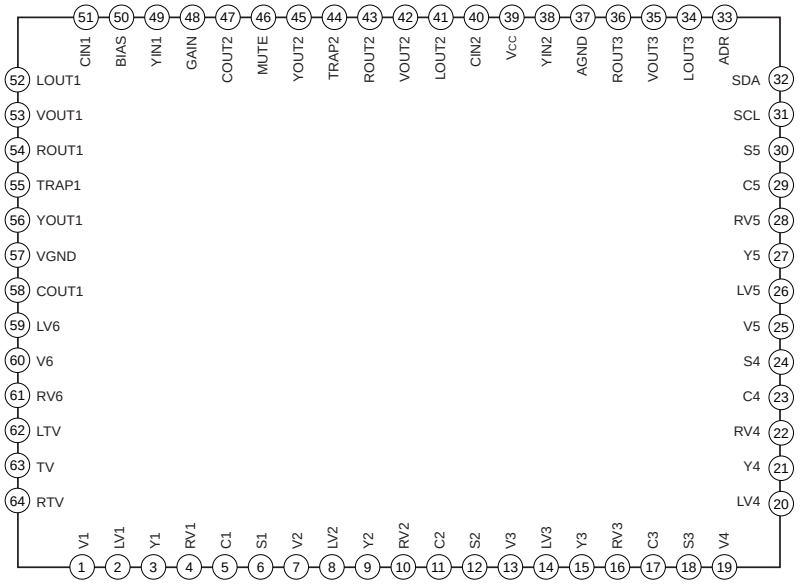
Operating Conditions

Supply voltage	V_{CC}	9±0.5	V

Structure

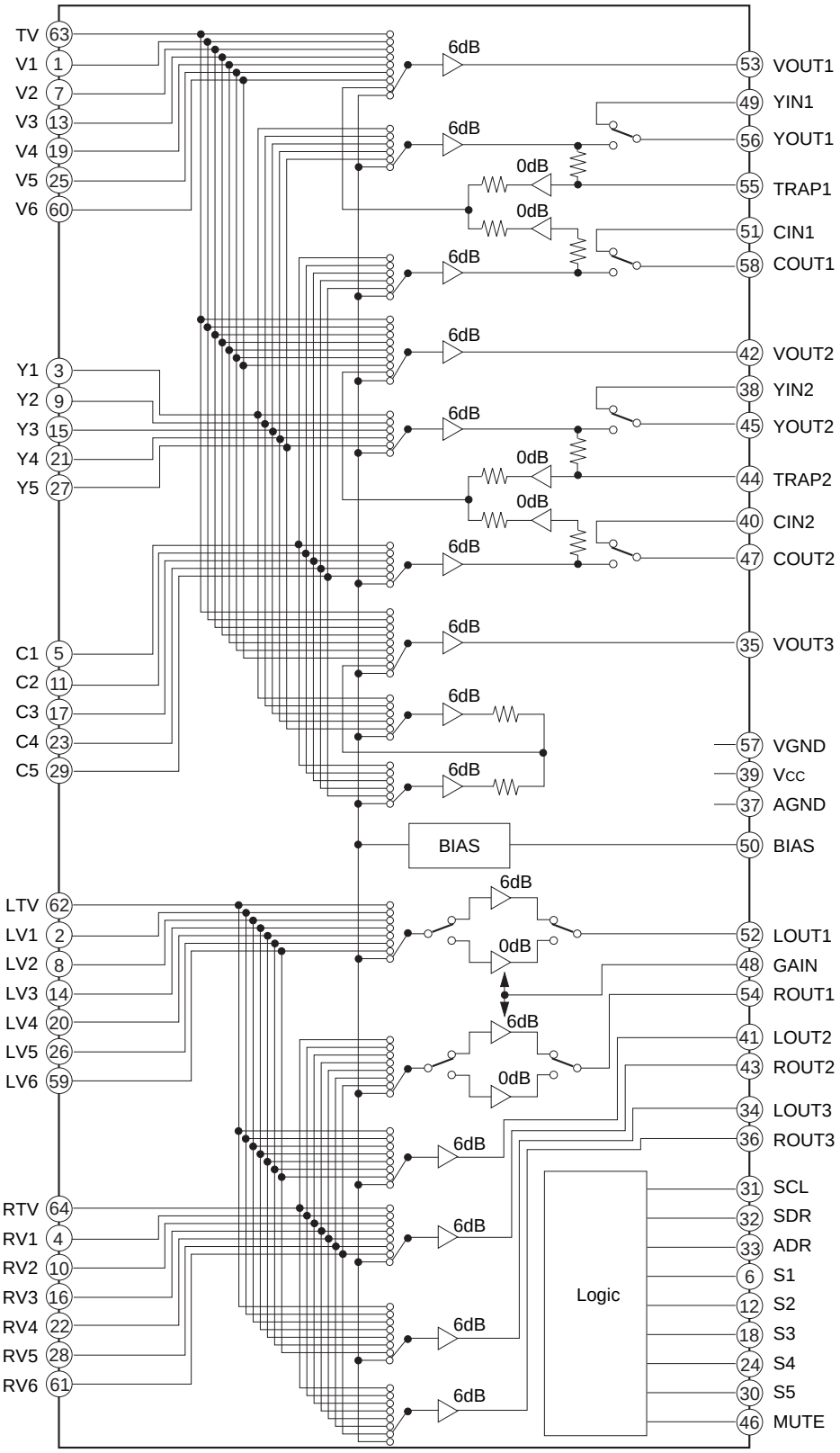
Bipolar silicon monolithic IC

Pin Configuration (Top View)



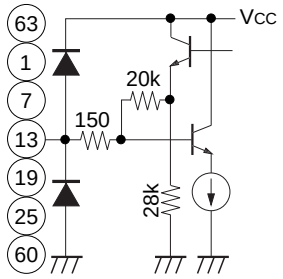
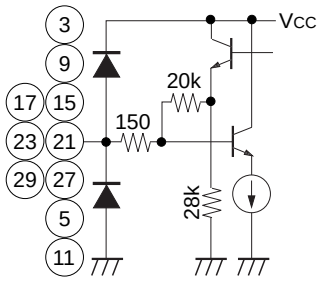
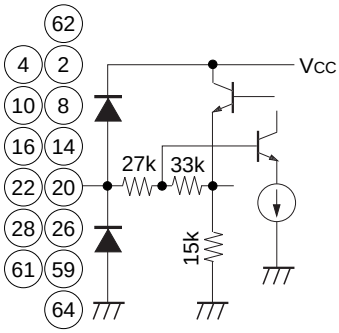
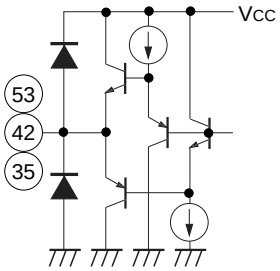
E93408C79-TE

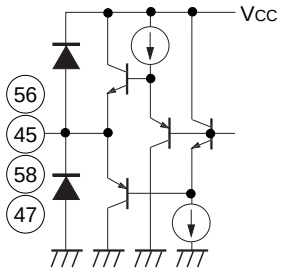
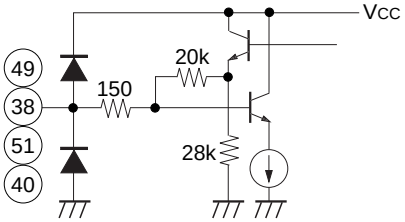
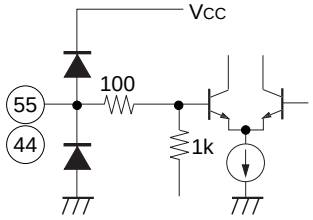
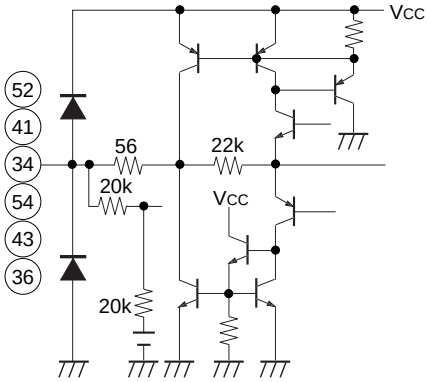
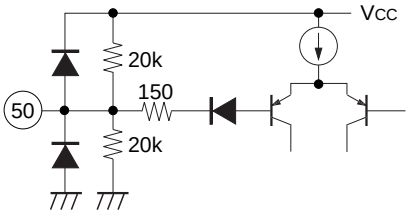
Block Diagram

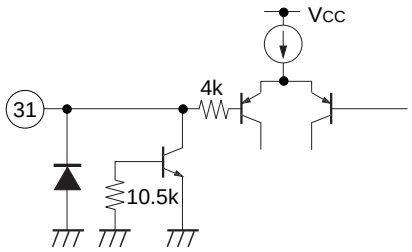
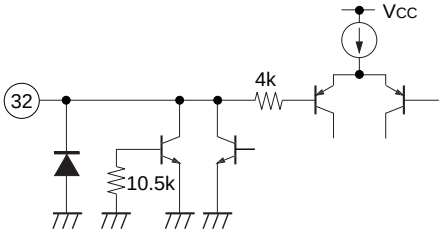
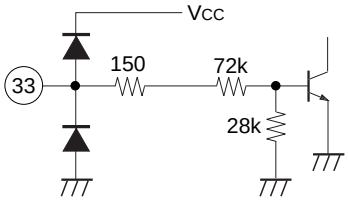
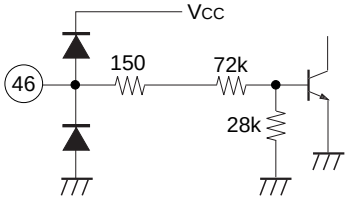
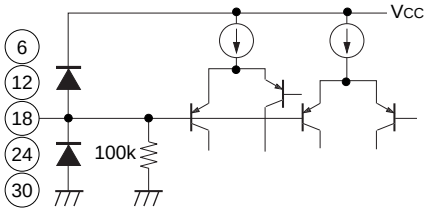


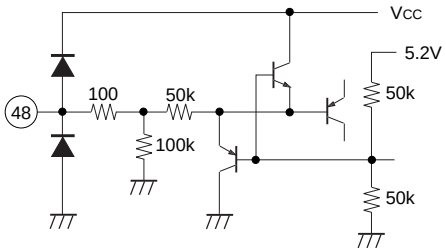
Note) A total gain of 0 dB is achieved by connecting a 6 kΩ resistor to the each audio input.

Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
63 1 7 13 19 25 60	TV V1 V2 V3 V4 V5 V6	4.5 V		Video signal inputs. Input composite video signals.
3 9 15 21 27 5 11 17 23 29	Y1 Y2 Y3 Y4 Y5 C1 C2 C3 C4 C5	4.5 V		Y/C separation signal inputs Y1 to Y5 pins : Input luminance signals. C1 to C5 pins : Input chrominance signals.
62 2 8 14 20 26 59 64 4 10 16 22 28 61	LTV LV1 LV2 LV3 LV4 LV5 LV6 RTV RV1 RV2 RV3 RV4 RV5 RV6	4.6 V		Audio signals inputs.
53 42 35	VOUT1 VOUT2 VOUT3	4.5 V		Video signal outputs. Output composite video signals.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
56 45 58 47	YOUT1 YOUT2 COUT1 COUT2	4.5 V		Y/C signal outputs. YOUT1, YOUT2 pins : Output luminance signals. COUT1, COUT2 pins : Output chrominace signals.
49 38 51 40	YIN1 YIN2 CIN1 CIN2	4.5 V		YIN1, CIN1 pins : Input the Y/C separated signal of VOUT1 output. YIN2, CIN2 pins : Input the Y/C separated signal of VOUT2 output.
55 44	TRAP1 TRAP2	4.5 V		Connect the subcarrier trap circuits.
52 41 34 54 43 36	LOUT1 LOUT2 LOUT3 ROUT1 ROUT2 ROUT3	4.6 V		Audio signal outputs. Z_{OUT}=50 Ω (Within DC ±2 mA)
50	BIAS	4.6 V		Internal reference bias (V_{CC}/2). A capacitor is connected between this pin and GND.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
31	SCL	—		I²C bus signal input. V_{IL}=1.5 V (max.) V_{IH}=3.0 V (min.)
32	SDA	—		I²C bus signal input/output. V_{IL}=1.5 V (max.) V_{IH}=3.0 V (min.) V_{OL}=0.4 V (max.)
33	ADR	—		Selects the slave address for the I²C bus. 90H at 1.5 V or less 92H at 2.5 V or more 90H when open
46	MUTE	—		Audio output mute. Mute OFF at 1.5 V or less Mute ON at 2.5 V or more Mute OFF when open
6 12 18 24 30	S1 S2 S3 S4 S5	—		Video/S signal selection. S signal output at 0.8 V or less Video signal output at 1.4 V or more S signal output when open

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
48	GAIN	—		Audio output gain control. 0 dB output at 2.0 V or less –6 dB output at 3.0 V or more 0 dB output when open

Electrical Characteristics (Ta=25 °C, V_{CC}=9 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	V_{CC}=9 V, no signal, no load	48	60	78	mA

(Video system)

Gain	GV_V	f=100 kHz, 0.3 Vp-p input (Fig. 1)	5.5	6.0	6.5	dB
Frequency response characteristics	F_{BWV1}	0.3 Vp-p input, input frequency where output amplitude is –3 dB with 100 kHz output serving as 0 dB (Fig. 1)	15	20	—	MHz
Frequency response characteristics (Y/C mix)	F_{BWV2}	0.3 Vp-p input, input frequency where output amplitude is –3 dB with 100 kHz output serving as 0 dB (Fig. 1)	10	15	—	MHz
Input dynamic range	Vdv	f=100 kHz, maximum with distortion<1.0 % (Fig. 1)	2.0	—	—	Vp-p
Cross talk	Vctv	f=4.43 MHz, 1 Vp-p input (Fig. 2)	—	—	–50	dB

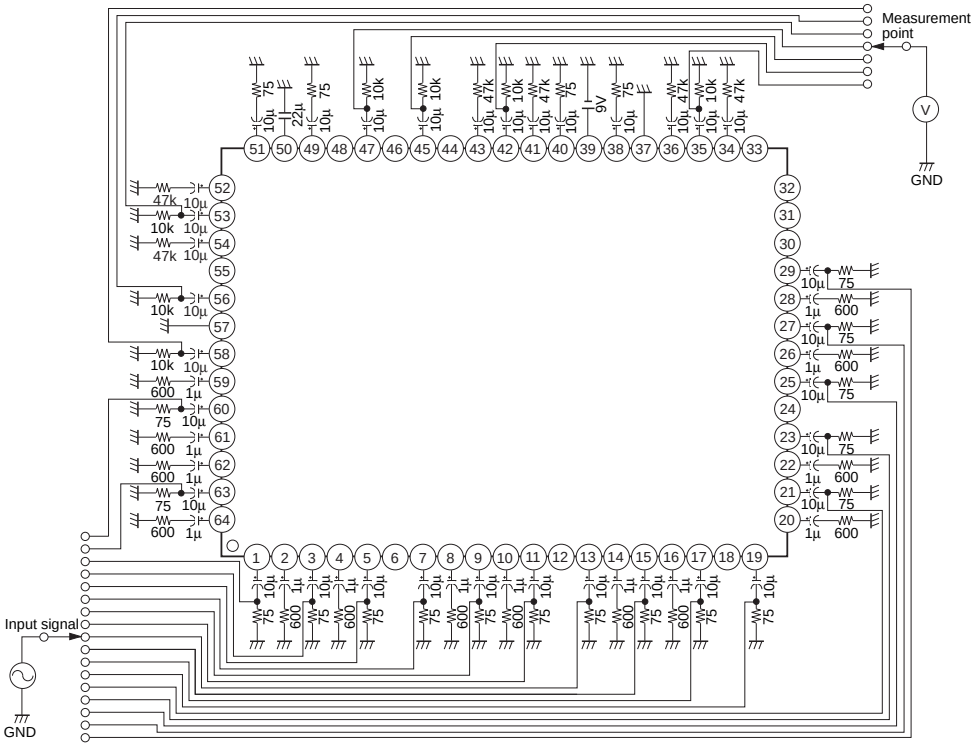
(Audio system)

Gain	GV_A	f=1 kHz, 1 Vp-p input, 6 kΩ resistor inserted to input (Fig. 3)	–1	0	1	dB
Frequency response characteristics	F_{BWA}	1 Vp-p input, input frequency where output amplitude is –3 dB with 100 kHz output serving as 0 dB (Fig. 3)	50	—	—	kHz
Total harmonic distortion	THD	f=1 kHz, 2.2 Vp-p input, when 400 Hz HPF +80 kHz LPF are inserted (Fig. 3)	—	0.03	0.05	%
Input dynamic range	Vd_A	f=1 kHz, maximum with distortion<0.3 %. (Fig. 3)	2.8	3.0	—	Vrms
Cross talk	Vct_A	f=1 kHz, 1 Vp-p input (Fig. 4)	—	–90	–80	dB
Ripple rejection ratio		f=100 Hz, 0.3 Vp-p applied to V_{CC} (Fig. 5)	—	–50	–40	dB
Output DC offset	V_{OFF}	Offset voltage between input and output (Fig. 6)	–30	—	30	mV
Residual noise	V_{NA}	f_{CL}=300 Hz, f_{CH}=19 kHz, 40 dB amplifier connected (Fig. 7)	0	—	6.0	mV
S/N ratio	S/N	f=1 kHz, 1 Vrms input (Fig. 3)	90	100	—	dB

(Logic system)

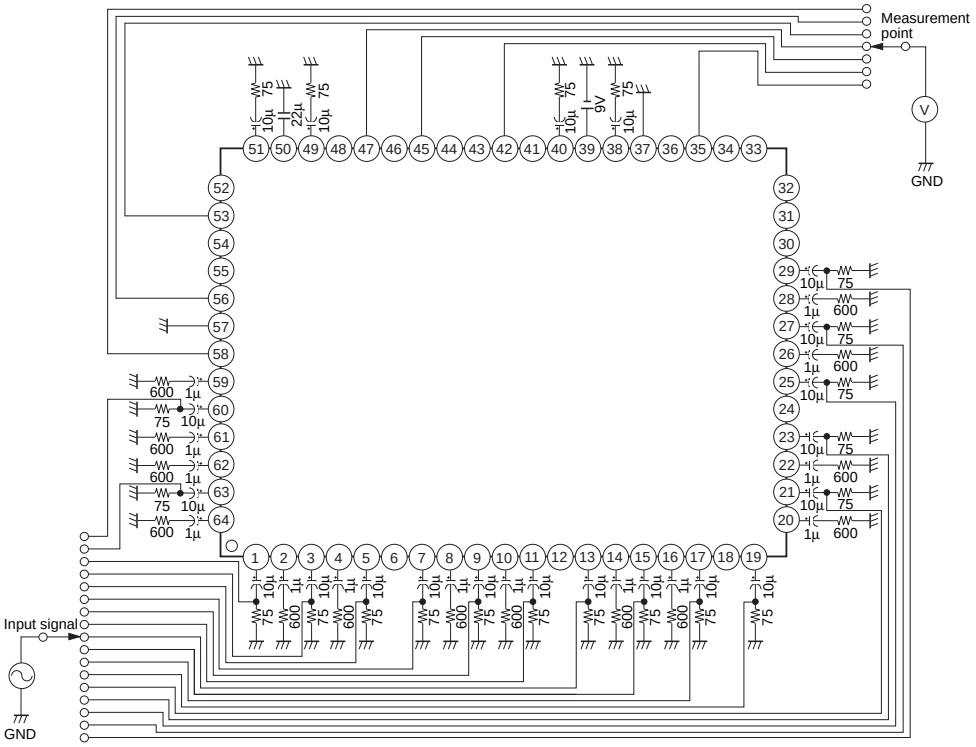
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		3.0	—	5.0	V
Low level input voltage	V_{IL}		0	—	1.5	V
Low level output voltage	V_{OL}	With SDA 3 mA current supplied	0	—	0.4	V
High level input current	I_{IH}	V_{IH}=4.5 V	0	—	10	µA
Low level input current	I_{IL}	V_{IL}=0.4 V	0	—	10	µA
Maximum clock frequency	f_{SCL}		0	—	100	kHz
Minimum waiting time for data change	t_{BUF}		4.0	—	—	µs
Minimum waiting time for data transfer start	$t_{HD;STA}$		4.0	—	—	µs
Low level clock pulse width	t_{LOW}		4.7	—	—	µs
High level clock pulse width	t_{HIGH}		4.0	—	—	µs
Minimum waiting time for start preparation	$t_{SU;STA}$		4.7	—	—	µs
Minimum data hold time	$t_{HD;DAT}$		120	—	—	ns
Minimum data preparation time	$t_{SU;DAT}$		650	—	—	ns
Rise time	t_R		—	—	1	µs
Fall time	t_F		—	—	300	ns
Minimum waiting time for stop preparation	$t_{SU;STO}$		4.7	—	—	µs

Electrical Characteristics Measurement Circuit



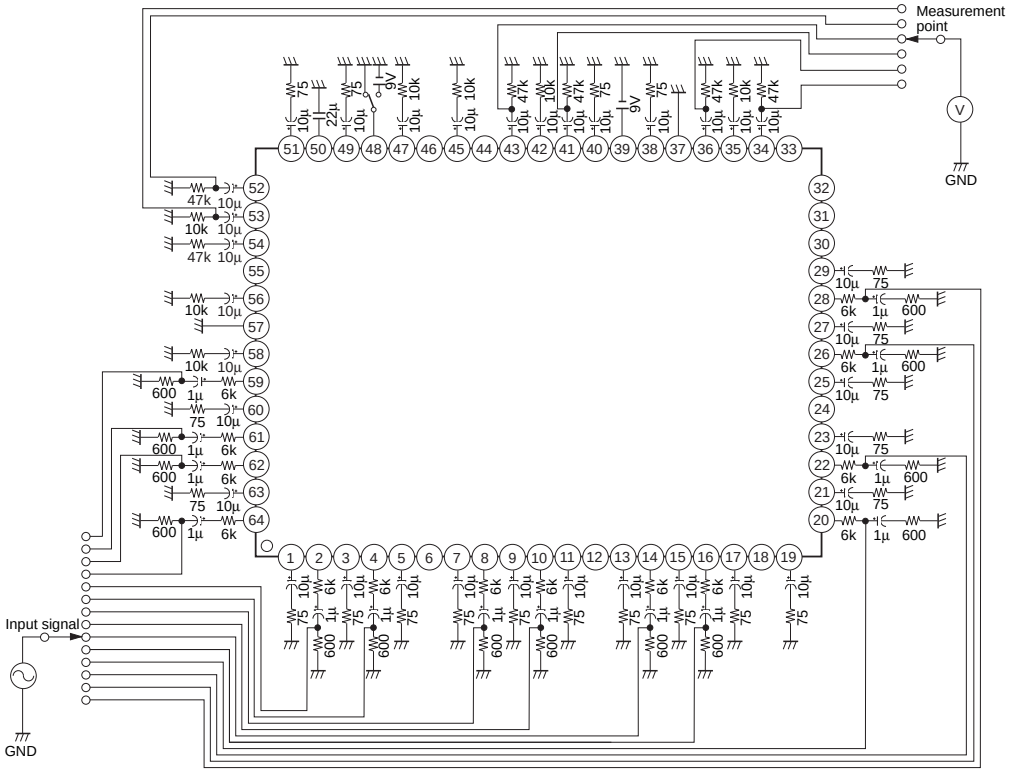
Signal is input from one of the following pins : 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 60, 63
Output signal is measured from one of the following pins : 35, 42, 45, 47, 53, 56, 58

Fig. 1 Video system (gain, frequency response characteristics, input dynamic range)



Signal is input from one of the following pins : 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 60, 63
Output signal from pins other than outputs selected with the switch is measured.

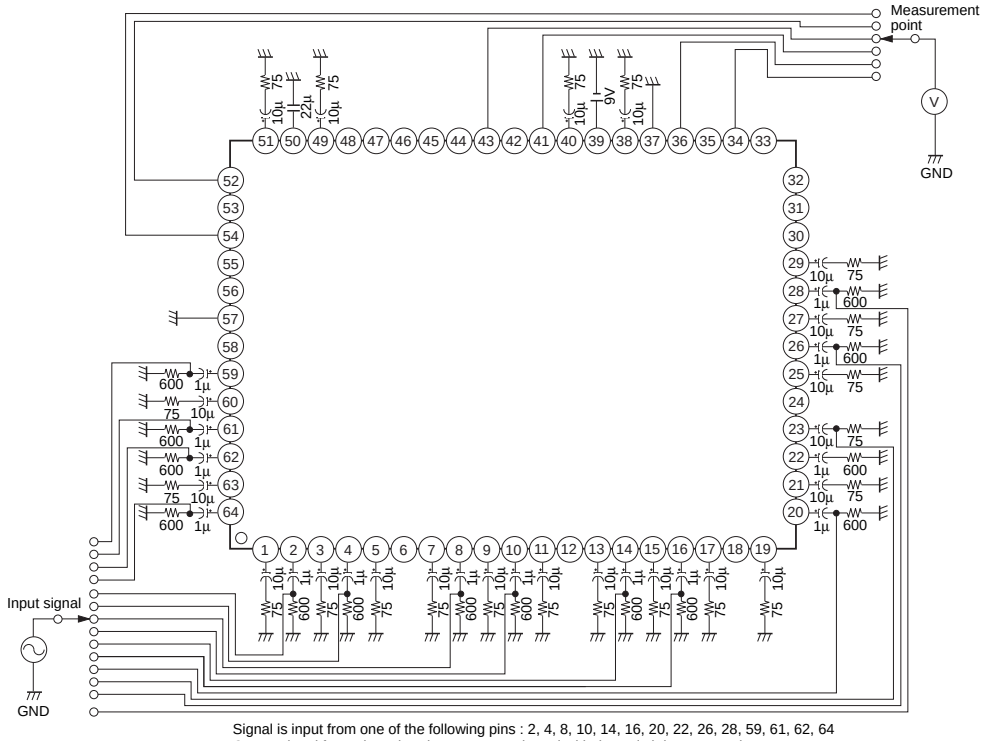
Fig. 2 Video system (cross talk)



Signal is input from one of the following pins : 2, 4, 8, 10, 14, 16, 20, 22, 26, 28, 59, 61, 62, 64
Output signal is measured from one of the following pins : 34, 36, 41, 43, 52, 54
When 9V is applied to Pin 48, the signals from Pins 52 and 54 can be measured for output gain of –6dB.

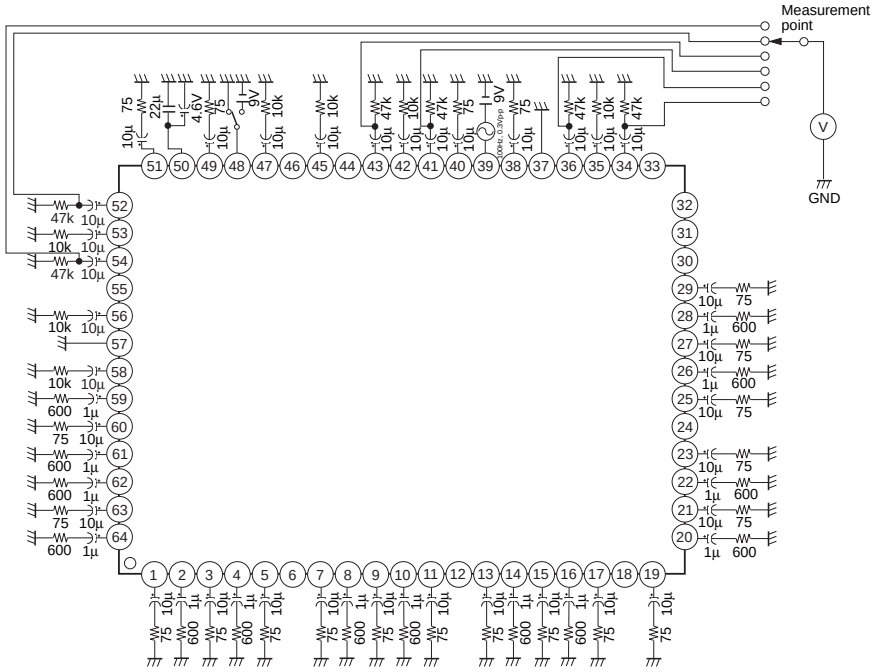
Fig. 3 Audio system

(gain, frequency response characteristics, total harmonic distortion input dynamic range)



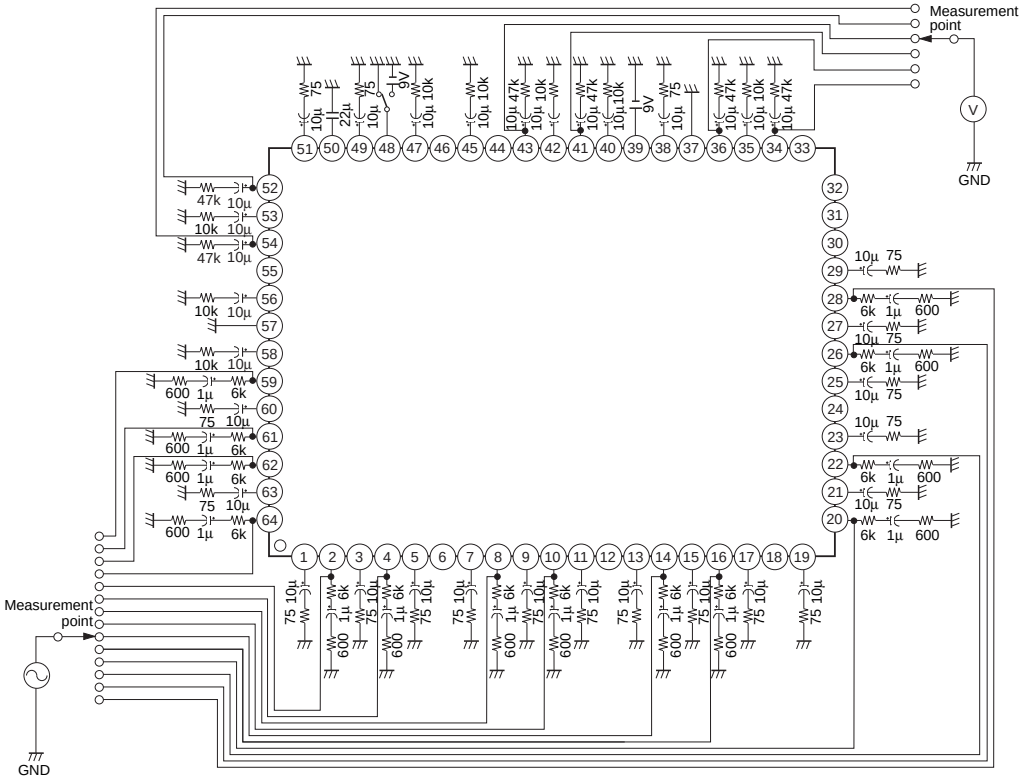
Signal is input from one of the following pins : 2, 4, 8, 10, 14, 16, 20, 22, 26, 28, 59, 61, 62, 64
Output signal from pins other than outputs selected with the switch is measured.

Fig. 4 Audio system (cross talk)



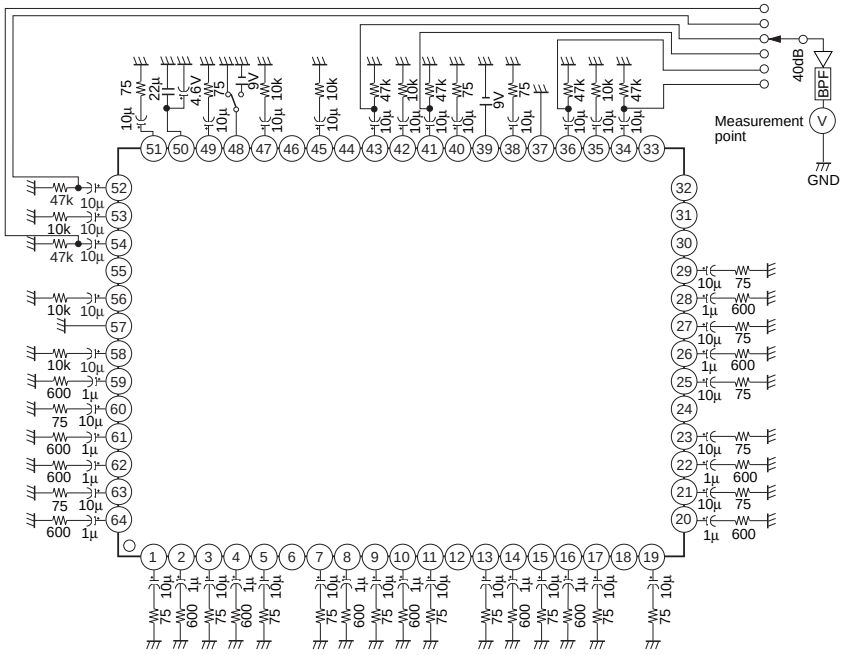
A f=100Hz, 0.3Vp-p signal is applied to V_{CC} and the output signals from Pins 34, 36, 41, 43, 52 and 54 are measured.
When 9V is applied to Pin 48, the signals from Pins 52 and 54 can be measured for output gain of –6dB.

Fig. 5 Audio system (ripple rejection)



When 9V is applied to Pin 48, the signals from Pins 52 and 54 can be measured for output gain of –6dB.

Fig. 6 Audio system (output DC offset)



When 9V is applied to Pin 48, the signals from Pins 52 and 54 can be measured for output gain of –6dB.

Fig. 7 Audio system (residual noise)

I²C Bus Control Signal

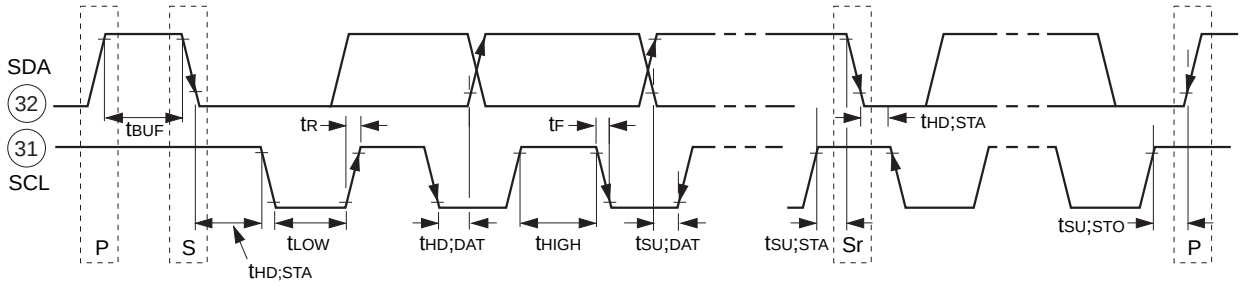


Fig. 8

Description of Operation

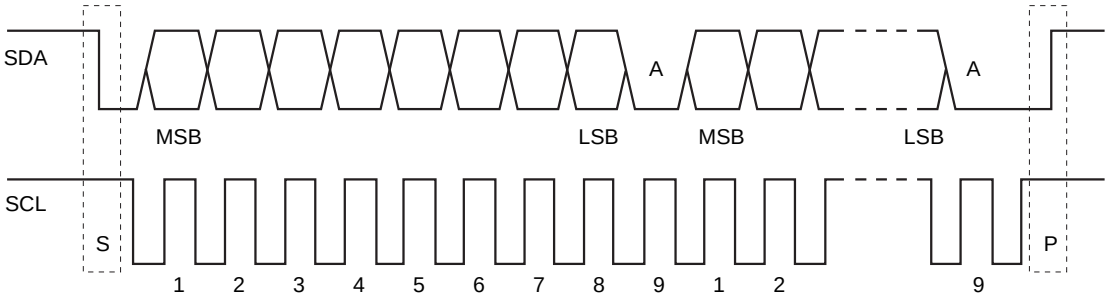
The CXA1845Q is a TV I²C bus-compatible AV switch IC. The video system and the stereo audio system both have 7 inputs and 3 outputs each. Each video output is provided with a built-in 6 dB amplifier. Desired inputs can be independently assigned to all outputs (in the audio system, the left and right channels are processed as one unit) by I²C bus control.

I²C Bus Registers

1. I²C Bus

The I²C bus (Inter-IC bus) is an inter-IC bus system developed by Philips.

Two lines (SDA-serial data, SCL-serial clock) provide control over start, stop, data transfer, synchronization, and collision avoidance. The IC outputs are either open collector or open drain, forming a bus line in the wired OR format.



S : Start condition; SDA is set at “Low” when SCL is “High”
P : Stop condition; SDA is set at “High” when SCL is “High”
A : Acknowledge signal sent from the slave

Data is transmitted by MSB-first. One data unit consists of 8 bits, to which the acknowledge signal, which indicates that the data has been accepted by the slave, is attached at the end. Normally, the slave*1 IC receives data at the rising edge of SCL and the master*2 IC changes data at the falling edge of SCL.

*1 Slave : An IC that is placed under the control of the master. In a normal system, all devices excluding the central microcomputer are slaves.

*2 Master : A central microcomputer or other controlling IC.

2. Control Registers

The CXA1845Q control is exercised by writing 3-byte data into the three 8-bit control registers which control the 3 outputs selector circuits.

S	Slave address	A	DATA1	A	DATA2	A	DATA3	A	P

S : Start condition
A : Acknowledge
P : Stop condition

- **Slave address**

1	0	0	1	0	0	×	0

R/W bit
This bit is set to 0 when the control register is to be written.
Value set by the address pin

DATA1 Provides video 1 output control
DATA2 Provides video 2 output control
DATA3 Provides video 3 output control

- **Control register structure (DATA1 to DATA3)**

b7	b6	b5	b4	b3	b2	b1	b0
S CONT		VIDEO			AUDIO		
(2)		(3)			(3)		

Parenthesized numbers indicate the number of bits.

Each register is set to 0 upon power ON.

Video switch control (VIDEO)

b5	b4	b3	Input signal selected
0	0	0	Mute
0	0	1	TV
0	1	0	V1 system
0	1	1	V2 system
1	0	0	V3 system
1	0	1	V4 system
1	1	0	V5 system
1	1	1	V6 system

V1 system; V1, Y1, C1
V2 system; V2, Y2, C2
V3 system; V3, Y3, C3
V4 system; V4, Y4, C4
V2 system; V5, Y5, C5
V6 system; V6

Audio switch control (AUDIO)

b2	b1	b0	Input signal selected
0	0	0	Mute
0	0	1	RTV/LTV
0	1	0	RV1/LV2
0	1	1	RV2/LV2
1	0	0	RV3/LV3
1	0	1	RV4/LV4
1	1	0	RV5/LV5
1	1	1	RV6/LV6

S input control (S CONT)

b7	b6	Output pin
0	×	Selected by S1 to S5 pins
1	0	Selects composite input.
1	1	Selects S input.

Composite input : TV, V1 to V6
S input : Y1 to Y5, C1 to C5

Note 1) When "b7" is set to 0, the S input/composite input is automatically switched by the voltages at S1 to S5 pins.

Note 2) The YOUT1/2 and COUT1/2 switches are also switched by this control.
Low : S input
High : Composite input

3. Status Registers

S	Slave address	A	DATA1	A	DATA2	NA	P

S	Slave address	A	DATA1	NA	P

S : Start condition
A : Acknowledge
P : Stop condition
NA : No acknowledge

When communication is to be terminated in the status register reading mode, the "no acknowledge" signal is needed to assure that the slave does not issue the acknowledge signal to master. Only DATA1 of status register can be read if NA is sent after DATA1.

• **Slave address**

1	0	0	1	0	0	×	0

R/W bit
This bit is set to 1 when the status register is to be read.

Value set by the address pin

• **DATA**

	b7			b4	b3	b2	b1	b0
DATA1	PONRES	×	×	S5 SEL	S4 SEL	S3 SEL	S2 SEL	S1 SEL
DATA2	PONRES	×	×	S5 OPEN	S4 OPEN	S3 OPEN	S2 OPEN	S1 OPEN

PONRES

When the CXA1845Q is reset upon power ON, logical 1 is returned. Once a read operation is completed, logical 0 is returned.

S1 to S5 OPEN

0 : S1 to S5 pins are not open.

1 : S1 to S5 pins are open.

S1 to S5 SEL

0 : S1 to S5 pins are not grounded.

1 : S1 to S5 pins are grounded.

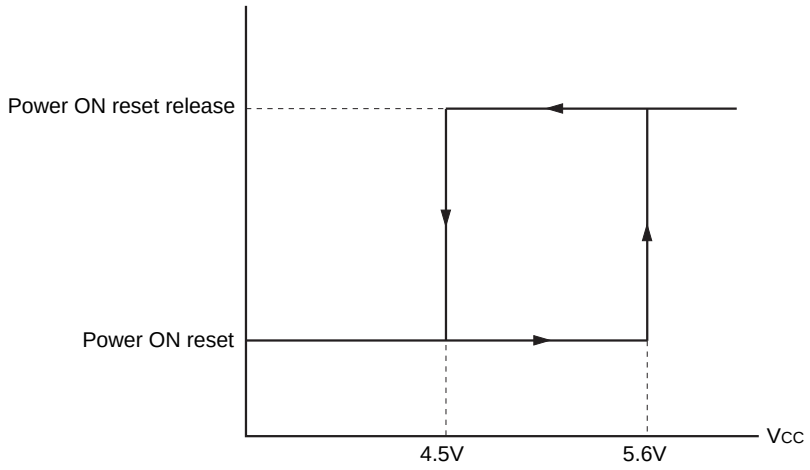
In actually, the logic states of the S1 to S5 OPEN and the S1 to S3 SEL bits are determined by comparing the DC voltages of S1 to S5 pins to two threshold values.

DC voltage of S1 to S5 pins	S1 to S5 OPEN	S1 to S5 SEL
0.8 V or less	0	1
1.3 V or more, 3.5 V or less	0	0
4.5 V or more	1	0

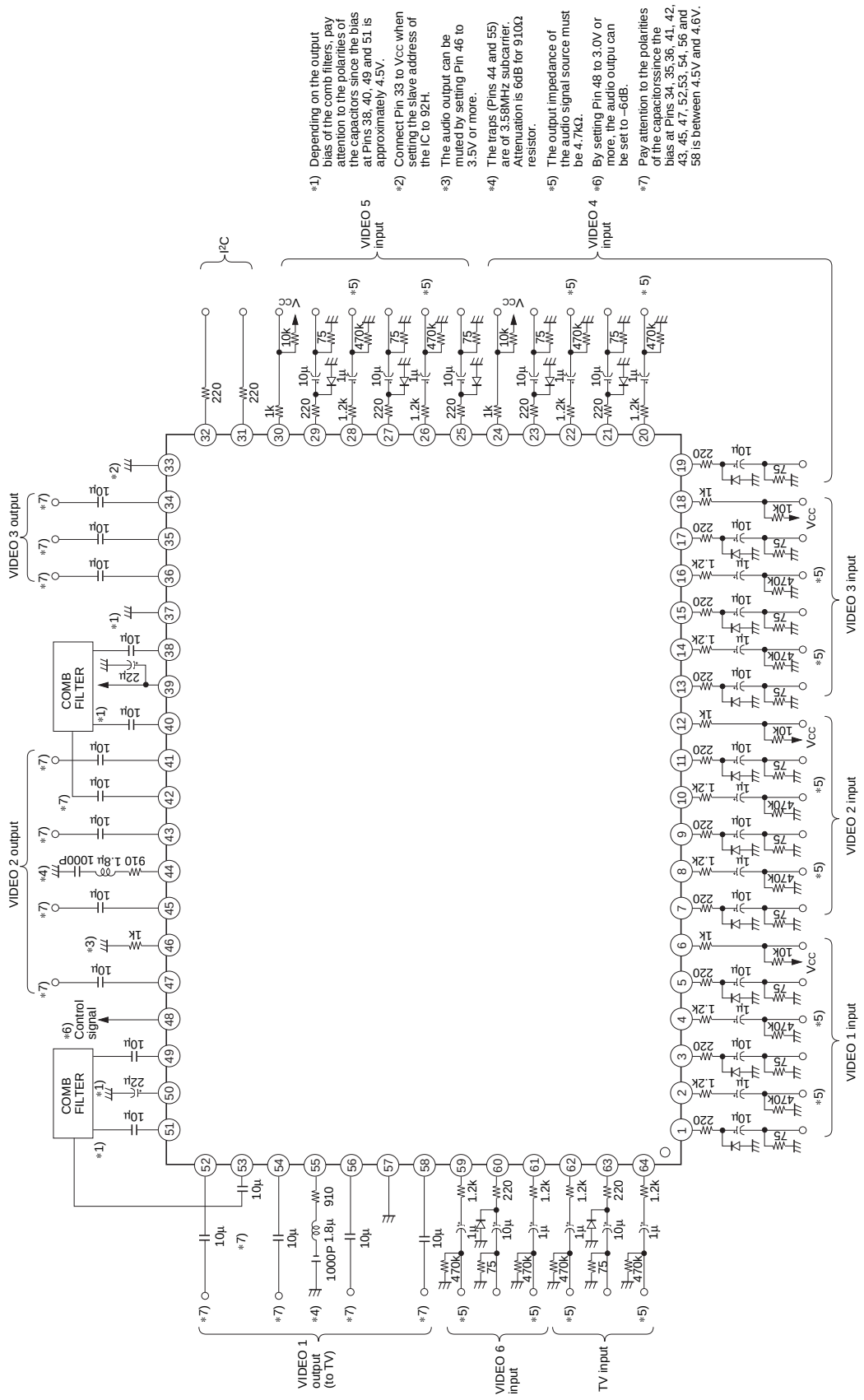
4. Power ON reset

The CXA1845Q incorporates the power ON reset function. Therefore, each control register is reset to 0 upon power ON.

The power ON reset V_{TH} is hysteretical. The PONRES bit of the status register is read to determine whether the IC is reset upon power ON.



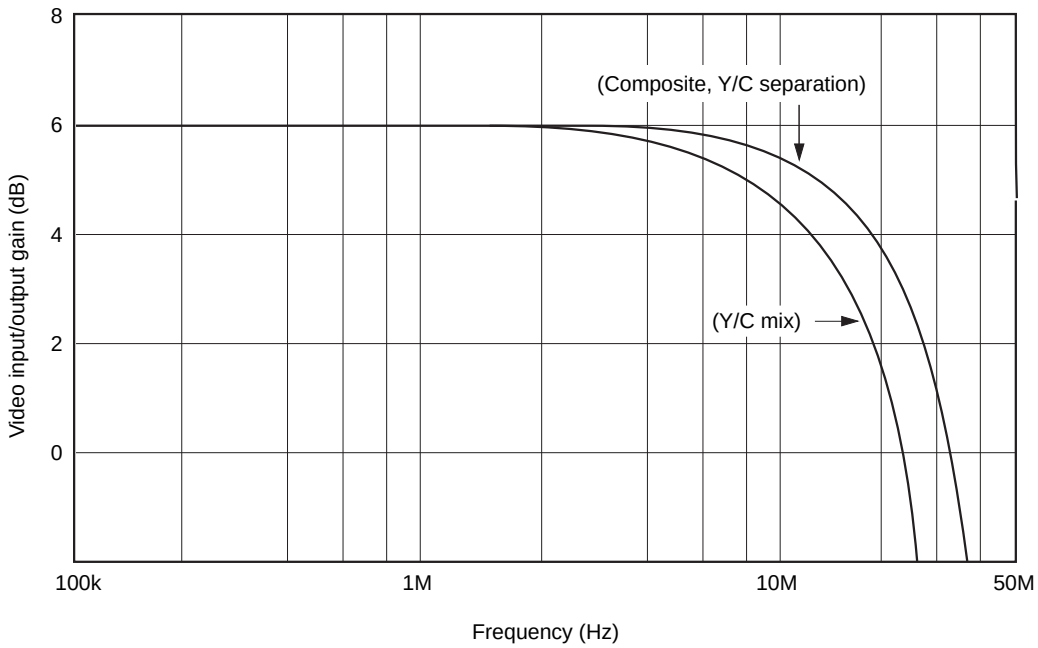
Application Circuit



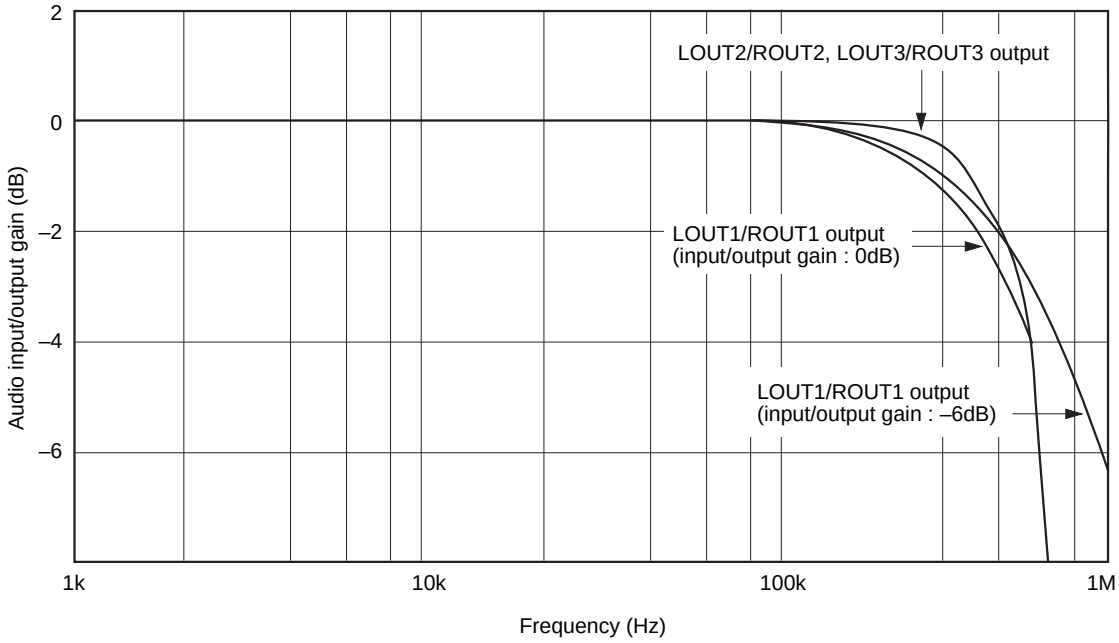
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

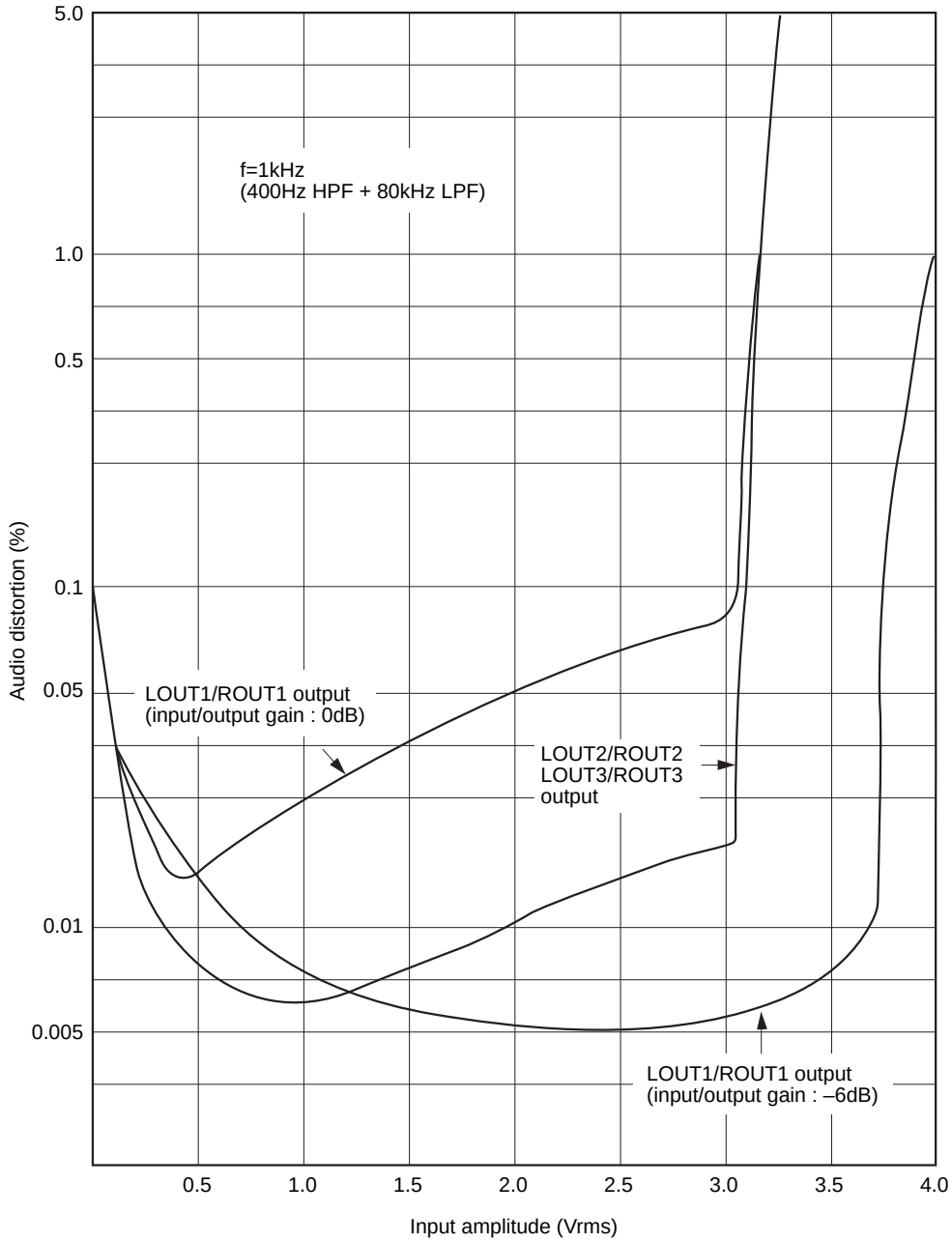
Video frequency response



Audio frequency response

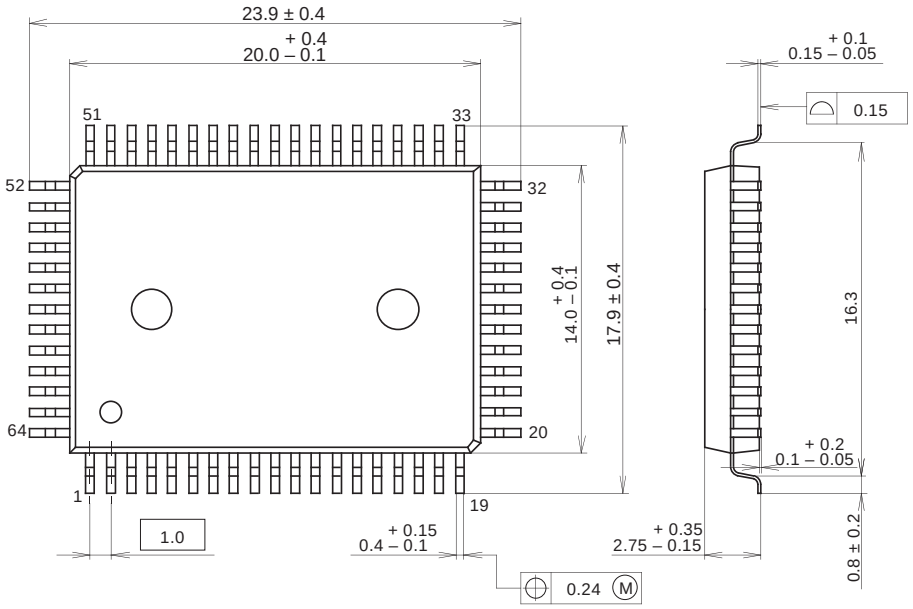


Audio distortion vs. Input amplitude



Package Outline Unit : mm

64PIN QFP(PLASTIC)



SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g