SONY

CXA3197R

10-bit 125MSPS D/A Converter

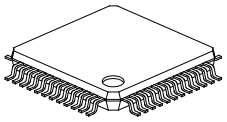
Preliminary

Description

The CXA3197R is a high-speed D/A converter which can perform the multiplexed input of the two system 10-bit data.

The maximum conversion rate achieves 125MSPS. The multiplexed operation is possible by the 1/2 frequency-divided clock or by halving the frequency of the clock with the clock frequency divider circuit having the reset pin in the IC. The data input pin is TTL; the clock input pin and reset input pin can select either TTL or PECL according to the application.

48 pin LQFP (Plastic)



Features

- Maximum conversion rate: 125MSPS
- Resolution: 10 bits
- Low glitch energy: 1.5pVs
- Low power consumption: 400mW (typ.)
- Differential linearity error: ±0.5LSB or less
- Integral linearity error: ±1.0LSB or less
- Data input level: TTL
- Clock, reset input level: TTL and PECL compatible
- 2:1 multiplexed input function
- 1/2 frequency-divided clock output possible by the built-in clock frequency divider circuit
- Voltage output (50Ω load drive possible)
- Single power supply or ±dual power supplies
- Polarity switching function of reset signal

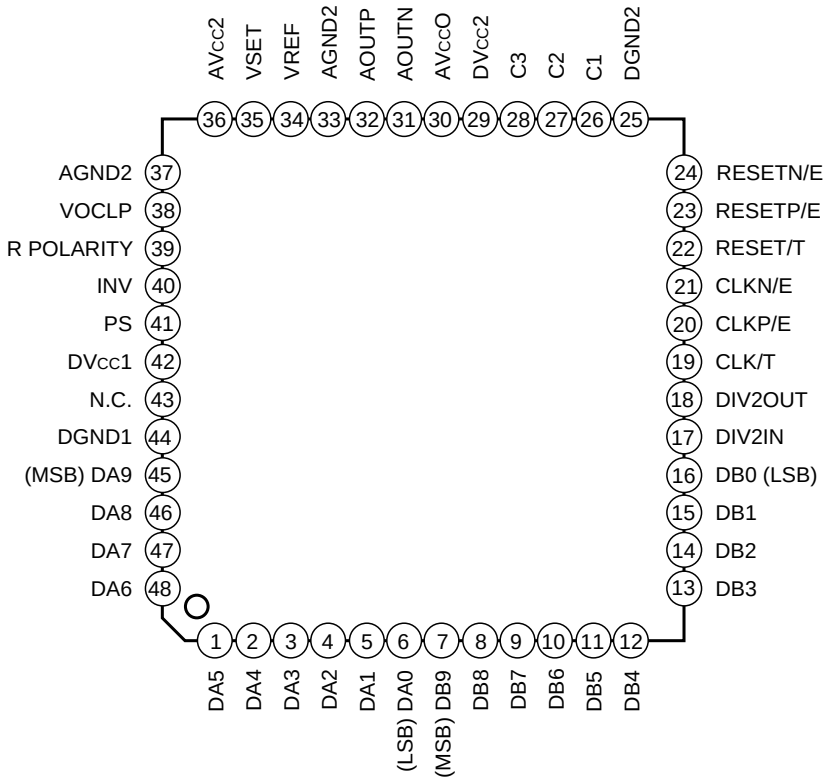
Structure

Bipolar silicon monolithic IC

Applications

- LCD
- DDS
- HDTV
- Communications (QPSK, QAM)
- Measuring device

Pin Configuration



PE97639-PS

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV$_{CC}$O, AV$_{CC}$2, DV$_{CC}$2	–0.5 to +7.0	V
	AGND2, DGND2	–7.0 to +0.5	V
	DV$_{CC}$1	–0.5 to +7.0	V
	AV$_{CC}$2 – AGND2	–0.5 to +7.0	V
	AV$_{CC}$O – AGND2	–0.5 to +7.0	V
	DV$_{CC}$2 – DGND2	–0.5 to +7.0	V
• Input voltage			
(Analog)	VSET	AGND2 – 0.5 to AV$_{CC}$2 + 0.5	V
(Digital)	TTL pin	DGND1 – 0.5 to DV$_{CC}$1 + 0.5	V
	PECL pin	DGND1 – 0.5 to DV$_{CC}$1 + 0.5	V
	PS	DGND1 – 0.5 to DV$_{CC}$1 + 0.5	V
(Others)	VOCLP	DGND1 – 0.5 to DV$_{CC}$1 + 0.5	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	Pd	1.4	W

(when mounted on a glass fabric base epoxy board with 76mm × 114mm, 1.6mm thick)

Recommended Operating Conditions

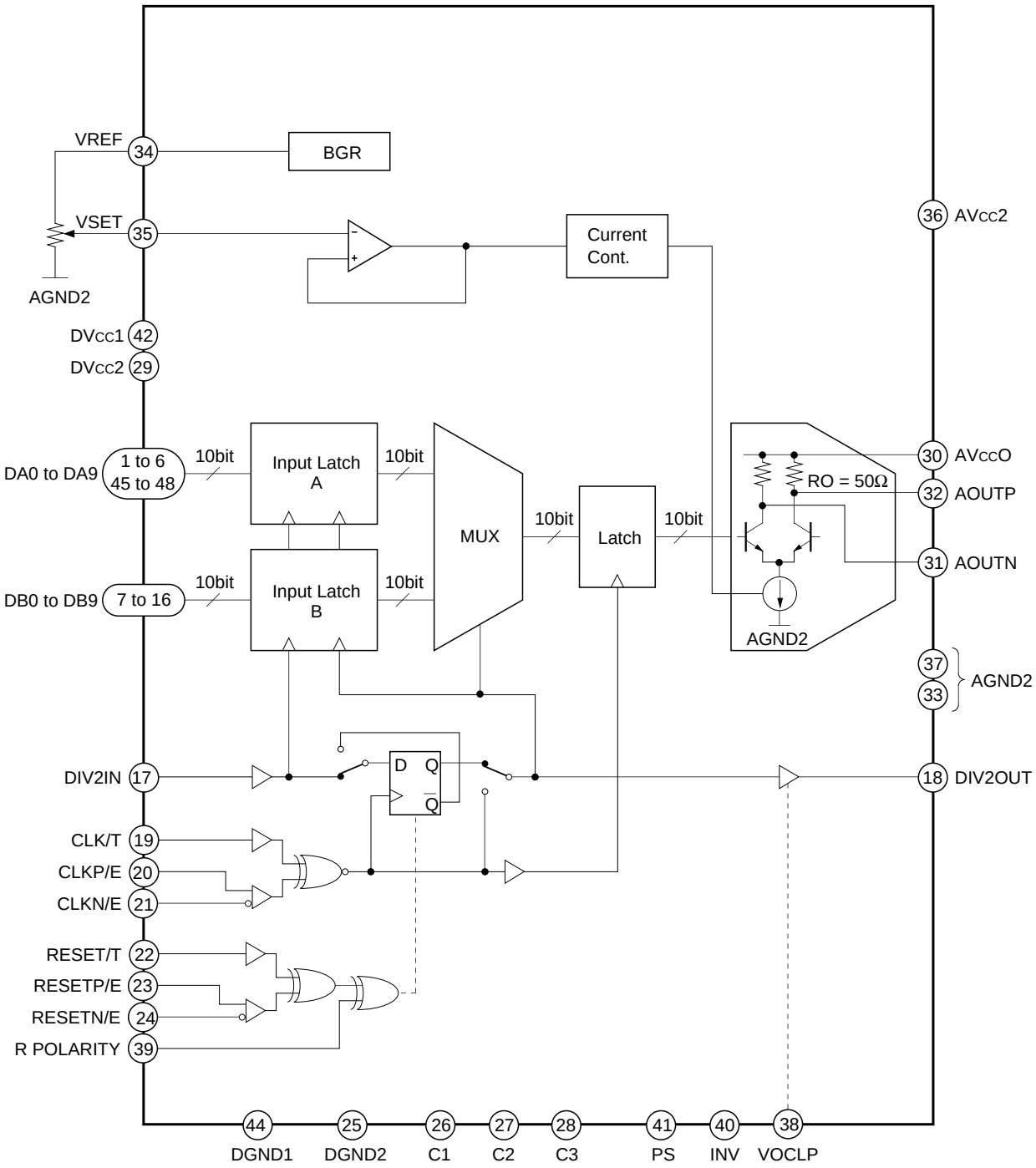
	[Single power supply]			[Dual power supplies]			Unit
• Supply voltage	Min.	Typ.	Max.	Min.	Typ.	Max.	
AV$_{CC}$O	+4.75	+5.0	+5.25	–0.05	0.0	+0.05	V
AV$_{CC}$2	+4.75	+5.0	+5.25	–0.05	0.0	+0.05	V
AGND2	–0.05	0.0	+0.05	–5.50	–5.0	–4.75	V
DV$_{CC}$1	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
DGND1	–0.05	0.0	+0.05	–0.05	0.0	+0.05	V
DV$_{CC}$2	+4.75	+5.0	+5.25	–0.05	0.0	+0.05	V
DGND2	–0.05	0.0	+0.05	–5.50	–5.0	–4.75	V

• Input voltage			Min.	Typ.	Max.	Unit
(Analog)	VSET		AGND2 + 0.7		AGND2 + 1.03	V
(Digital)	TTL pin	V_{IH}	DGND1 + 2.0			V
		V_{IL}			DGND1 + 0.8	V
	PECL pin	V_{IH}	DGND1 + 2.6	DV$_{CC}$1 – 1.0	DV$_{CC}$1	V
		V_{IL}	V_{IH} – 4.0	DV$_{CC}$1 – 1.6	V_{IH} – 0.4	V
	PS	V_{IH}	DGND1 + 2.0			V
		V_{IL}			DGND1 + 0.8	V
(Others)	VOCLP		DGND1 + 2.7		DV$_{CC}$1	V
• CLK pulse width	tpw1		4.0			ns
	tpw0		4.0			ns
• Maximum conversion rate	Fc		125			MSPS
• Load resistance	R_L		50	50	≥ 10k	Ω
• Analog output full-scale voltage						
RL ≥ 10kΩ	V_{FS}		1.5	2.0	2.2	V
RL = 50Ω	V_{FS}		0.75	1.0	1.2	V
• Operating temperature	Ta		–20		+75	°C

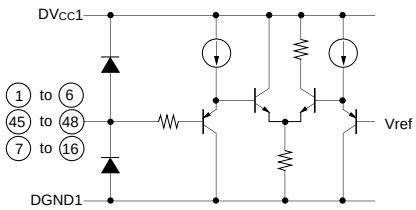
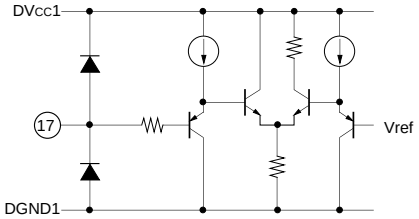
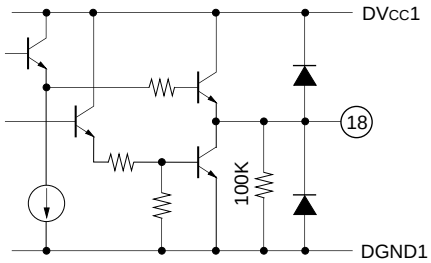
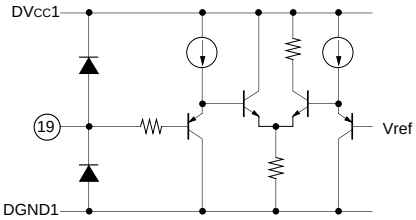
Pin Description

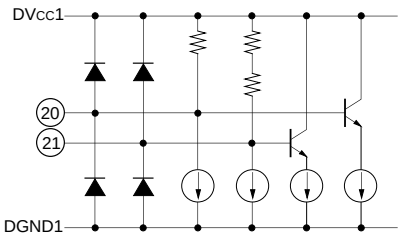
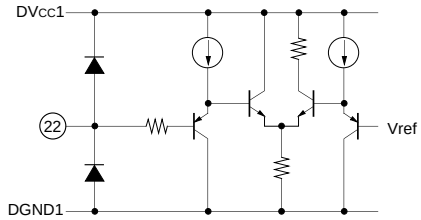
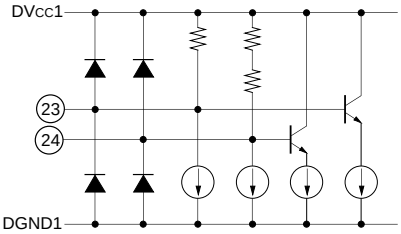
[Symbol]	[Pin No.]	[Description]	[Level for a single power supply]	[Level for dual power supplies]
DA0 to DA9	1 to 6, 45 to 48	Side A data input.	TTL	TTL
DB0 to DB9	7 to 16	Side B data input.	TTL	TTL
DIV2IN	17	1/2 frequency-divided clock input.	TTL	TTL
DIV2OUT	18	1/2 frequency-divided clock output.	TTL	TTL
CLK/T	19	TTL clock input.	TTL	TTL
CLKP/E	20	PECL clock input.	PECL	PECL
CLKN/E	21	PECL clock input.	PECL	PECL
RESET/T	22	TTL reset input.	TTL	TTL
RESETP/E	23	PECL reset input.	PECL	PECL
RESETN/E	24	PECL reset input.	PECL	PECL
DGND2	25	Digital ground.	0V	–5V
C1	26	Function setting.	TTL	TTL
C2	27	Function setting.	TTL	TTL
C3	28	Function setting.	TTL	TTL
$DV_{CC}2$	29	Digital power supply.	5V	0V
$AV_{CC}O$	30	Analog output power supply.	5V (typ.)	0V (typ.)
AOUTN	31	D/A negative output.	$AV_{CC}O - V_{FS}$	$AV_{CC}O - V_{FS}$
AOUTP	32	D/A positive output.	$AV_{CC}O - V_{FS}$	$AV_{CC}O - V_{FS}$
AGND2	33	Analog ground.	0V	–5V
VREF	34	Analog reference voltage.	AGND2 + 1.2V	AGND2 + 1.2V
VSET	35	Full-scale adjustment.		
$AV_{CC}2$	36	Analog power supply.	5V	0V
AGND2	37	Analog ground.	0V	–5V
VOCLP	38	TTL High level clamp.	Clamp voltage	Clamp voltage
R POLARITY	39	Reset signal polarity switching.	TTL	TTL
INV	40	Analog output inversion.	TTL	TTL
PS	41	Power saving.	TTL	TTL
$DV_{CC}1$	42	Digital power supply.	5V	5V
N.C.	43	Not connected.		
DGND1	44	Digital ground.	0V	0V

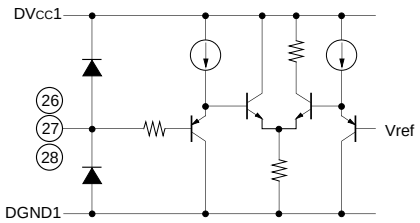
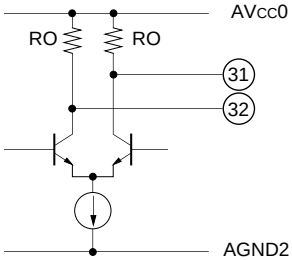
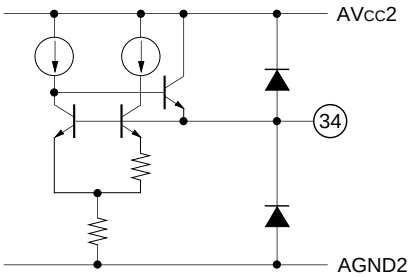
Block Diagram

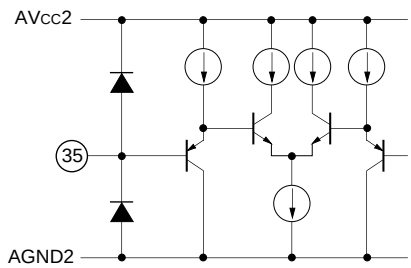
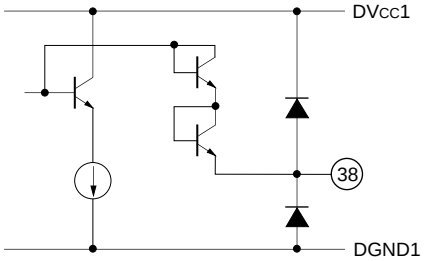
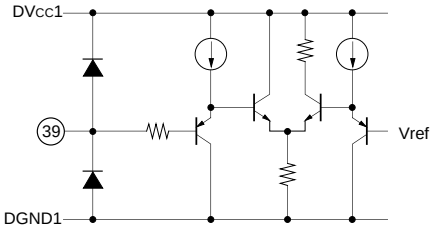
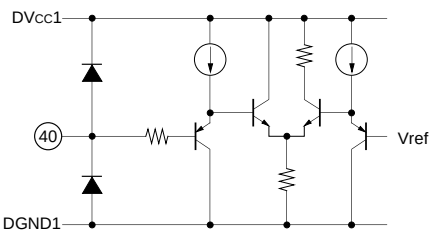


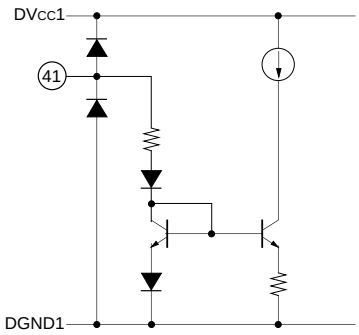
Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Typical voltage level	Equivalent circuit	Description
1 to 6 45 to 48	DA0 to DA9	I	TTL		Side A data input.
7 to 16	DB0 to DB9	I	TTL		Side B data input.
17	DIV2IN	I	TTL		1/2 frequency-divided clock input. Use this pin for MUX.1A or MUX.2 mode. Leave open for other modes.
18	DIV2OUT	O	TTL		1/2 frequency-divided clock output. The signal with the 1/2 frequency-divided clock (DIV2OUT) is output for MUX.1A mode. Leave open for other modes.
19	CLK/T	I	TTL		Clock input. Use this pin when the clock is input in the TTL level. At this time, leave Pins 20 and 21 open.

Pin No.	Symbol	I/O	Typical voltage level	Equivalent circuit	Description
20	CLKP/E	I	PECL		Clock input. Use this pin when the clock is input in PECL level. At this time, leave Pin 19 open.
21	CLKN/E	I	PECL		CLKP/E complimentary input. When left open, this pin goes to the threshold potential(DVcc1 – 1.3V). Operation is possible only with CLKP/E, but complimentary input is recommended to attain fast and stable operation.
22	RESET/T	I	TTL		Reset signal input. When the multiple CXA3197R are operated at a time for MUX.1A or MUX.1B mode, the start timing of the internal 1/2 frequency divider circuits should be matched. At this time, the reset signal is used; when the reset signal is the TTL level, Pin 22 is used and Pins 23 and 24 are left open. When the reset signal is the PECL level, Pins 23 and 24 are used and Pin 22 is left open. For the PECL level, operation is possible only with RESETP/E as with the case for the clock. The reset signal polarity can be set by Pin 39 (R POLARITY). Leave the reset pin open when the other modes are used.
23	RESETP/E	I	PECL		
24	RESETN/E	I	PECL		
25	DGND2		Single power supply: GND Dual power supplies: –5V		Digital power supply.

Pin No.	Symbol	I/O	Typical voltage level	Equivalent circuit	Description
26	C1	I	TTL		Function setting.
27	C2	I	TTL		Function setting.
28	C3	I	TTL		Function setting.
29	DVcc2		Single power supply: +5V Dual power supplies: GND		Digital power supply.
30	AVccO				Analog output power supply.
31	AOUTN	O	AVccO – VFS		D/A negative output. The inversion of the D/A positive output pin is output. Terminate the inversion output pin with 50Ω when the inversion output is not used and the positive output is terminated with 50Ω.
32	AOUTP	O	AVccO – VFS		D/A positive output.
33	AGND2		Single power supply: GND Dual power supplies: –5V		Analog ground.
34	VREF	O	AGND + 1.2V		Analog reference voltage. Output.

Pin No.	Symbol	I/O	Typical voltage level	Equivalent circuit	Description
35	VSET	I	AGND2+0.7V to AGND2+1.03V		Full-scale adjustment.
36	AVCC2		Single power supply: +5V Dual power supplies: GND		Analog power supply.
37	AGND2		Single power supply: GND Dual power supplies: –5V		Analog power supply.
38	VOCLP	I	Clamp voltage		TTL output High level clamp. The TTL level signal is output from the DIV2OUT pin for MUX.1A mode. The TTL High level voltage is clamped to the value approximately equivalent to the voltage supplied to this pin. Leave the VOCLP pin open for other modes.
39	R POLARITY	I	TTL		Reset signal polarity switching. At High level, the reset polarity is active High; at Low level, active Low.
40	INV	I	TTL		Analog output polarity inversion. The analog output is inverted at Low level.

Pin No.	Symbol	I/O	Typical voltage level	Equivalent circuit	Description
41	PS	I	TTL		Power saving. Power saving at Low level. Normally pull up the PS pin to High level as this pin is open Low.
42	DVcc1		5V		Digital power supply.
43	NC				No connected.
44	DGND1		0V		Digital ground.

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		10	10	10	bit
Differential linearity error	DLE	V_{FS} = 1000mV			±0.5	LSB
Integral linearity error	ILE				±1.0	LSB
Digital input current (TTL pin)	I_{IH}	I_{IH} = 2.0V	–10		0	µA
	I_{IL}	I_{IL} = 0.8V	–10		0	µA
Digital input current (PECL pin)	I_{IH}	V_{IH} = $DV_{CC}1$ – 1.1			10	µA
	I_{IL}	V_{IL} = $DV_{CC}1$ – 1.5			10	µA
Digital input current (PS)	I_{IH}	V_{IH} = 2.0V or more	5		60	µA
	I_{IL}	V_{IL} = 0.8V or less	0			µA
Clamp pin input current (VOCLP)	I_O	V = $DV_{CC}1$			0	µA
	I_O	V = 2.7V	–10			µA
Digital input capacitance	C_{IN}			3		pF
Digital output voltage (DIV2OUT)	V_{OH}	I_{OH} = –2mA	2.4			V
	V_{OL}	I_{OL} = 1mA			0.5	V
VREF pin voltage	V_{REF}	Iref = 1mA	AGND2 +1.16	AGND2 +1.20	AGND2 +1.24	V
Analog output voltage	V_{FS}	$R_L \geq 10k\Omega$	1.5	2.0	2.2	V
		R_L = 50Ω	0.75	1.0	1.2	V
Compliance voltage	V_{OC}					V
Output zero offset voltage	V_{OF}	$R_L \geq 10k\Omega$			12	mV
		R_L = 50Ω			6	mV
Output resistance	R_O			50		Ω
Output capacitance	C_O			10		pF
Absolute amplitude error	E_G	V_{FS} = 1000mV	–10		+10	% of F.S.
Absolute amplitude error temperature characteristics	T_{CG}					% of F.S./°C
Current consumption	I_{CC}		70	85	100	mA
Maximum conversion rate	F_C		125			MSPS
Analog output						
Rise time	tr	R_L = 50Ω		1.0	1.2	ns
Fall time	tf			1.0	1.2	ns
Settling time	t_{SET}			3.5		ns
Glitch energy	GE			1.5		pVs

Input Coding Table

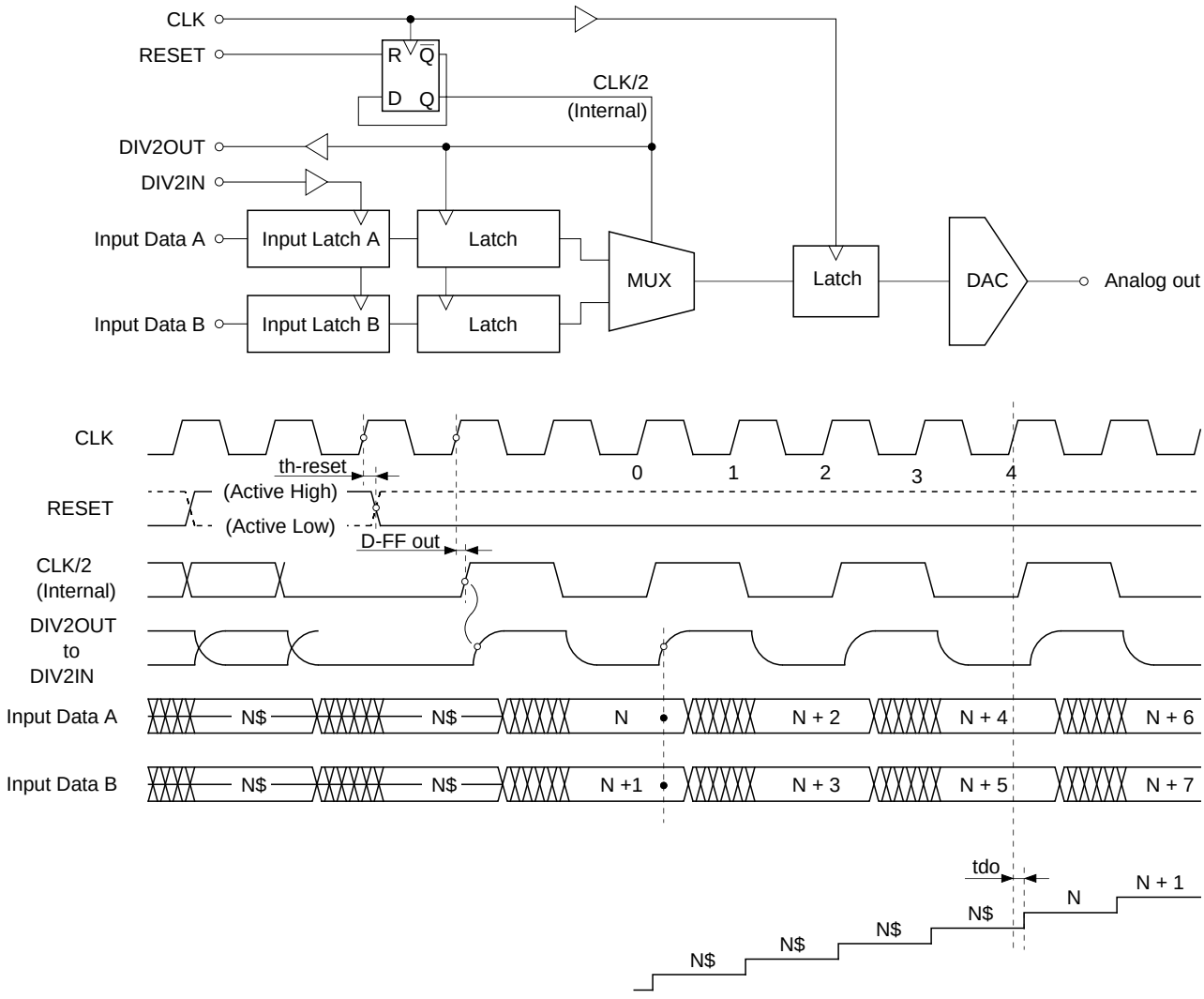
IN V	Data input D0 to D9	AOUT P	AOUT N
0	000···00	AV_{CCO} – 0	AV_{CCO} – V_{FS}
1		AV_{CCO} – V_{FS}	AV_{CCO} – 0
0	111···11	AV_{CCO} – V_{FS}	AV_{CCO} – 0
1		AV_{CCO} – 0	AV_{CCO} – V_{FS}

Description of Operating Modes

C1	C2	C3	Mode	CLK IN (MSPS)	Data IN (Mbps)	AOUT (Mbps)	DIV2OUT	Description
0	0	0	MUX.1A	125	62.5	125	Enable	MUX operation by the internal CLK/2
0	0	1	MUX.1B				High impedance	MUX operation by the internal CLK/2
0	1	0	MUX.2				High impedance	MUX operation by the external DIV2IN
1	0	0	SELE.A		125		High impedance	Side A data select
1	1	0	SELE.B				High impedance	Side B data select

Description of Operation

Block Diagram & Timing Chart (MUX.1A Mode)

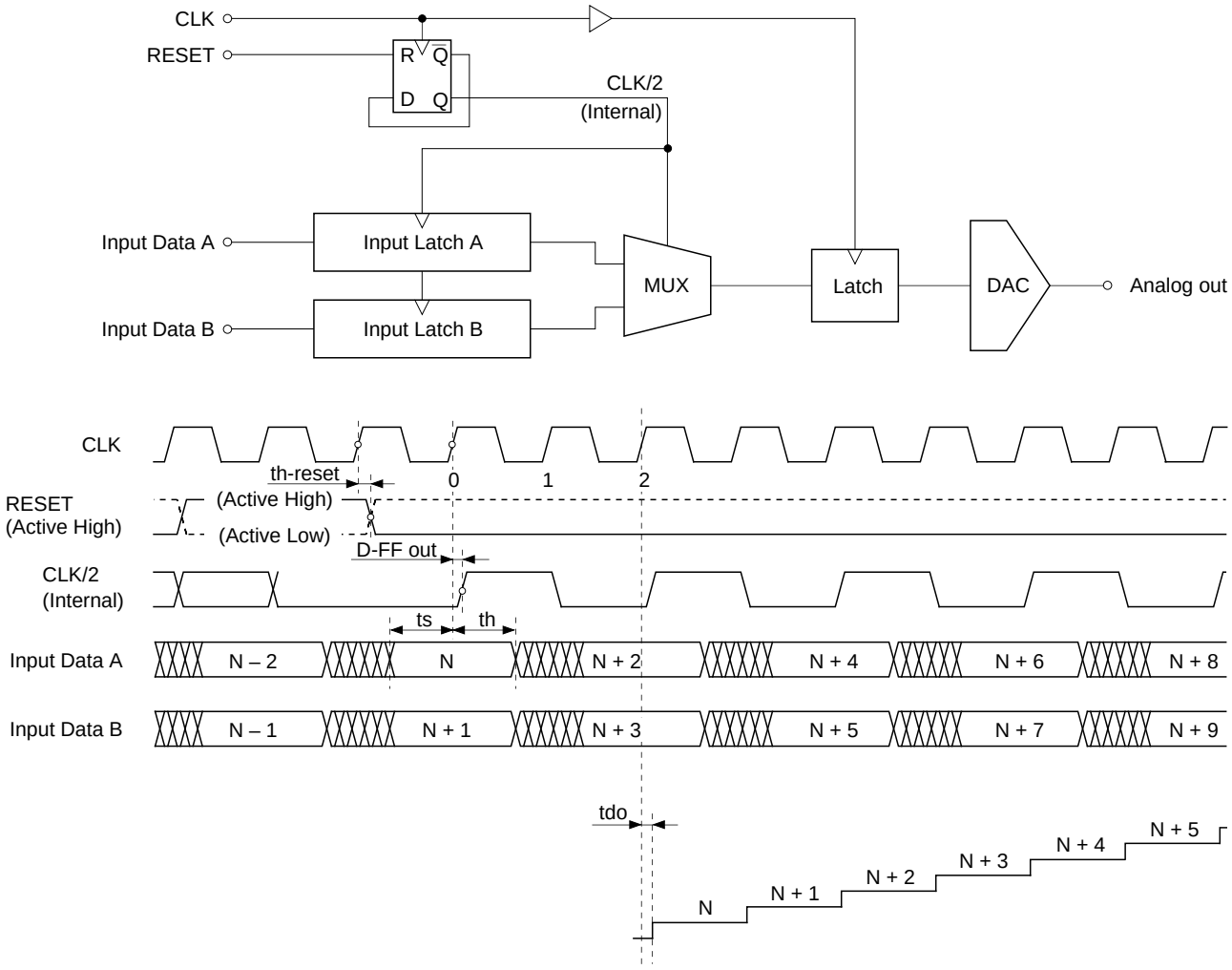


For MUX.1A mode, Data A and Data B are internally multiplexed and then the resulting signal can be analog output.

The frequency of the clock is halved by the built-in clock divider circuit and the CLK/2 can be output in the TTL level (DIV2OUT).

CLK/2 can be reset by the reset signal.

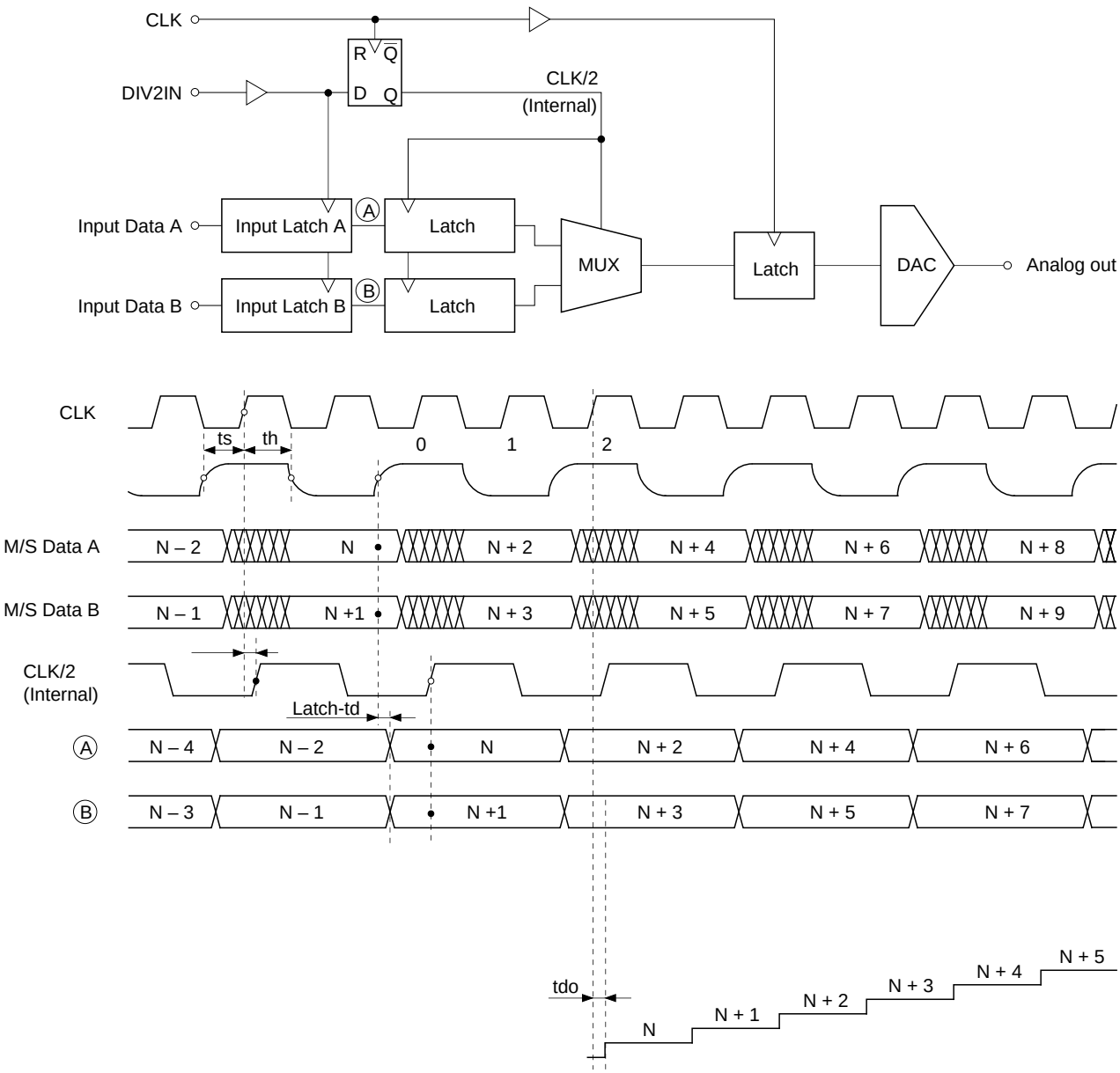
Block Diagram & Timing Chart (MUX.1B Mode)



For MUX.1B mode, Data A and Data B are internally multiplexed and then the resulting signal can be analog output.

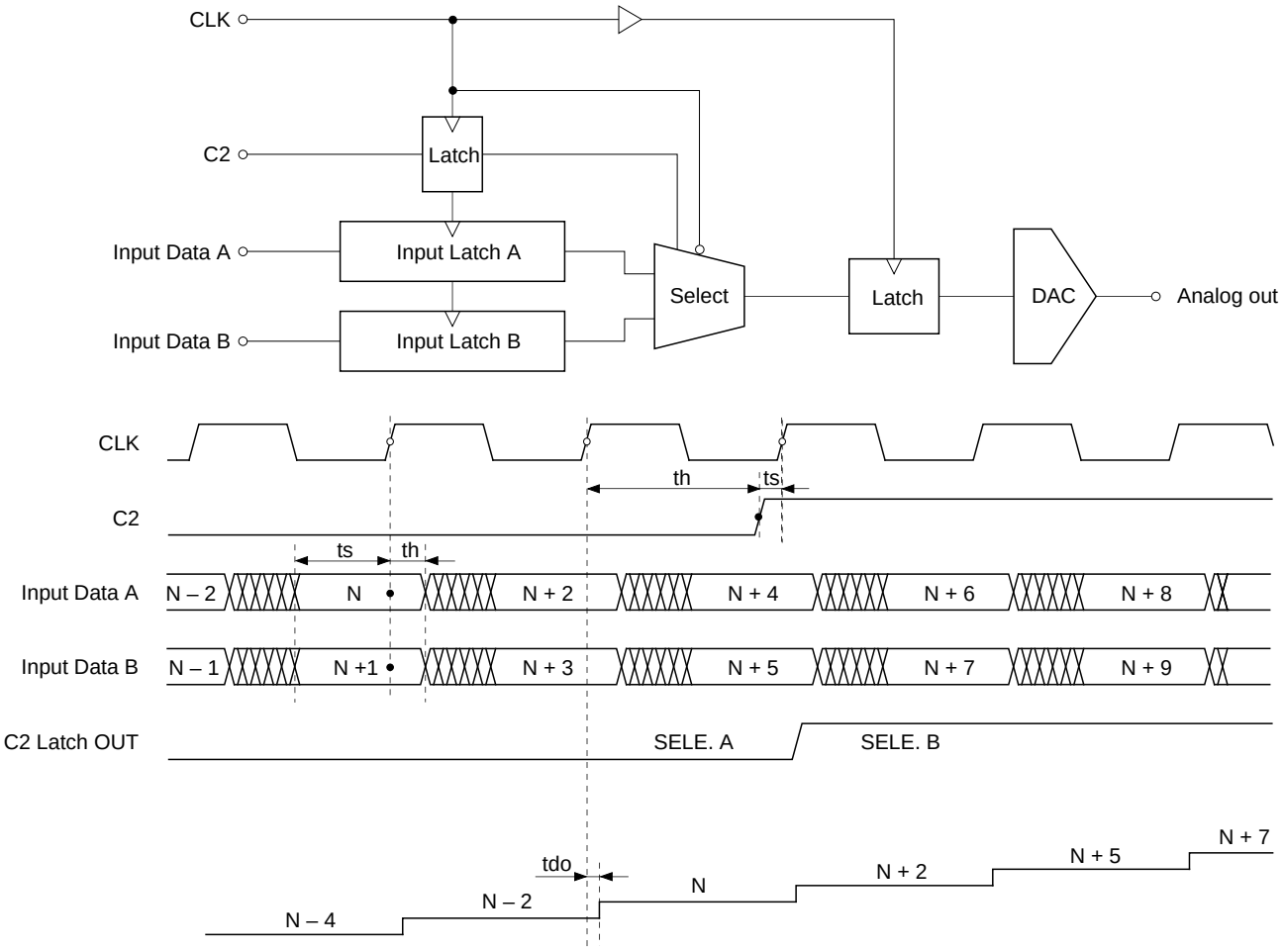
The frequency of the internal clock is halved by the built-in clock divider circuit. CLK/2 can be reset by the reset signal.

Block Diagram & Timing Chart (MUX.2 Mode)



For MUX.2 mode, the frequency-halved CLK/2 and Data A and Data B, which are synchronized with CLK/2, are provided simultaneously. They are internally multiplexed and the resulting signal can be analog output.

Block Diagram & Timing Chart (SELE.A , SELE.B Mode)



For SELE.A and SELE.B modes, input Data A or Data B is selected and the selected data can be analog output. In the state of C1=1, C3=0,Data A is selected for C2=0 and Data B is selected for C2=1.

Application Circuit

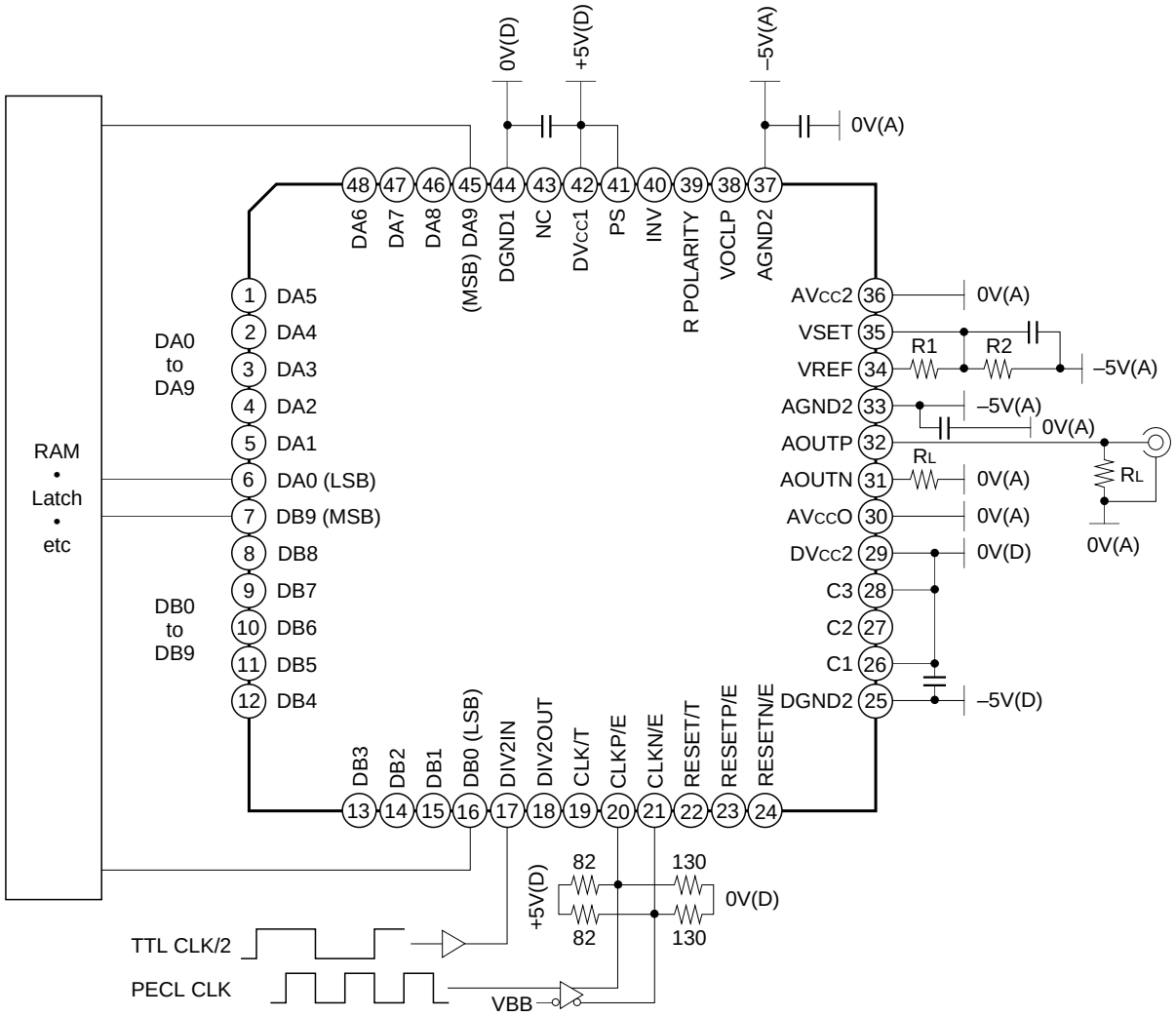
The circuit shown below is the basic circuit when the analog output is terminated with the external resistance of 50Ω in the dual ±5V power supplies for MUX.2 mode.
The analog output full-scale voltage V_{FS} is obtained with the following equation.

$$V_{FS} = \frac{V_{SET}}{375} \times (15 + \frac{63}{64}) \times R$$

R = Ro//RL
Ro: Output impedance (= 50Ω)
RL: External termination resistance

$$\text{Here, } V_{SET} = \frac{R2}{R1 + R2} V_{REF}$$

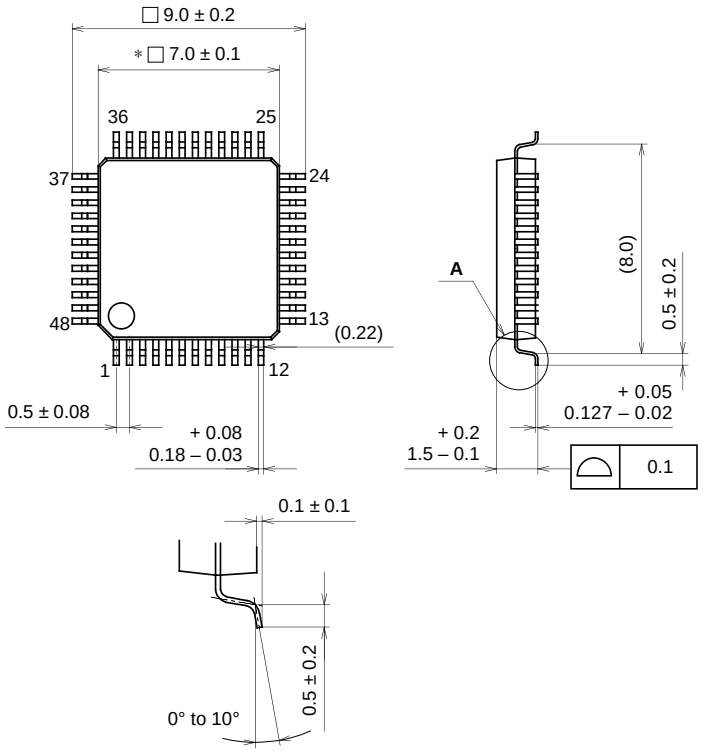
($V_{REF} \approx 1.2V$)
($R1 + R2 \geq 1.2k\Omega$)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g