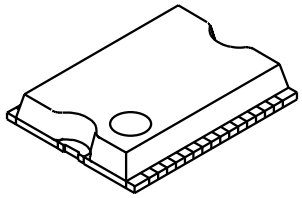
SONY

CXB1810FN

Post Amplifier for Optical Fiber Communication Receiver

16 pin HSOF (plastic)



Description

The CXB1810FN achieves 2R optical fiber communication receiver functions (Reshaping and Regenerating) on a single chip.

This IC is equipped with a signal detection function, and outputs at TTL level.

Features

- Auto-offset canceler circuit
- Signal interruption alarm output
- Single 3.3V or 5.0V power supply

Applications

SONET/SDH

Absolute Maximum Ratings

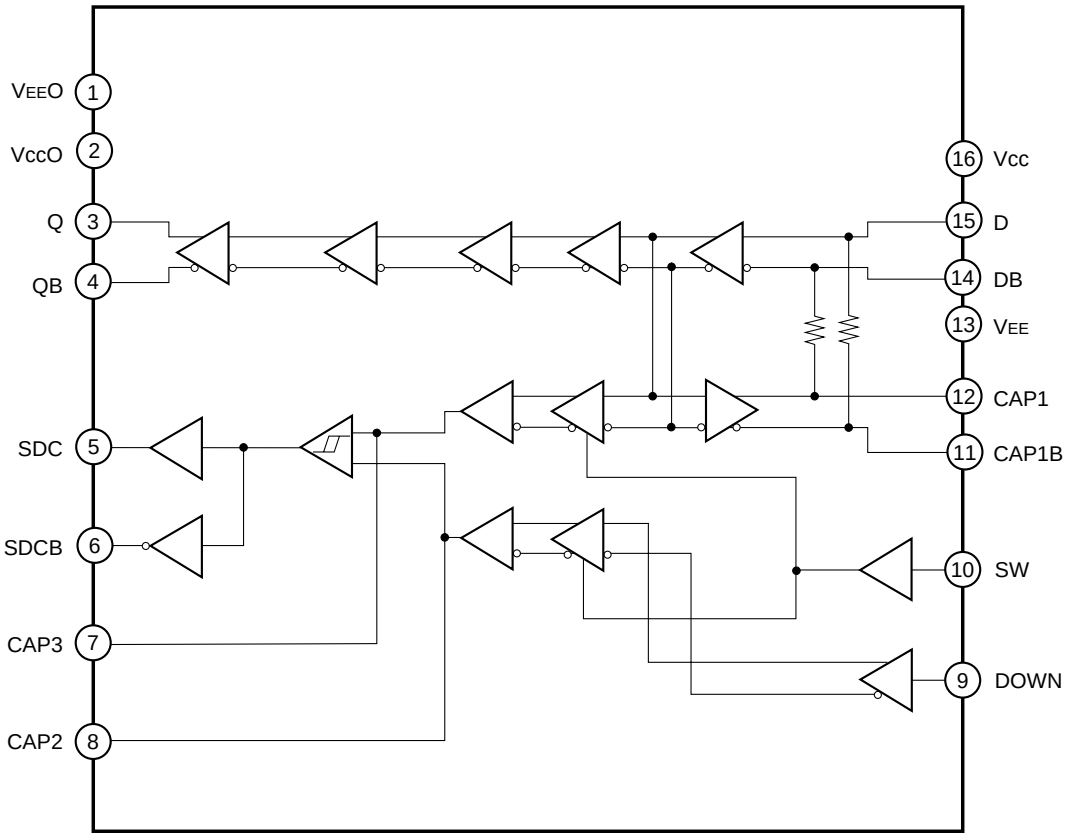
• Supply voltage	$V_{CC} - V_{EE}$	–0.3 to +6.0	V
• Input voltage difference	$\lvert V_D - V_{DN} \rvert$	2.5	V
• ECL/TTL output current (Continuous)		50	mA
(Surge)		70	mA
• Storage temperature	Tj	–65 to +150	°C

Recommended Operating Conditions

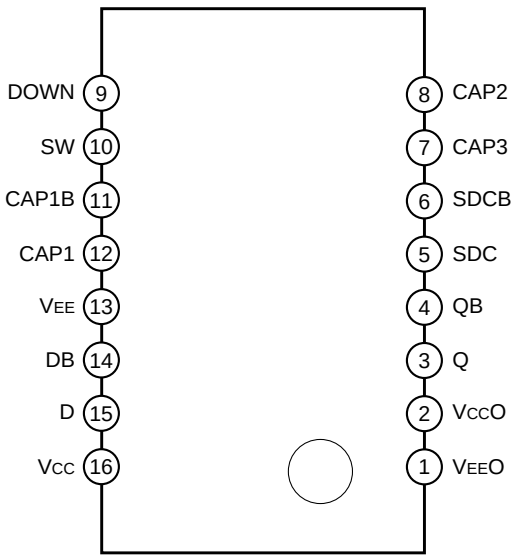
• Supply voltage	$V_{CC} - V_{EE}$	3.14 to 5.25	V
• Termination voltage (for Q/QB)	Vt1	V_{CC} – 1.8 to Vcc – 2.2	V
• Termination resistance (for Q/QB)	Rt	46 to 56	Ω
• Operating temperature	Ta	–40 to +85	°C

E99801B0Y-PS

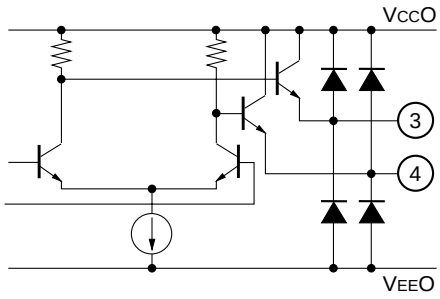
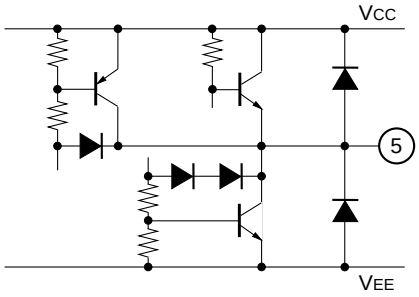
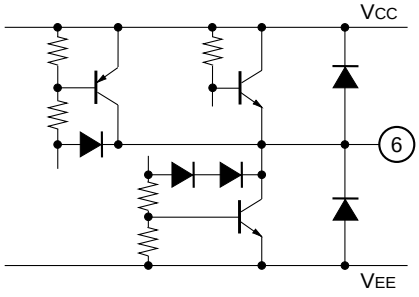
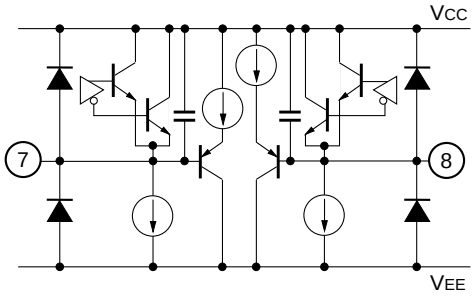
Block Diagram

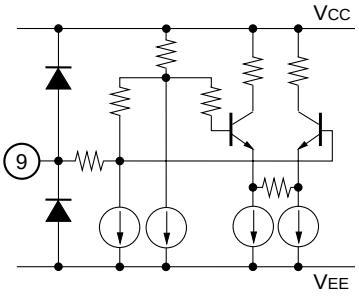
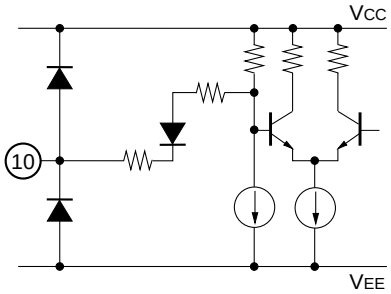
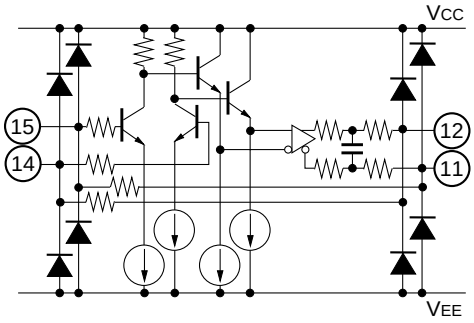


Pin Configuration



Pin Description

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
1	$V_{EE}O$	0			Ground for data output circuit.
2	VccO	3.3 or 5.0			Positive power supply for data output circuit.
3 4	Q QB		1.7 to 2.4 or 3.4 to 4.1		Data outputs.
5	SDC		0.2 to 2.9 or 0.2 to 4.7		Signal detection output (TTL). The SDC output is driven to low level while signal interruption is detected.
6	SDCB		0.2 to 2.9 or 0.2 to 4.7		Signal detection output (TTL). The SDCB output is driven to high level while signal interruption is detected.
7 8	CAP3 CAP2	 1.6 or 3.3	1.3 to 1.8 or 3.0 to 3.5		Connect a peak hold capacitor for the signal detection circuit. 470pF (typ.)

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
9	DOWN	2.4 or 4.1			Connect a resistor between this pin and the VCC pin to decrease the signal detection level from the default value.
10	SW				Switches the maximum identification voltage amplitude. This pin is set to 50mVp-p (single ended) when open or high level, or to 15mVp-p (single ended) when low level. Setting to low level is recommended when using a resistor of 510Ω or less between the VCC and DOWN pins.
11 12	CAP1B CAP1	2.2 or 3.9			Connect an external capacitor between these pins. 0.022µF (typ.)
14 15	DB D				Data inputs.
13	VEE	0			Ground.
16	VCC	3.3 or 5.0			Positive power supply.

Electrical Characteristics

DC Characteristics

(V_{CC} = 3.14 to 5.25V, Ta = –40 to +85°C, unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Q/QB high output voltage Q/QB low output voltage	VOH1 VOL1	51Ω terminated to V_{CC} – 2V 51Ω terminated to V_{CC} – 2V	V_{CC} – 1100 V_{CC} – 1800		V_{CC} – 650 V_{CC} – 1300	mV mV
Q/QB output amplitude	Vp	51Ω terminated to V_{CC} – 2V	500		1000	mVp-p
SDC/SDCB high output voltage SDC/SDCB low output voltage	VOHT VOLT	IOH = –0.2mA IOL = 2.1mA	2.4		 0.5	V V
SW high input voltage SW low input voltage	VIHT VILT		V_{CC} – 0.3 V_{EE}		V_{CC} V_{EE} + 0.3	V V
Maximum input voltage amplitude	Vmax	During single-phase input	1000			mVp-p
D/DB input resistance	Rin		33	50	69	Ω
Supply current	ICC	All outputs open		40	55	mA

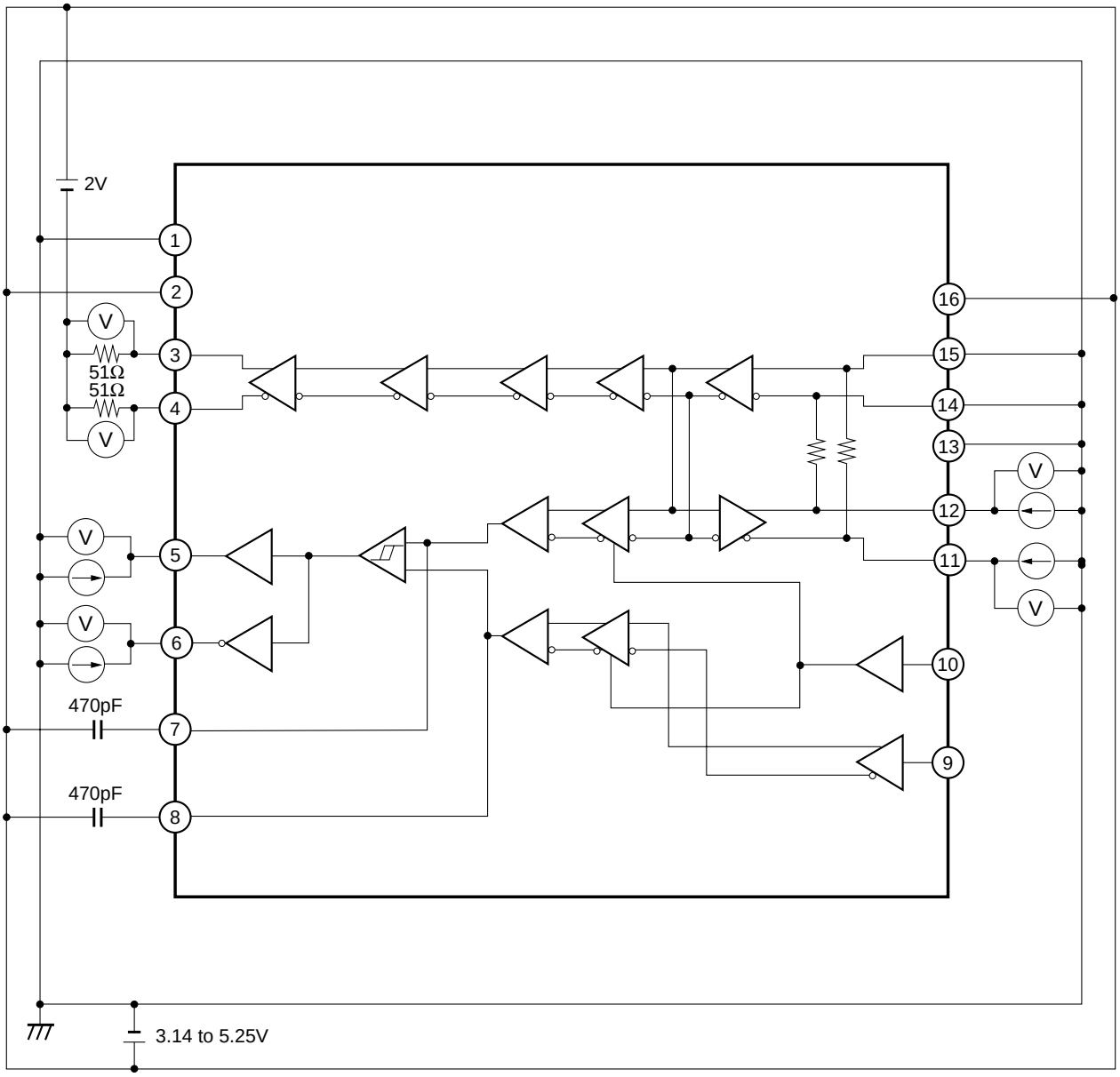
AC Characteristics

(V_{CC} = 3.14 to 5.25V, Ta = –40 to +85°C, unless otherwise specified)

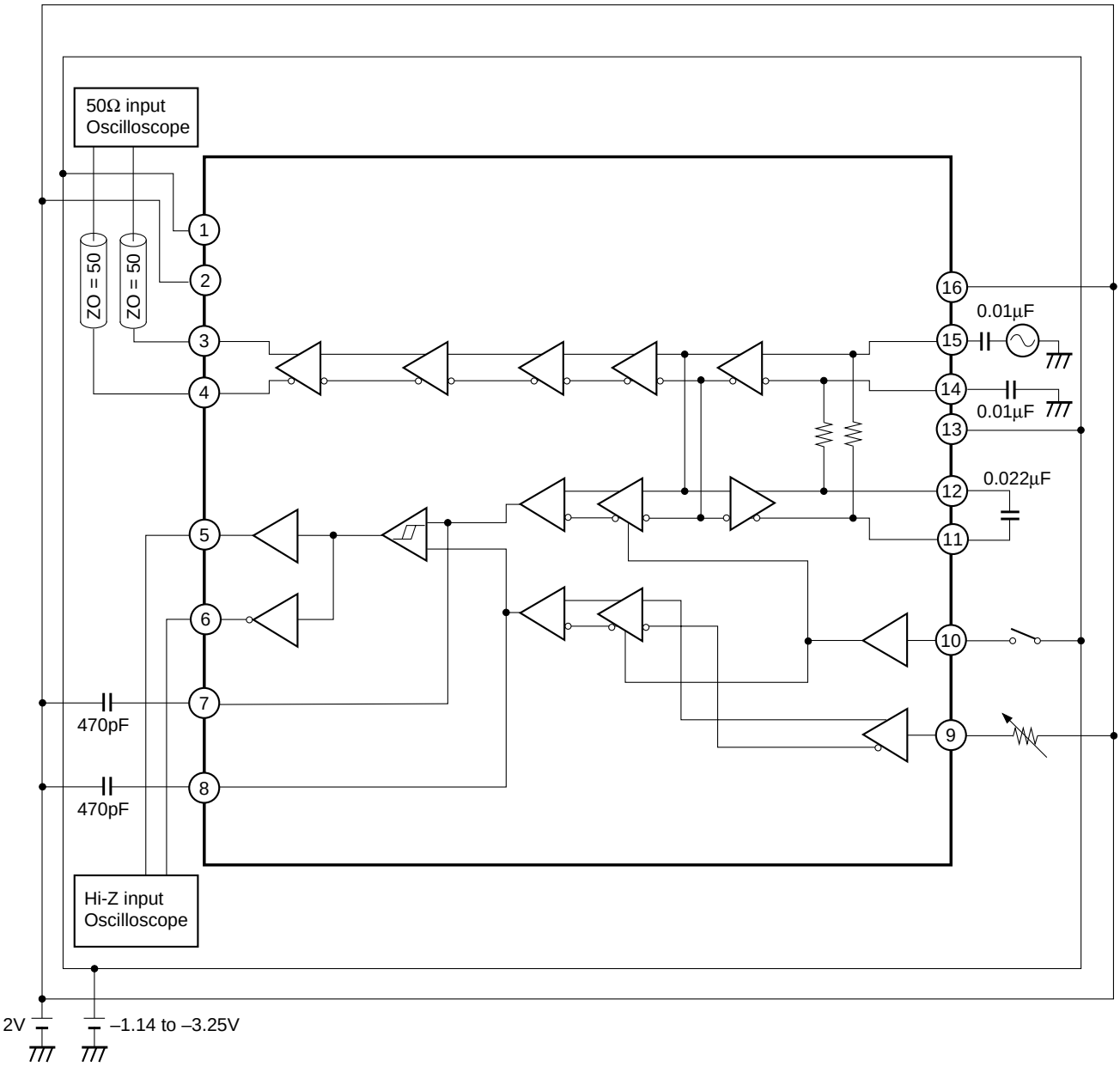
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Limiting amplifier gain	GL		45			dB
Signal detection threshold voltage	Vth	During single ended input		34		mVp-p
Signal detection hysteresis width	ΔP		3	6	8	dB
Signal detection response assert time*1 Signal detection response deassert time*1	Tas Tdas		0 2.3		100 100	µs µs
Q/QB rise time (20 to 80%) Q/QB fall time (20 to 80%)	TR TF	51Ω terminated to V_{CC} – 2V 51Ω terminated to V_{CC} – 2V		130 110		ps ps

*1 Data = PN23 – 1 pattern, 100mVp-p single ended, Rd = open, CAP2/CAP3 = 470pF

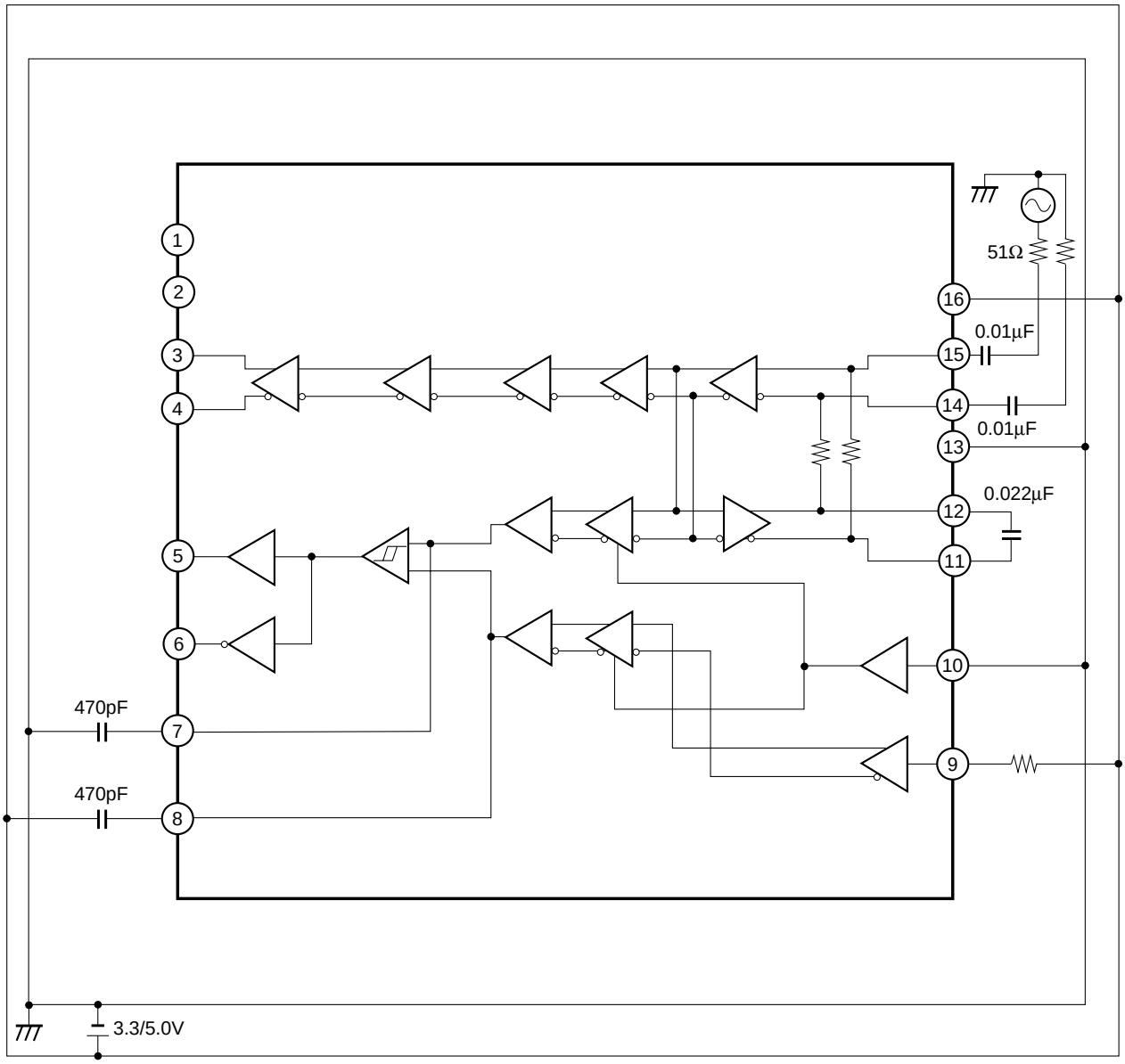
DC Electrical Characteristics Measurement Circuit



AC Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1. Limiting amplifier block

The limiting amplifier block is equipped with an auto-offset canceler circuit. When external capacitors C1 and C2 are connected as shown in Fig. 1, the DC bias is set automatically in this block.
External capacitor C1 and internal resistor R1 determine the input low cut-off frequency f2 as shown in Fig. 2. Similarly, external capacitor C2 and internal resistor R2 determine the high cut-off frequency for DC feedback. Since a peak may occur in the low frequency area of the gain characteristics depending on the f1/f2 combination, set the C1 and C2 values so as to avoid the occurrence of this peak. The typical values of R1, R2, C1 and C2 are indicated below.
Also, when a single ended input is used, provide AC grounding by connecting Pin 14 to a capacitor which has the same capacitance as capacitor C1.

R1 (internal): 50Ω
C1 (external): 0.01µF
f2: 318kHz

R2 (internal): 10kΩ
C2 (external): 0.022µF
f1: 723Hz

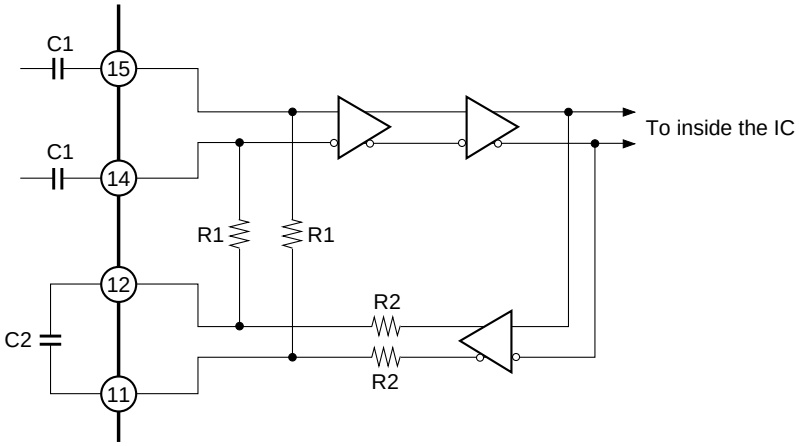


Fig. 1

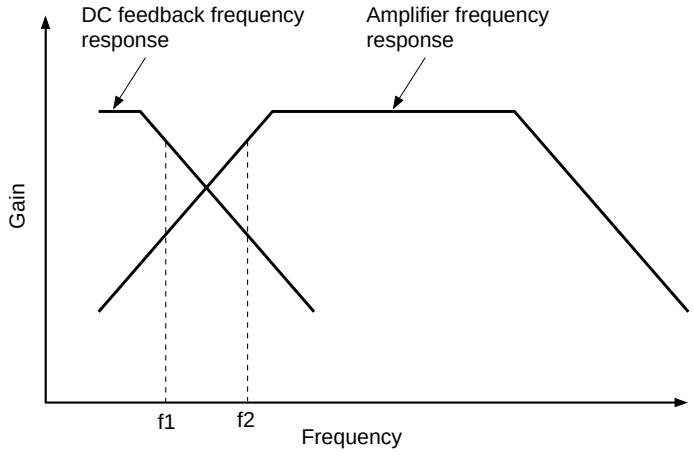


Fig. 2

2. Alarm block

In this block, the input signal amplitude is detected and the signal interruption alarm is output when the amplitude becomes lower than the set alarm level. The alarm level setting can be adjusted by connecting an external resistor Rd between the DOWN and V_{CC} pins.
Also, this IC can set the maximum identification voltage amplitude to two levels. The maximum identification voltage amplitude is set to 50mVp-p (single ended) when the SW pin is open or high level, or to 15mVp-p (single ended) when the SW pin is low level.
Figs. 15 and 16 show the relation of Rd and the alarm assert/deassert level. Setting the SW pin to low level is recommended when Rd is 510Ω or less.

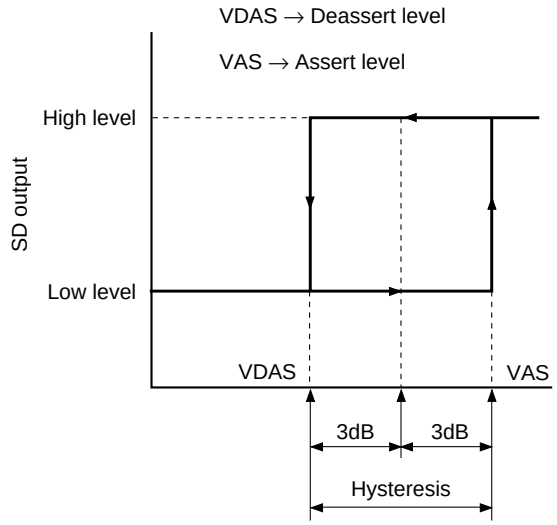


Fig. 3

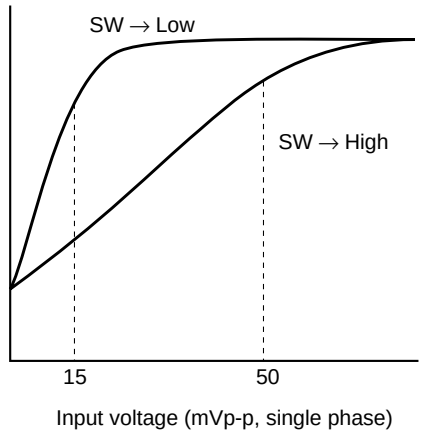


Fig. 4

In addition, the SD response deassert time is guaranteed only under the conditions noted in the AC Electrical Characteristics item, but the response becomes delayed as the input signal amplitude becomes larger. This is because the input resistor R1 shown in Fig. 1 is small at 50Ω, so the charge accumulated in C2 is relatively large and the discharge time for this charge accounts for most of the SD response deassert time. The SD response deassert time can be shortened by using the external circuit shown in Fig. 5 or by shorting the CAP1 and CAP1B pins. However, care should be taken as the auto-offset canceler circuit does not operate in this case causing the reception sensitivity to deteriorate. Fig. 14 shows the relation between the SD response deassert time and the electrical input amplitude when using the connection shown in Fig. 5.

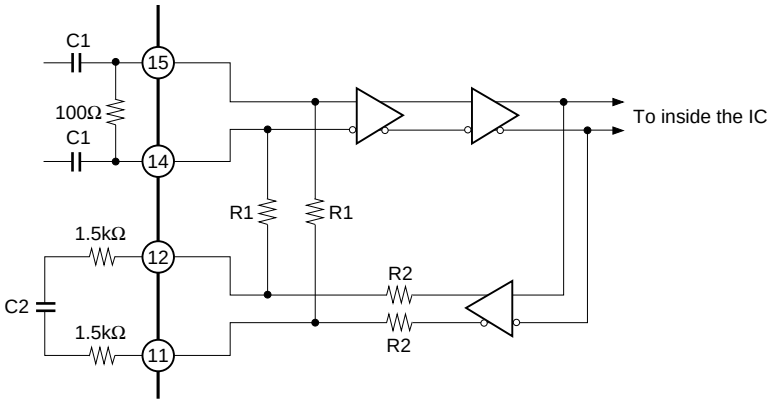
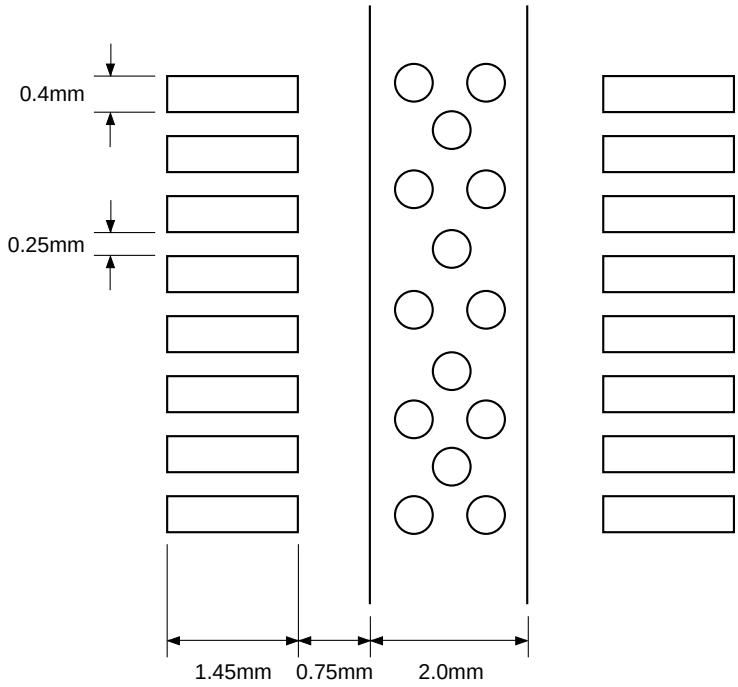


Fig. 5

3. Substrate layout

The exposed metal portions on the rear surface of the package used for the CXB1810FN are electrically connected to the silicon substrate. Superior thermal radiation characteristics can be obtained by connecting the rear surface of the package and these exposed metal portions to the ground surface on the PCB. Providing lands directly below the package as shown in the figure below and connecting as many thermal vias as possible to the inner layer ground surface is recommended.



4. Other

- Be careful when handling this IC as its electrostatic discharge strength is weak.
- Be sure to connect all power supply pins ($V_{CC}O$, V_{CC}) and ground pins ($V_{EE}O$, V_{EE}) to power supplies or grounds, respectively. For example, if only $V_{CC}O$ is left open and power is supplied to the other pin, the IC may malfunction.

Example of Representative Characteristics

ICC vs. Supply voltage

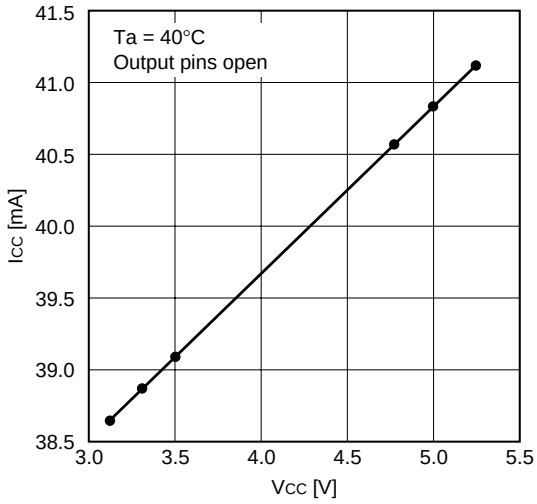


Fig. 6

ICC vs. Temperature

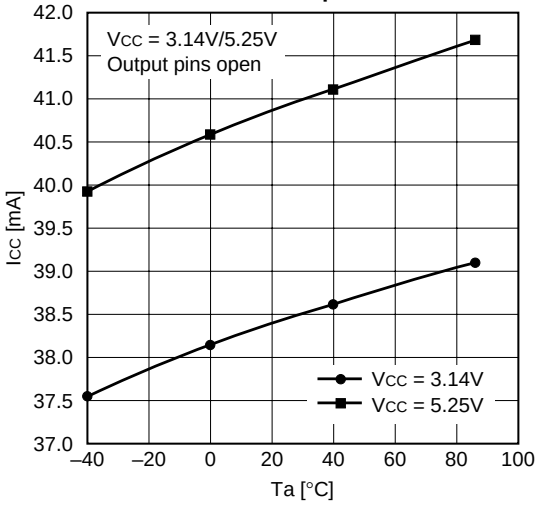


Fig. 7

Q/QB output voltage vs. Supply voltage

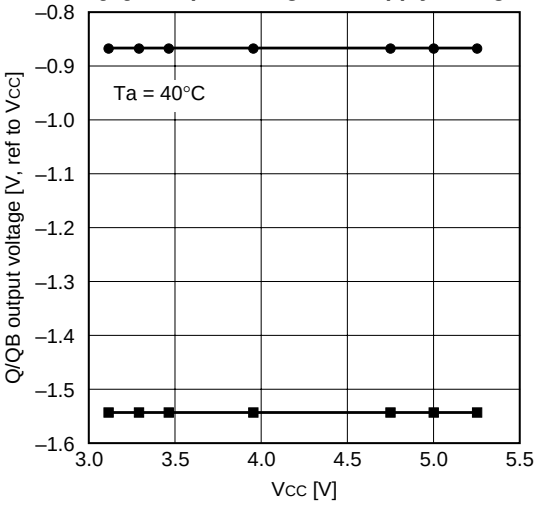


Fig. 8

Q/QB output voltage vs. Temperature

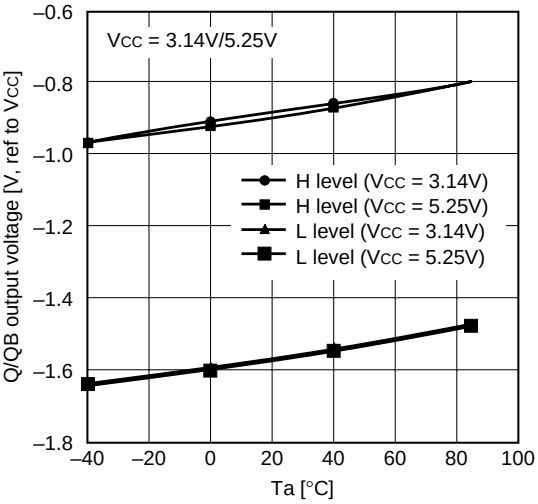


Fig. 9

Q/QB output voltage amplitude vs. Supply voltage

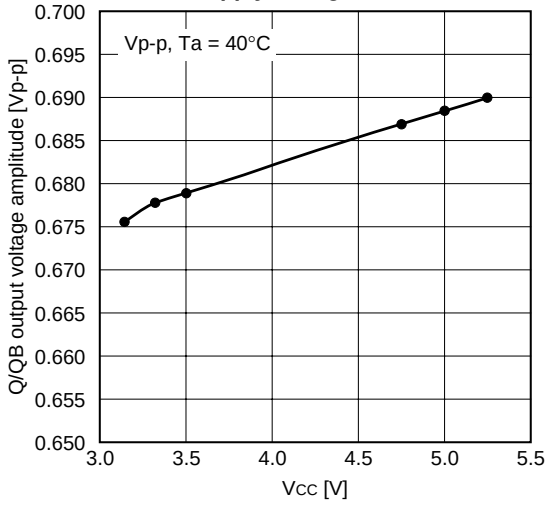


Fig. 10

Q/QB output voltage amplitude vs. Temperature

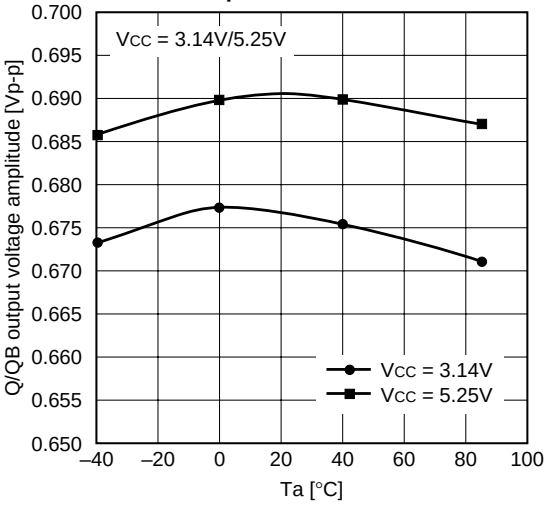


Fig. 11

SDC/SDCB output voltage vs. Supply voltage

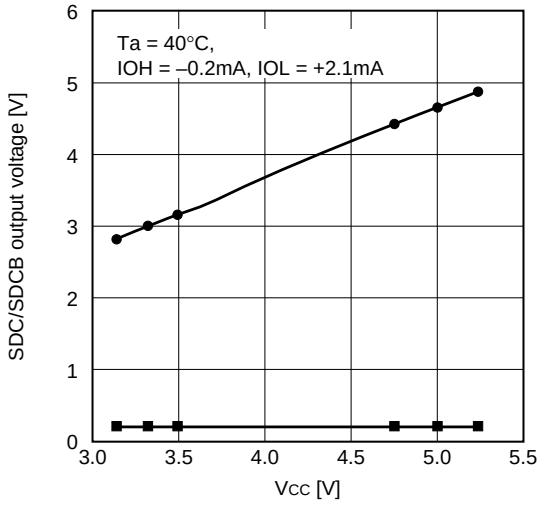


Fig. 12

SDC/SDCB output voltage vs. Temperature

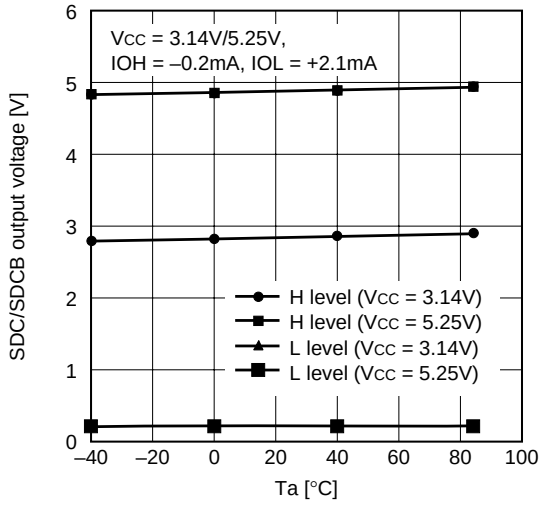


Fig. 13

Input voltage amplitude vs. SD response deassert time

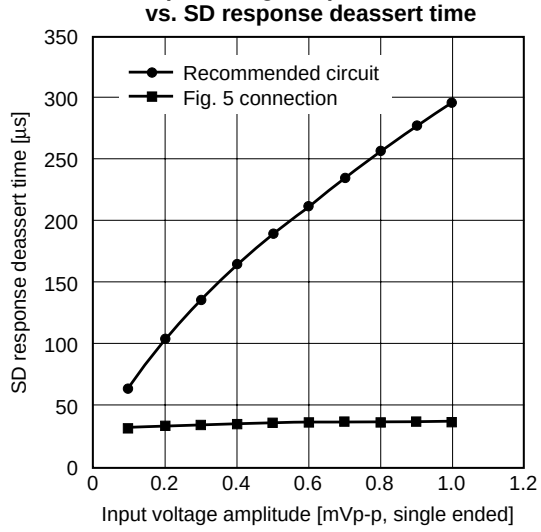


Fig. 14

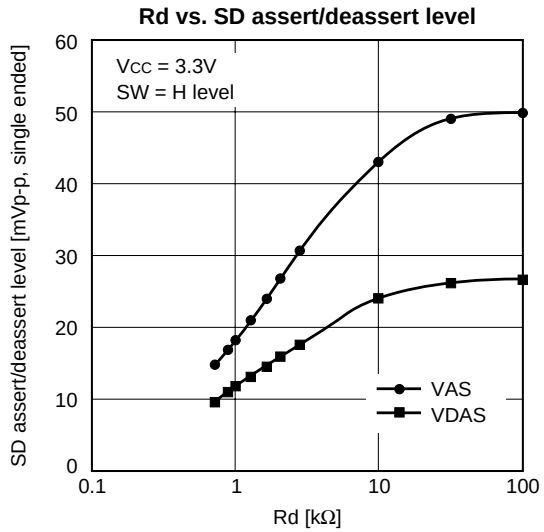


Fig. 15

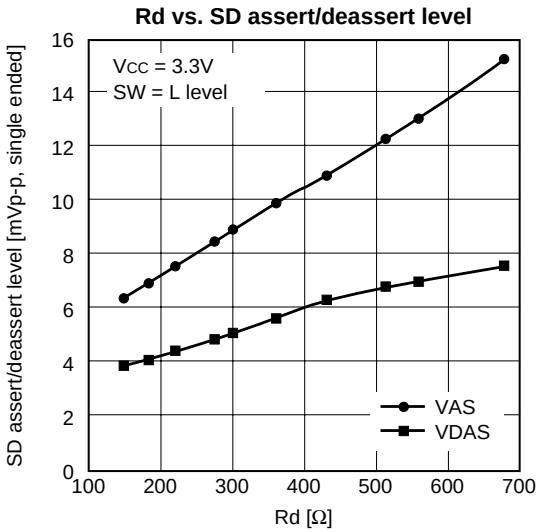


Fig. 16

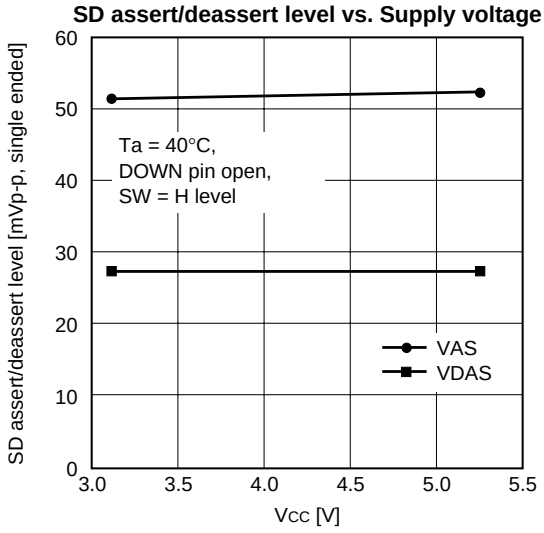


Fig. 17

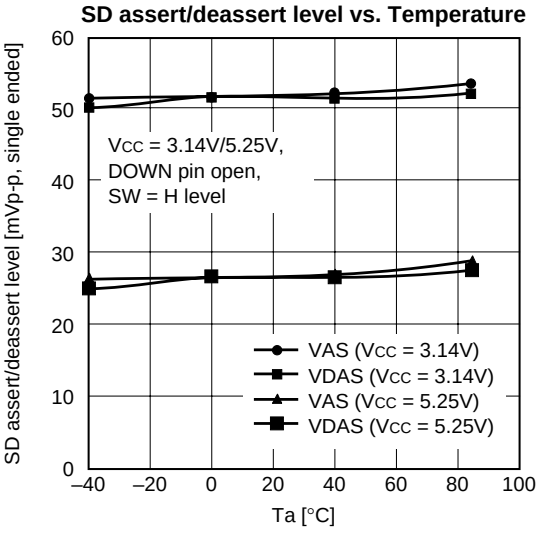


Fig. 18

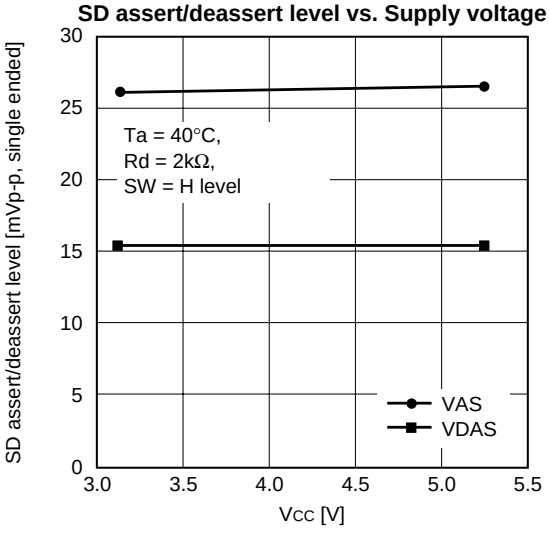


Fig. 19

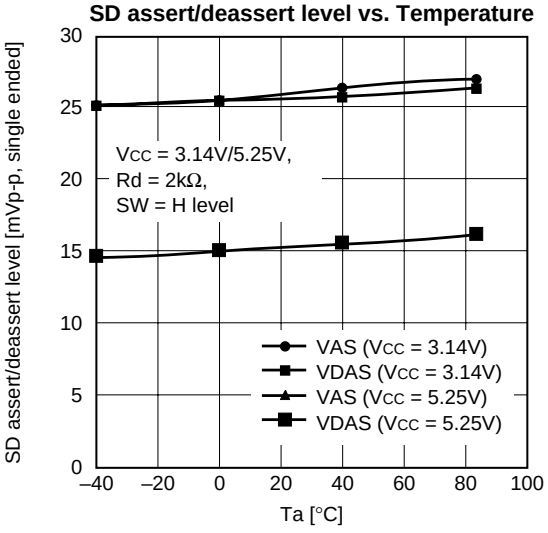


Fig. 20

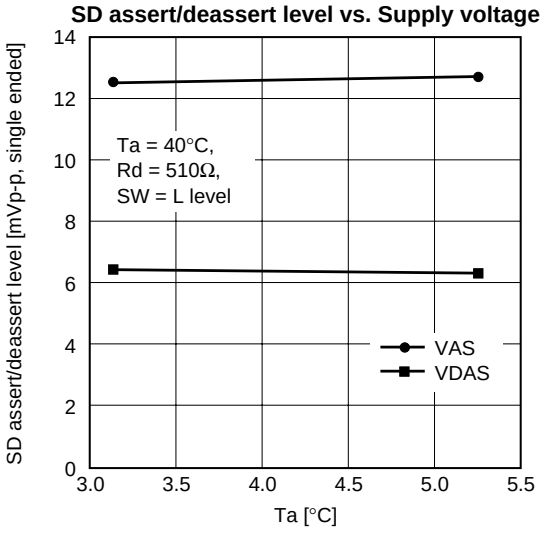


Fig. 21

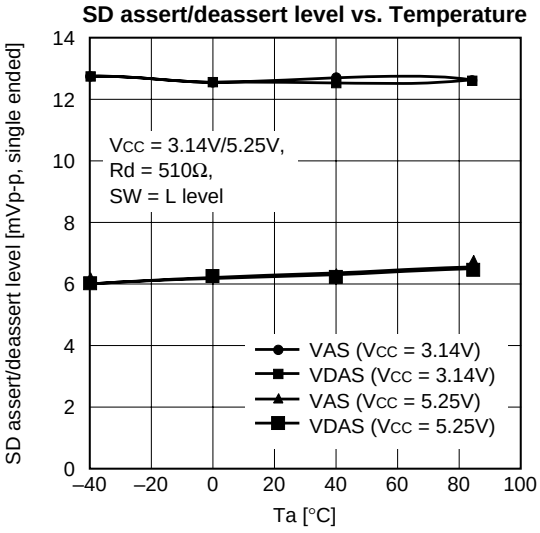


Fig. 22

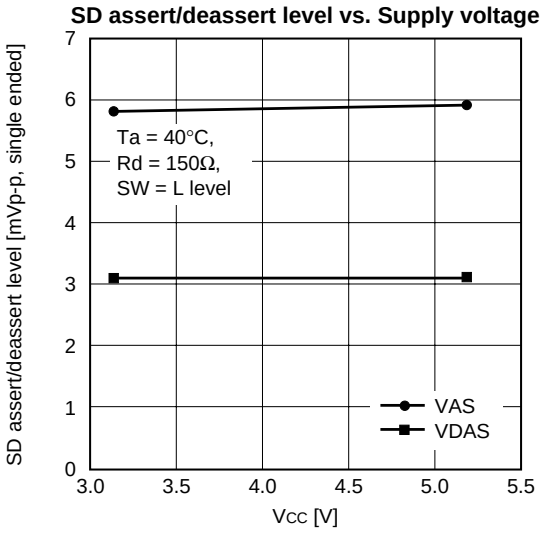


Fig. 23

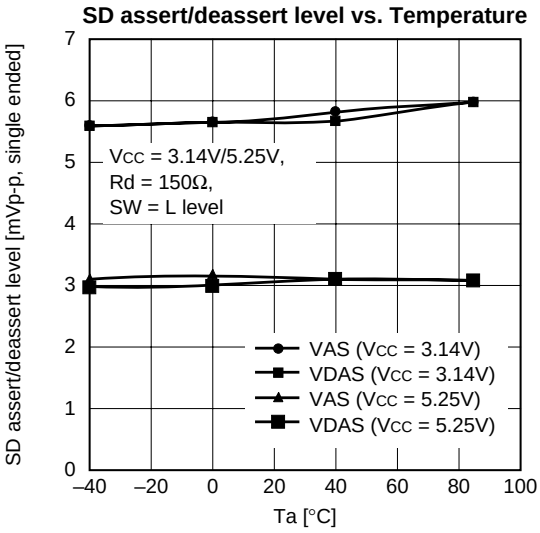


Fig. 24

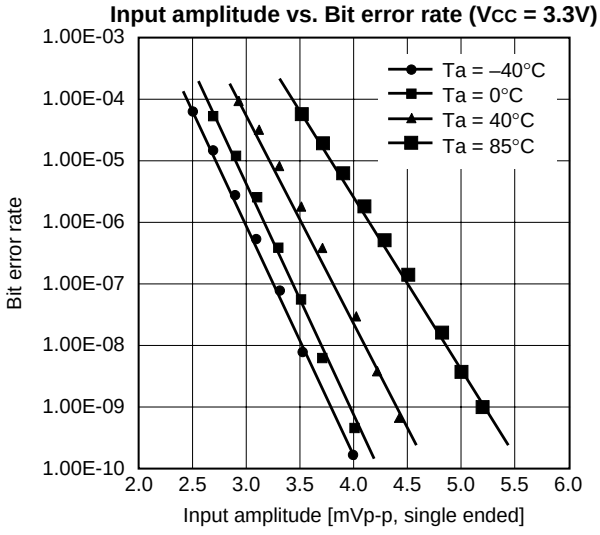


Fig. 25

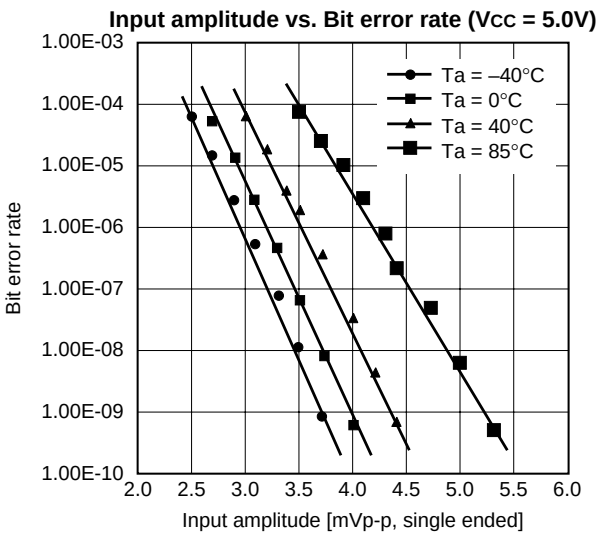
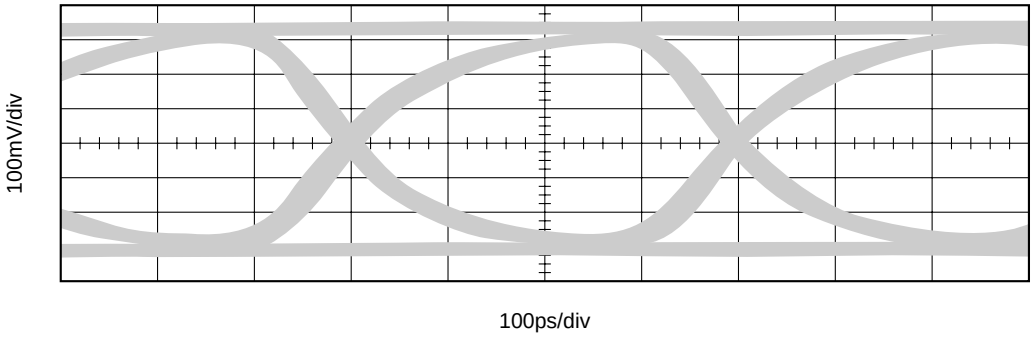
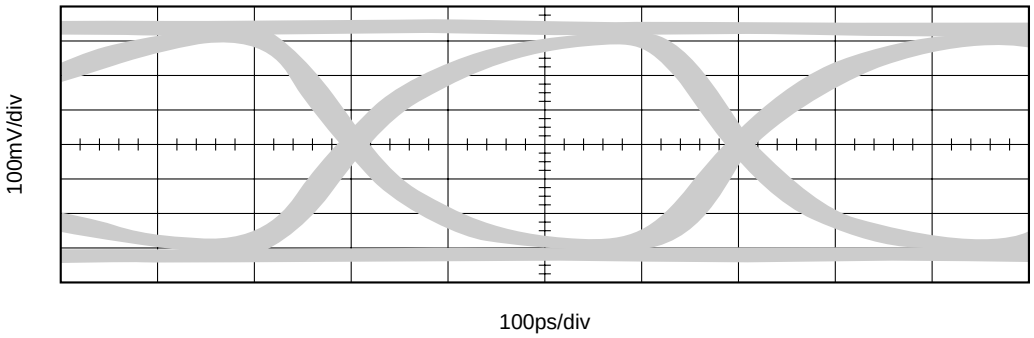


Fig. 26



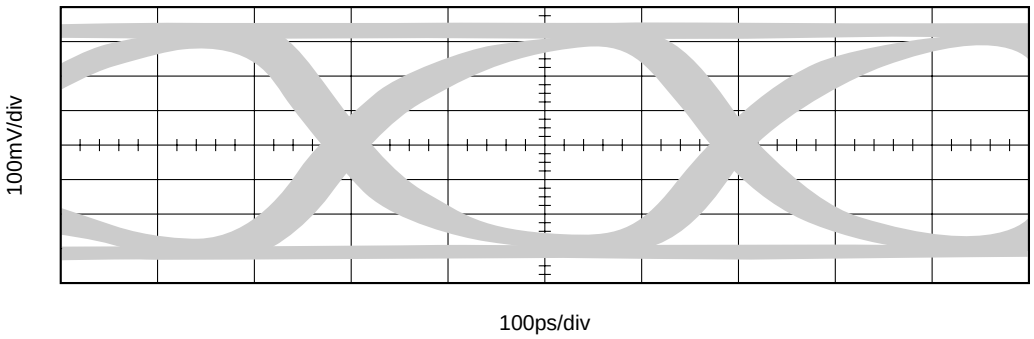
Q output waveform
V_{CC} = 3.3V, Ta = 40°C
D = 100mVp-p
(single ended)
PN23 pattern

Fig. 27



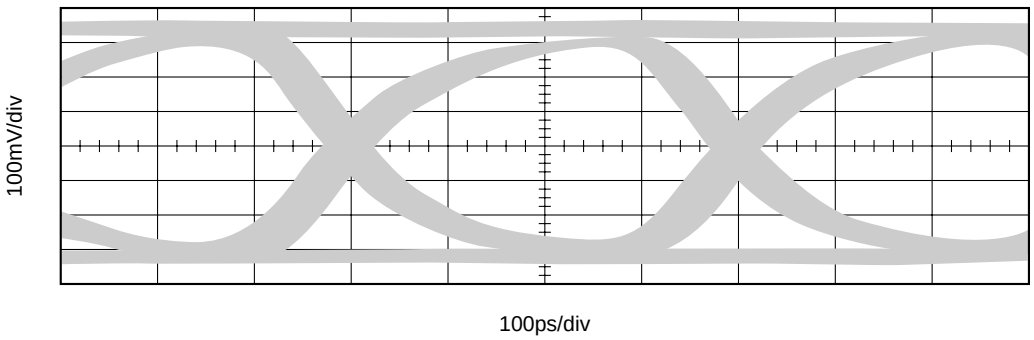
Q output waveform
V_{CC} = 5.0V, Ta = 40°C
D = 100mVp-p
(single ended)
PN23 pattern

Fig. 28



Q output waveform
V_{CC} = 3.3V, Ta = 40°C
D = 10mVp-p
(single ended)
PN23 pattern

Fig. 29

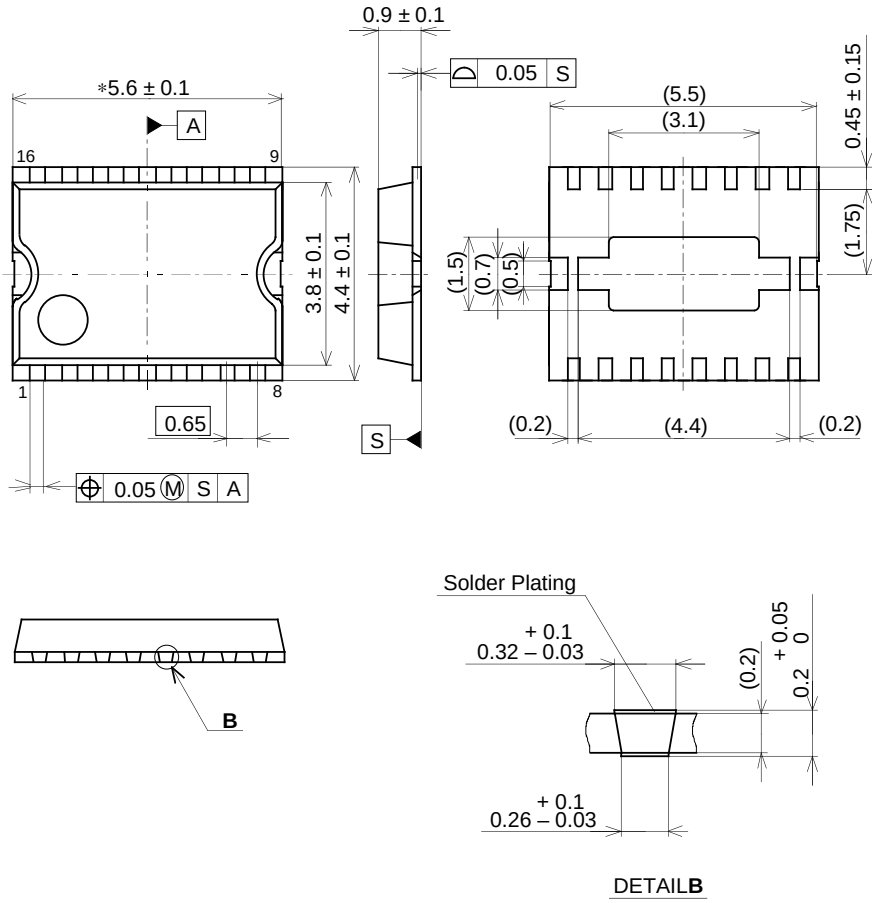


Q output waveform
V_{CC} = 5.0V, Ta = 40°C
D = 10mVp-p
(single ended)
PN23 pattern

Fig. 30

Package Outline Unit: mm

HSOF 16PIN(PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	HSOF-16P-02
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.06g