

# CXD1175AM/AP

## 8-bit 20MSPS Video A/D Converter (CMOS)

**Description**

The CXD1175A is an 8-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low consumption at a maximum conversion speed of 20MSPS minimum, 35MSPS typical.

**Features**

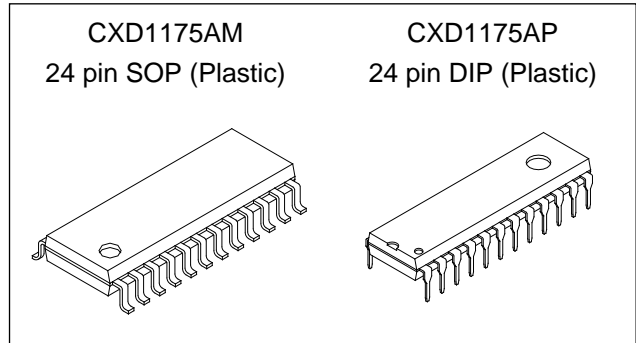
- Resolution: 8 bit  $\pm 1/2$ LSB (DL)
- Maximum sampling frequency: 20MSPS
- Low power consumption: 60mW (at 20MSPS typ.) (reference current excluded)
- Built-in sampling and hold circuit
- Built-in reference voltage self-bias circuit
- 3-state TTL compatible output
- Power supply: 5V single
- Low input capacitance: 11pF
- Reference impedance: 300 $\Omega$  (typ.)

**Applications**

TV, VCR digital systems and a wide range of fields where high speed A/D conversion is required.

**Structure**

Silicon gate CMOS monolithic IC



**Absolute Maximum Ratings (Ta = 25°C)**

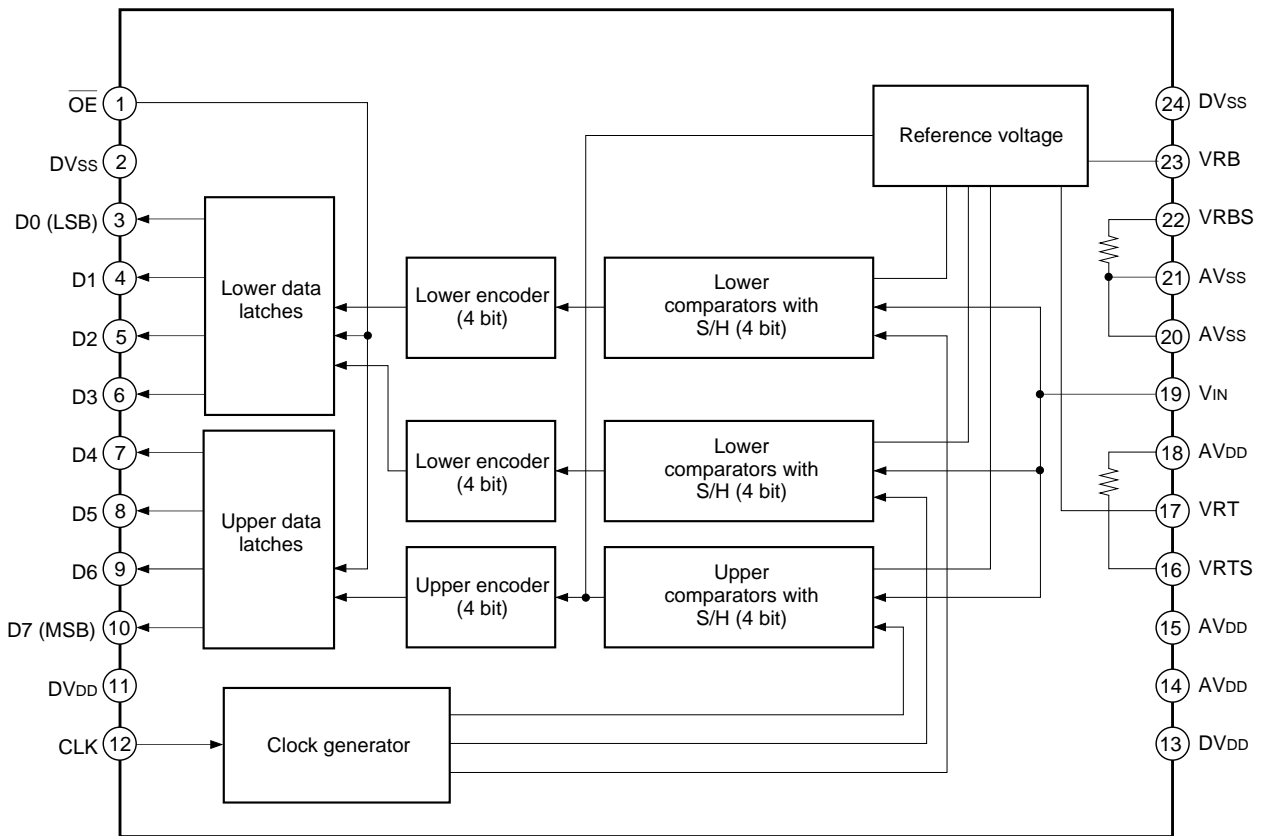
• Supply voltage	V <sub>DD</sub>	7	V
• Reference voltage	V <sub>RT</sub> , V <sub>RB</sub>	V <sub>DD</sub> + 0.5 to V <sub>SS</sub> - 0.5V	
• Input voltage (Analog)	V <sub>IN</sub>	V <sub>DD</sub> + 0.5 to V <sub>SS</sub> - 0.5V	
• Input voltage (Digital)	V <sub>I</sub>	V <sub>DD</sub> + 0.5 to V <sub>SS</sub> - 0.5V	
• Output voltage (Digital)	V <sub>O</sub>	V <sub>DD</sub> + 0.5 to V <sub>SS</sub> - 0.5V	
• Storage temperature	T <sub>stg</sub>	-55 to +150	°C

**Recommended Operating Conditions**

• Supply voltage	A <sub>VDD</sub> , A <sub>VSS</sub>	4.75 to 5.25	V
	D <sub>VDD</sub> , D <sub>VSS</sub>	D <sub>VSS</sub> - A <sub>VSS</sub>	0 to 100 mV
• Reference input voltage	V <sub>RB</sub>	0 and above	V
	V <sub>RT</sub>	2.8 and below	V
• Analog input	V <sub>IN</sub>	1.8Vp-p above	
• Clock pulse width	T <sub>PW1</sub> , T <sub>PW0</sub>	23ns (min) to 1.1 $\mu$ s (max)	
• Operating ambient temperature	T <sub>opr</sub>	-40 to +85	°C

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Block Diagram and Pin Configuration



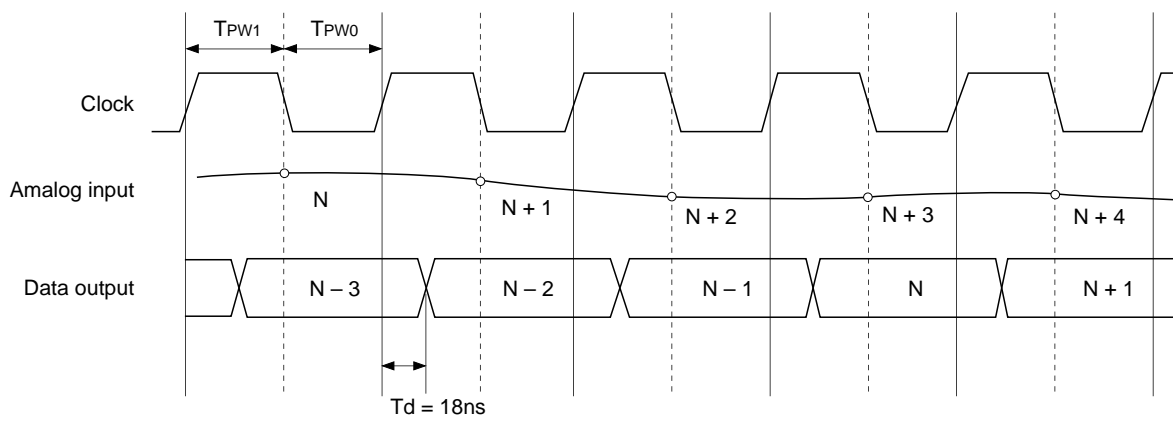
Pin Description and Equivalent Circuits

No.	Symbol	Equivalent circuit	Description
1	$\overline{OE}$		When $\overline{OE}$ = Low, Data is output. When $\overline{OE}$ = High, D0 to D7 pins turn to High impedance.
2, 24	DVSS		Digital ground
3 to 10	D0 to D7		D0 (LSB) to D7 (MSB) output
11, 13	DVDD		Digital +5V
12	CLK		Clock input
16	VRTS		Shorted with VRT generates, +2.6V.
17	VRT		Reference voltage (Top)
23	VRB		Reference voltage (Bottom)
14, 15, 18	AVDD		Analog +5V
19	V <sub>IN</sub>		Analog input
20, 21	AVSS		Analog GND
22	VRBS		Shorted with VRB generates +0.6V.

**Digital output**

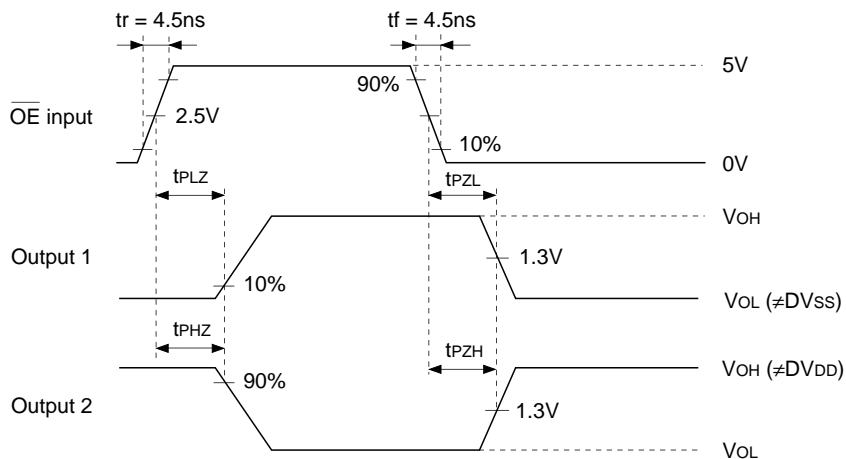
Compatibility between analog input voltage and the digital output code is indicated in the chart below.

Input signal voltage	Step	Digital output code	
		MSB	LSB
V <sub>RT</sub>	0	1	1 1 1 1 1 1 1 1
⋮	⋮		⋮
⋮	127	1	0 0 0 0 0 0 0 0
⋮	128	0	1 1 1 1 1 1 1 1
⋮	⋮		⋮
V <sub>RB</sub>	255	0	0 0 0 0 0 0 0 0



○ : Point for analog signal sampling.

**Timing Chart 1**



**Timing Chart 2**

## Electrical Characteristics

## Analog characteristics

(F<sub>C</sub> = 20MSPS, V<sub>DD</sub> = 5V, V<sub>RB</sub> = 0.5V, V<sub>RT</sub> = 2.5V, T<sub>a</sub> = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Conversion speed	F <sub>C</sub>	V <sub>DD</sub> = 4.75 to 5.25V T <sub>a</sub> = -40 to +85°C V <sub>IN</sub> = 0.5 to 2.5V f <sub>IN</sub> = 1kHz ramp	0.5		20	MSPS
Analog input band width (-1dB)	BW	Envelope		18		MHz
Offset voltage*1	E <sub>OT</sub>	Potential difference to V <sub>RT</sub>	-10	-35	-60	mV
	E <sub>OB</sub>	Potential difference to V <sub>RB</sub>	0	+15	+45	
Integral non-linearity error	E <sub>L</sub>	End point		+0.5	+1.3	LSB
Differential non-linearity error	E <sub>D</sub>			±0.3	±0.5	
Differential gain error	DG	NTSC 40 IRE mod ramp F <sub>C</sub> = 14.3MSPS		1.0		%
Differential phase error	DP			0.5		deg
Aperture jitter	t <sub>aj</sub>			30		ps
Sampling delay	t <sub>sd</sub>			4		ns

\*1 The offset voltage E<sub>OB</sub> is a potential difference between V<sub>RB</sub> and a point of position where the voltage drops equivalent to 1/2 LSB of the voltage when the output data changes from "00000000" to "00000001".  
E<sub>OT</sub> is a potential difference between V<sub>RT</sub> and a potential of point where the voltage rises equivalent to 1/2LSB of the voltage when the output data changes from "11111111" to "11111110".

**DC characteristics**

( $F_c = 20\text{MSPS}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{RB} = 0.5\text{V}$ ,  $V_{RT} = 2.5\text{V}$ ,  $T_a = 25^\circ\text{C}$ )

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply current	$I_{DD}$	$F_c = 20\text{MSPS}$ NTSC ramp wave input			12	17	mA
Reference pin current	$I_{REF}$			4.5	6.6	8.7	mA
Analog input capacitance	$C_{IN}$	$V_{IN} = 1.5\text{V} + 0.07\text{V}_{rms}$			11		pF
Reference resistance ( $V_{RT}$ to $V_{RB}$ )	$R_{REF}$			230	300	450	$\Omega$
Self-bias I	$VRB_1$	Shorts $VRB$ and $VRBS$ Shorts $V_{RT}$ and $V_{RTS}$		0.60	0.64	0.68	V
	$V_{RT1} - VRB_1$			1.96	2.09	2.21	
Self-bias II	$V_{RT2}$	$VRB = AGND$ Shorts $V_{RT}$ and $V_{RTS}$		2.25	2.39	2.53	V
Digital input voltage	$V_{IH}$	$V_{DD} = 4.75$ to $5.25\text{V}$ $T_a = -40$ to $+85^\circ\text{C}$		3.5			V
	$V_{IL}$					1.0	
Digital input current	$I_{IH}$	$V_{DD} = \text{max}$	$V_{IH} = V_{DD}$			5	$\mu\text{A}$
	$I_{IL}$		$V_{IL} = 0\text{V}$			5	
Digital output current	$I_{OH}$	$\overline{OE} = V_{SS}$ $V_{DD} = \text{min}$	$V_{OH} = V_{DD} - 0.5\text{V}$	-1.1			mA
	$I_{OL}$		$V_{OL} = 0.4\text{V}$	3.7			
	$I_{OZH}$	$\overline{OE} = V_{DD}$ $V_{DD} = \text{max}$	$V_{OH} = V_{DD}$			16	$\mu\text{A}$
	$I_{OZL}$		$V_{OL} = 0\text{V}$			16	

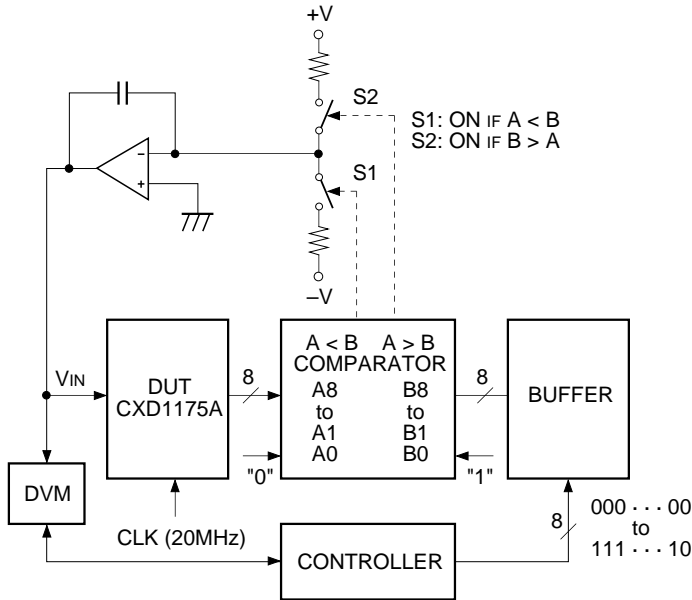
**Timing**

( $F_c = 20\text{MSPS}$ ,  $V_{DD} = 4.75$  to  $5.25\text{V}$ ,  $V_{RB} = 0.5\text{V}$ ,  $V_{RT} = 2.5\text{V}$ ,  $T_a = -40$  to  $+85^\circ\text{C}$ )

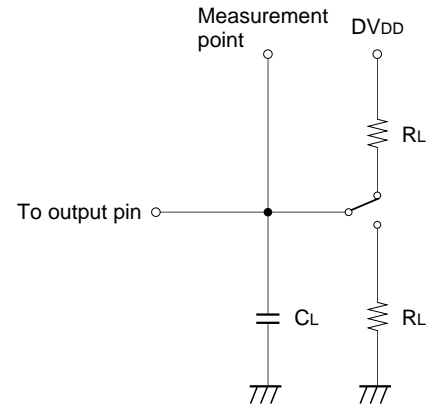
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output data delay	$T_{DL}$	With TTL 1 gate and 10pF load		18	30	ns
Tri-state output enable time	$t_{PZH}$	$R_L = 1\text{k}\Omega$ , $C_L = 20\text{pF}$ $\overline{OE} = 5\text{V} \rightarrow 0\text{V}$	3	7	13	ns
	$t_{PZL}$					
Tri-state output disable time	$t_{PHZ}$	$R_L = 1\text{k}\Omega$ , $C_L = 20\text{pF}$ $\overline{OE} = 0\text{V} \rightarrow 5\text{V}$	7	15	26	ns
	$t_{PLZ}$					

**Electrical Characteristics Measurement Circuit**

Integral non-linearity error } measurement circuit  
 Differential non-linearity error }  
 Offset voltage }

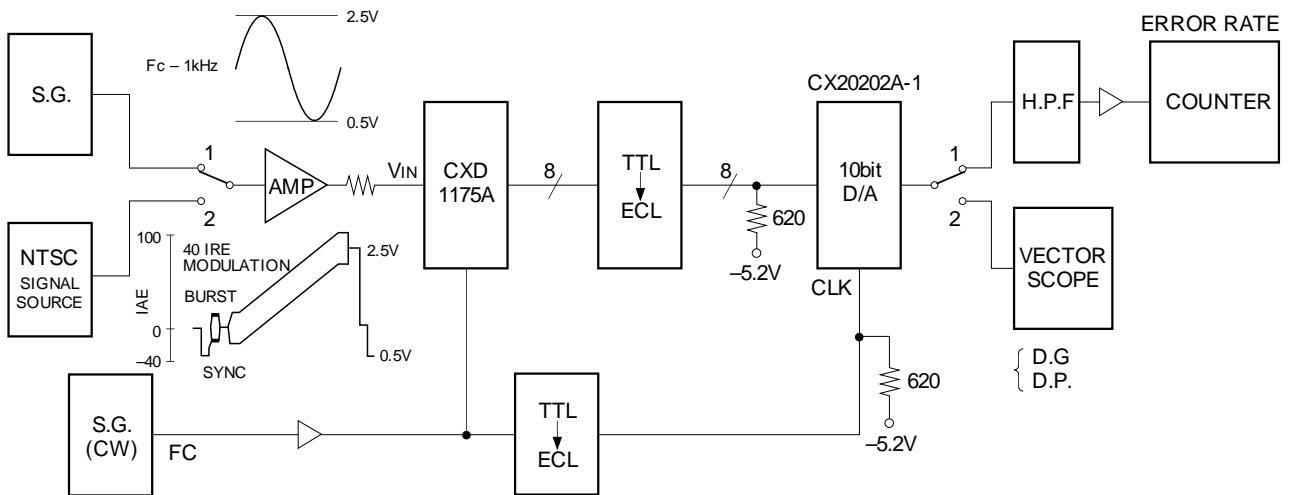


**3-state output measurement circuit**

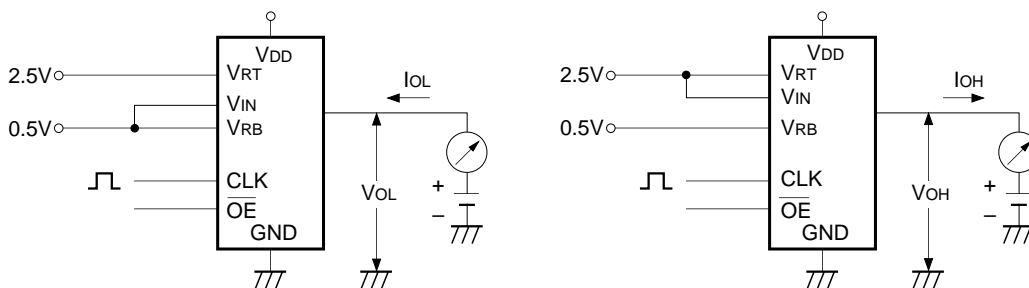


Note)  $C_L$  includes the capacitance of the probe and others.

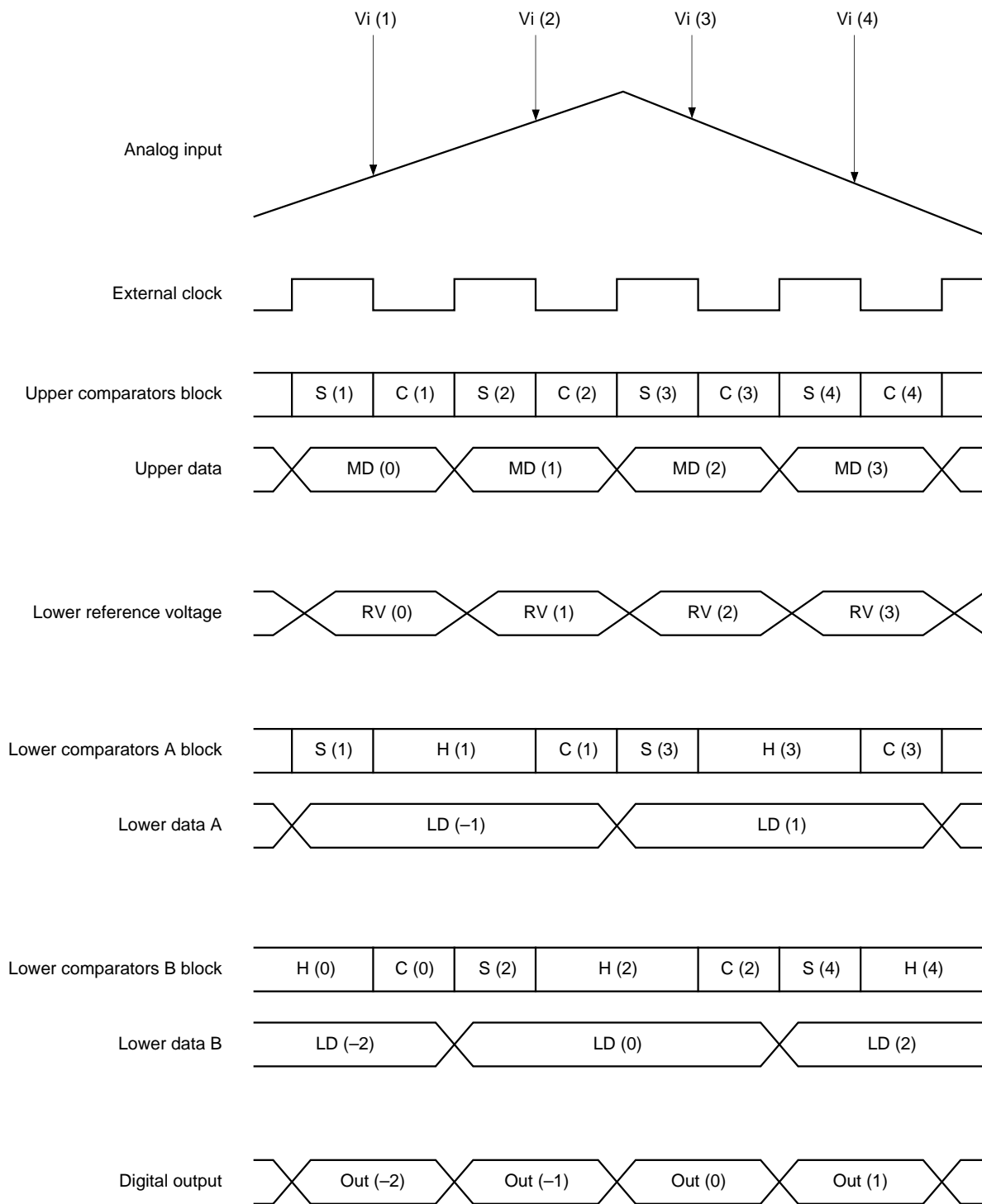
Maximum operational speed } measurement circuit  
 Differential gain error }  
 Differential phase error }



**Digital output current measurement circuit**



Timing Chart 3



Operation (See Block Diagram and Timing Chart)

1. The CXD1175AM/AP is a 2-step parallel system A/D converter featuring a 4-bit upper comparators group and 2 lower comparators groups of 4-bit each. The reference voltage that is equal to the voltage between  $VRT - VRB/16$  is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data.  $VRTS$  and  $VRBS$  pins serve for the self generation of  $VRT$  (Reference voltage top) and  $VRB$  (Reference voltage bottom).

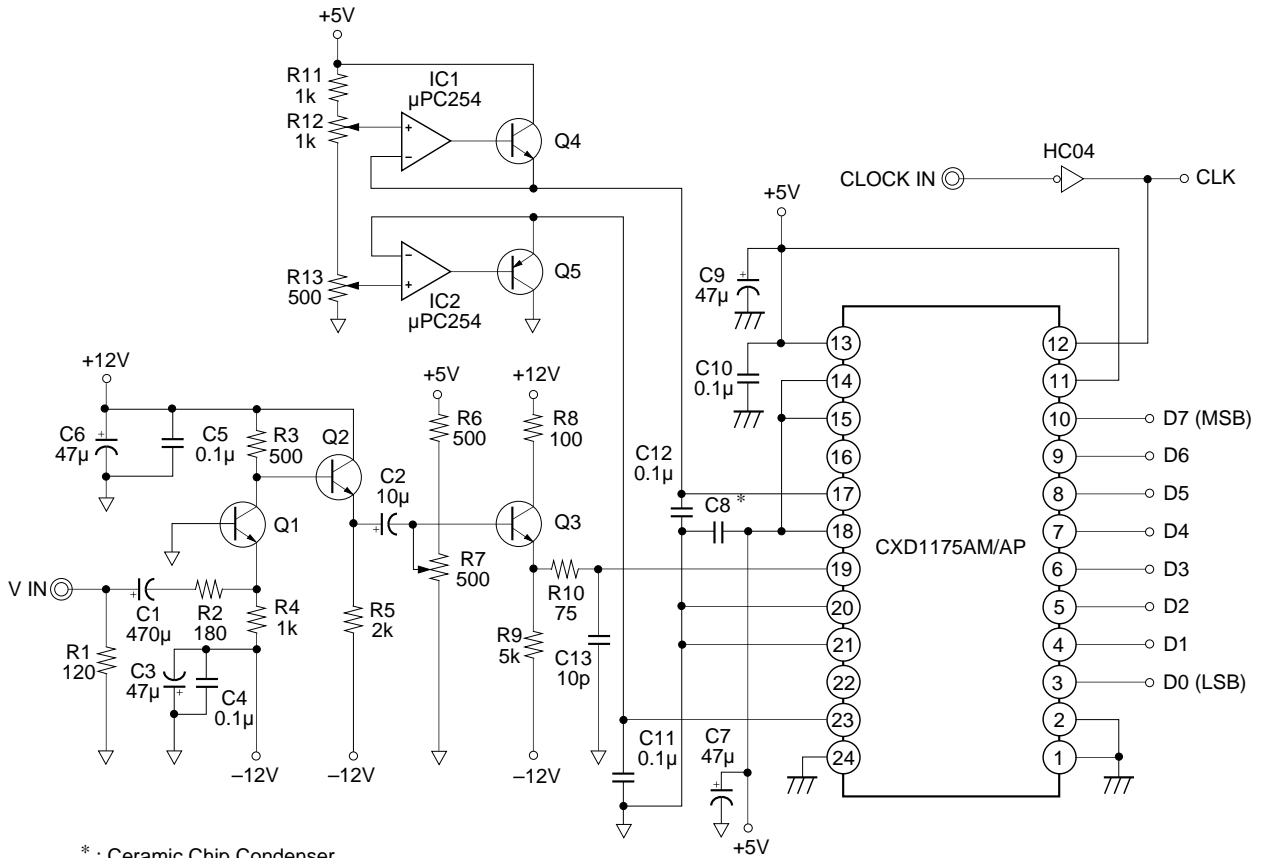


2. This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.
3. The operation of respective parts is as indicated in the chart. For instance input voltage  $V_i$  (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.  
The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

### Operation Notes

1.  $V_{DD}$ ,  $V_{SS}$   
To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog  $V_{DD}$  pins, use a ceramic capacitor of about  $0.1\mu\text{F}$  set as close as possible to the pin to bypass to the respective GND's.
2. Analog input  
Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about  $100\Omega$  in series between the amplifier output and A/D input.
3. Clock input  
The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.
4. Reference input  
Voltage between  $V_{RT}$  to  $V_{RB}$  is compatible with the dynamic range of the analog input. Bypassing  $V_{RT}$  and  $V_{RB}$  pins to GND, by means of a capacitor about  $0.1\mu\text{F}$ , stable characteristics are obtained. By shorting  $V_{RT}$  and  $V_{RTS}$ ,  $V_{RB}$  and  $V_{RBS}$ , the self-bias function that generates  $V_{RT} = 2.6\text{V}$  and  $V_{RB} = 0.6\text{V}$ , is activated.
5. Timing  
Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.
6.  $\overline{\text{OE}}$  pin  
By connecting  $\overline{\text{OE}}$  to GND output mode is obtained. By connecting to  $V_{DD}$  high impedance is obtained.
7. About latch up  
It is necessary that  $\text{AV}_{DD}$  and  $\text{DV}_{DD}$  pins be the common source of power supply.  
This is to avoid latch up due to the voltage difference between  $\text{AV}_{DD}$  and  $\text{DV}_{DD}$  pins when power is ON.

Application Circuit



\* : Ceramic Chip Condenser  
0.1 $\mu$ F

▽ : Analog GND

⏏ : Digital GND

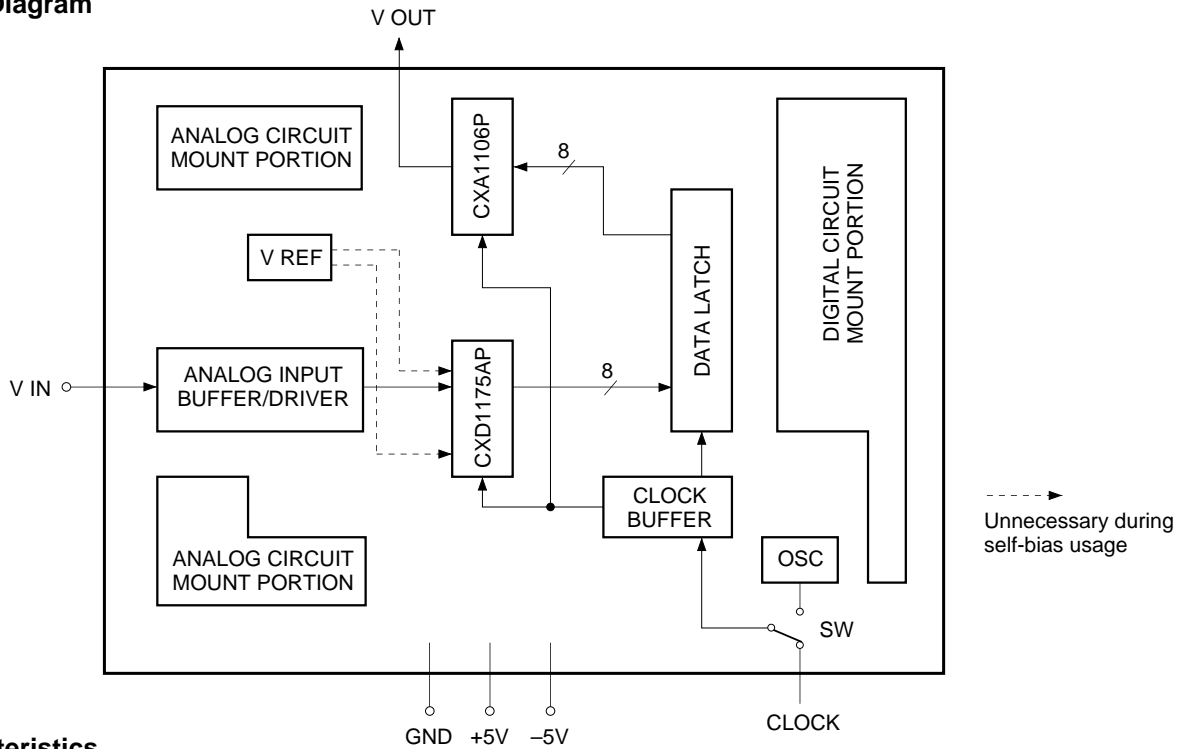
Note) It is necessary that AV<sub>DD</sub> and DV<sub>DD</sub> pins the common source of power supply.  
The gain of analog input signal can be variable by adjustment of value of R3.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**8-bit 20MSPS ADC and DAC Evaluation Board**

The CXD1175AP/CXA1106P PCB is evaluation PCB for the 8-bit high speed and low power consumption CMOS A/D converter CXD1175AP and the 8-bit high speed bipolar D/A converter CXD1106P. This PCB features a high speed and low power consumption CMOS A/D converter, analog input buffer, clock buffer, latch and high speed bipolar D/A converter designed to fully enhance the performance of A/D and D/A converters.

**Block Diagram**



**Characteristics**

- Resolution 8bit
- Maximum conversion rate 20MHz
- Digital input level TTL level
- Supply voltage  $\pm 5.0V$

**Supply voltage**

Item	Min.	Typ.	Max.	Unit
+5V			150	mA
-5V			20	

**Analog input**

**AC input voltage**

Item	Min.	Typ.	Max.	Unit
Gain ( $V_{IN} = 2V_{p-p}$ input)	0.5		2	
Offset voltage	0		5	V

**Clock input**

TTL compatible

- Pulse width  $T_{cw1}$  25ns (min.)
- $T_{cw0}$  25ns (min.)

**Analog Output (CXA1106)** (RL > 10kΩ)

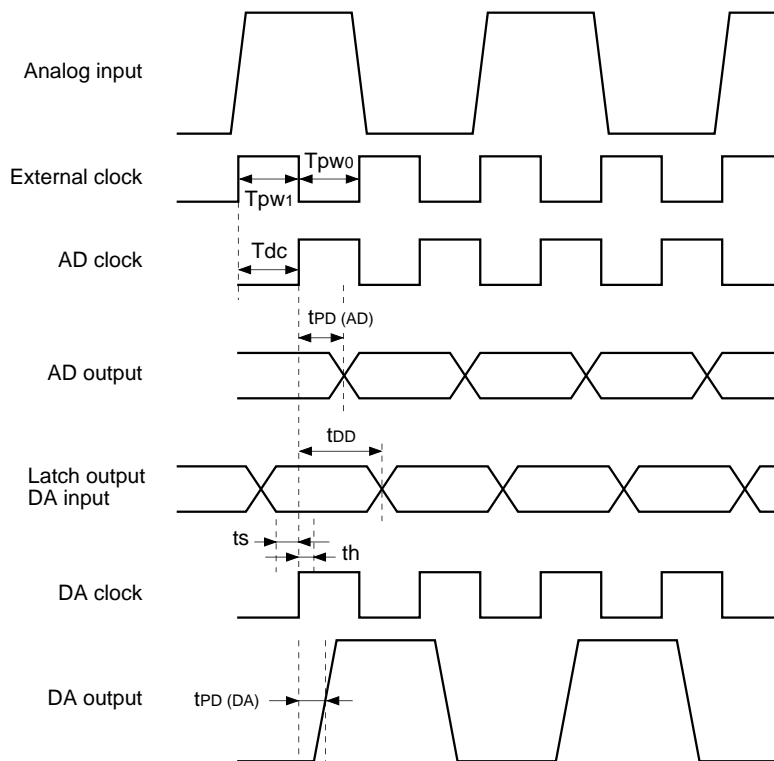
Item	Min.	Typ.	Max.	Unit
Analog output	0.9	1.0	1.1	V

**Output Format (CXD1175A)**

The table shows the output format of A/D converter.

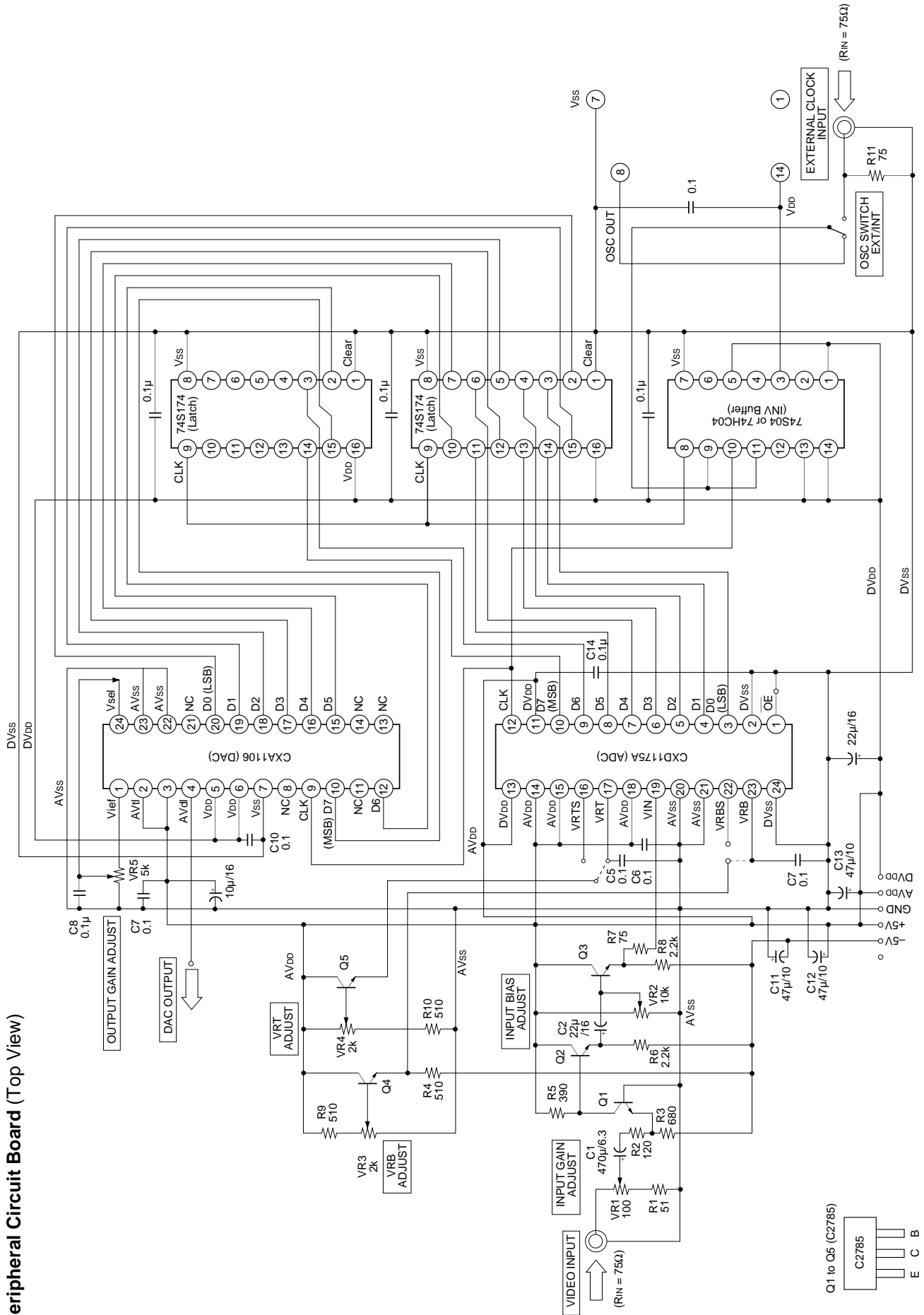
Input signal voltage	Step	Digital output code							
		MSB				LSB			
V <sub>RT</sub>	0	1	1	1	1	1	1	1	1
⋮	⋮	⋮							
⋮	127	1	0	0	0	0	0	0	0
⋮	128	0	1	1	1	1	1	1	1
⋮	⋮	⋮							
V <sub>RB</sub>	255	0	0	0	0	0	0	0	0

**Timing Chart**



Item	Symbol	Min.	Typ.	Max.	Unit
Clock high time	TPW1	25			ns
Clock low time	TPW0	25			ns
Clock delay	Tdc			24	ns
Data delay AD	t <sub>PD (AD)</sub>		18	30	ns
Data delay (latch)	t <sub>DD</sub>			17	ns
Set up time	t <sub>s</sub>	10			ns
Hold time	t <sub>h</sub>	2			ns
Data delay DA	t <sub>PD (DA)</sub>		11		ns

Peripheral Circuit Board (Top View)



## List of Parts

### resistor

R1	51Ω
R2	120Ω
R3	680Ω
R4	510Ω
R5	390Ω
R6	2.2kΩ
R7	75Ω
R8	2.2kΩ
R9	510Ω
R10	510Ω
R11	75Ω
VR1	100Ω
VR2	10kΩ
VR3	2kΩ
VR4	2kΩ
VR5	5kΩ

### capacitor

C1	470μF/6.3V (chemical)
C2	22μF/16V (chemical)
C3	0.01μF
C4	10μF/16V (tantalate)
C5	0.1μF
C6	0.1μF
C7	0.1μF
C8	0.1μF
C9	0.1μF
C10	0.1μF
C11	47μF/10V (chemical)
C12	47μF/10V (chemical)
C13	47μF/10V (chemical)
C14	0.1μF

### transistor

Q1	2SC2785
Q2	2SC2785
Q3	2SC2785
Q4	2SC2785
Q5	2SC2785

### IC

IC1	74S174
IC2	74S174
IC3	74S04

### oscillator

OSC

### others

connector	BNC071
SW	AT1D2M3

## Method of Adjustment

1. Vgain (VR1)  
Gain adjustment of the analog input.
2. Voffset (VR2)  
Offset adjustment of the analog input.
3. Vref (VR3, VR4)  
Adjustment of the A/D converter reference voltage.  
VRB is adjusted at VR3, and VRT at VR4. Reference voltage is given with self-bias for PCB shipment.
4. Analog output gain (VR5)  
Full-scale voltage of the D/A converter output is adjusted.

**Points on the PCB Pattern Layout**

1. Layout so that digital current does not flow to analog GND (part 1).  
(See Component Side on page 19 for part 1.)
2. Capacitor C6 (between AV<sub>SS</sub> and AV<sub>DD</sub>) and capacitor C14 (between DV<sub>SS</sub> and DV<sub>DD</sub>) are important factors to enhance the CXD1175A performance. Those capacitors should feature good high frequency characteristics over 0.1 $\mu$ F (ceramic capacitor). Layout as close to the IC as possible.
3. Analog GND (AV<sub>SS</sub>) and Digital GND (DV<sub>SS</sub>) have a common voltage and a supply source. The DV<sub>SS</sub> of A/D converter (part 2) location as close to the voltage source is possible will give even better results. That is, a layout where the A/D converter is close to the voltage source is recommended. (See Component Side on page 19 for part 2.)
4. AV<sub>DD</sub> (Pins 14, 15 and 18) and DV<sub>DD</sub> (Pins 11 and 13) are provided in the CXD1175A, and a common voltage source should be used for them as for part 3. (See the paragraph for Latch Up Prevention.) (See Soldering Side on page 19 for part 3.)
5. The A/D converter samples analog signals at the falling edge of clock. Accordingly, clocks fed to the A/D converter should not be affected by jitter.
6. In this PCB, to evaluate A/D and D/A converters independently, an independent layout has been adopted for the analog GND of A/D and D/A converters, from the voltage generation source. For the user's actual PCB even a common source poses no problems. For the CXA1106, as analog signals are output with the supply voltage as reference, take care not to let noise interfere with the analog V<sub>DD</sub> of D/A converter.

## Notes on Operation

### 1. Reference voltage

The self-bias function where  $V_{RT} = 2.6V$  and  $V_{RB} = 0.6V$  is available by shorting  $V_{RT}$  and  $V_{RTS}$ ,  $V_{RB}$  and  $V_{RBS}$  in the CXD1175A. At the PCB, either self-bias or external reference voltage can be selected according to the way the jumper wire is connected. For shipment, the reference voltage is provided by the self-bias. Also, when reference voltage is to be provided from the exterior, adjust the dynamic range ( $V_{RT} - V_{RB}$ ) to 1.8Vp-p or over.

### 2. Clock input

There are two modes for the PCB clock input.

- 1) Through an external signal generator (external clock)
- 2) Using a crystal oscillator (internal clock)

These two modes can be selected with a switch on the PCB.

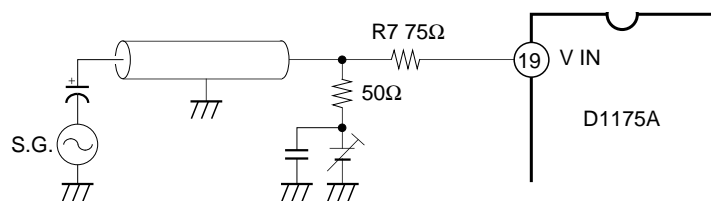
They are given from the external clock for shipment.

### 3. Peripheral through hole

There is a number of through holes at the analog input, output and LOGIC areas. Those are used when additional circuits are to be mounted on the PCB circuit.

4 The two latch ICs (74S174) on the circuit diagram are not absolutely necessary for the A/D and D/A converter evaluation. That is, when the A/D converter output data is directly input to D/A converter input, normal operation is maintained. However, as A/D converter output data is hardly ever subject to D/A conversion without the digital signal processing, the PCB has been fitted with the 74S174 to show a layout example for digital signal processing IC.

5. Analog input buffer & driver block is designed to handle conventional video band signals. Accordingly, for tests involving frequencies higher than that, methods shown in the figure below are recommended.



**High frequency input measurement circuit**

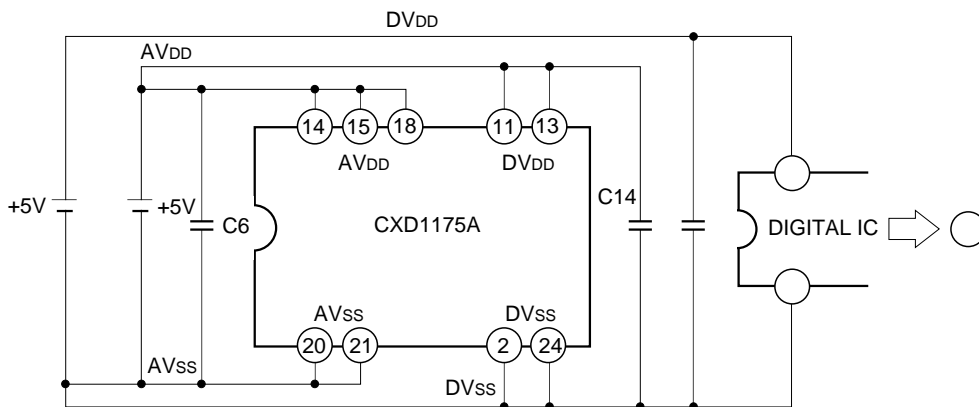


**Latch Up Prevention**

The CXD1175A is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV<sub>DD</sub> (Pins 14, 15 and 18) and DV<sub>DD</sub> (Pins 11 and 13), when power supply is ON.

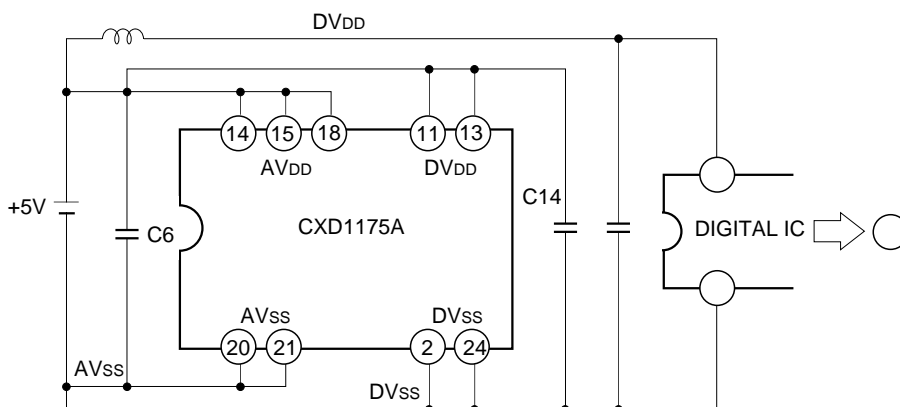
**1. Correct usage**

**a. When analog and digital supplies are from different sources**

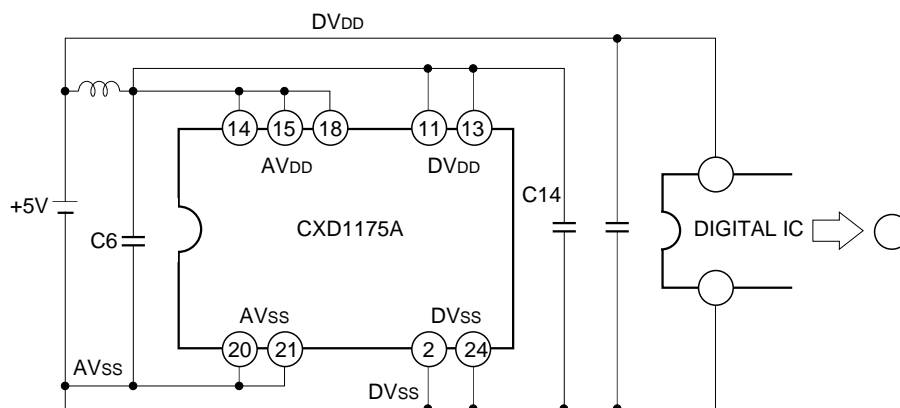


**b. When analog and digital supplies are from a common source**

(i)

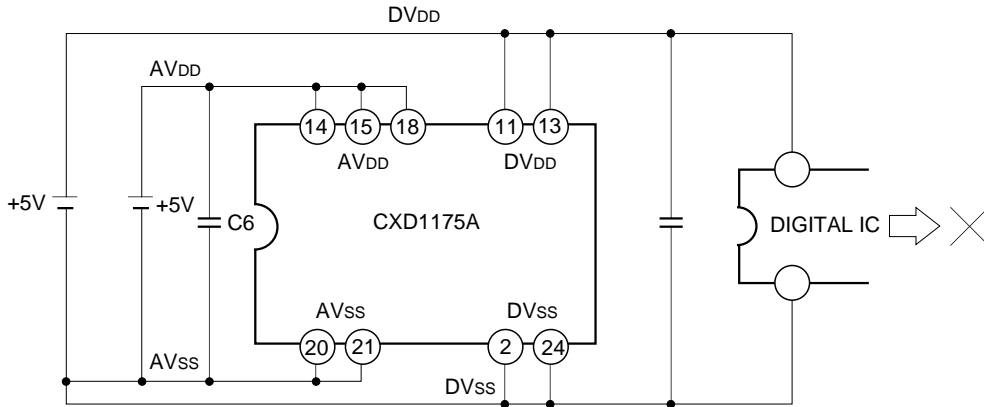


(ii)



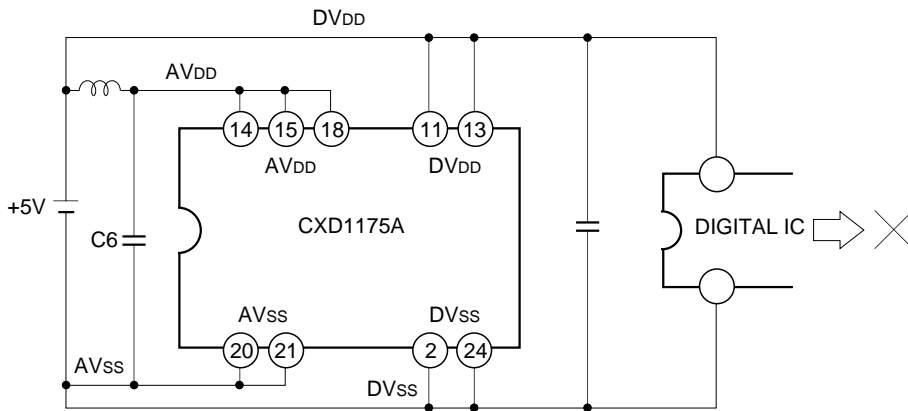
2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources

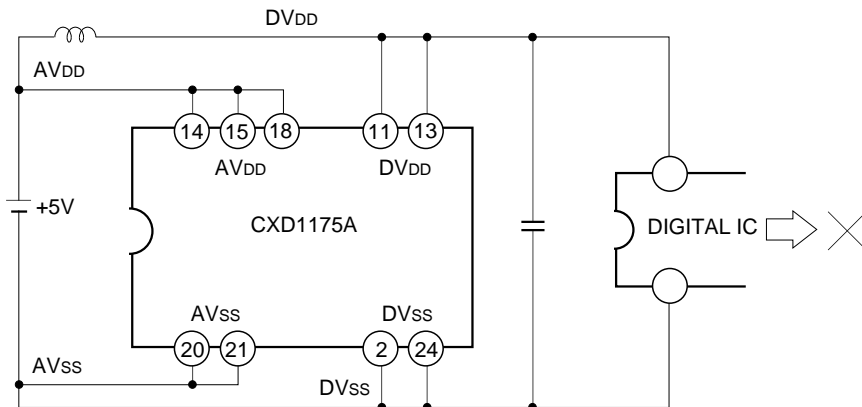


b. When analog and digital supplies are from common source

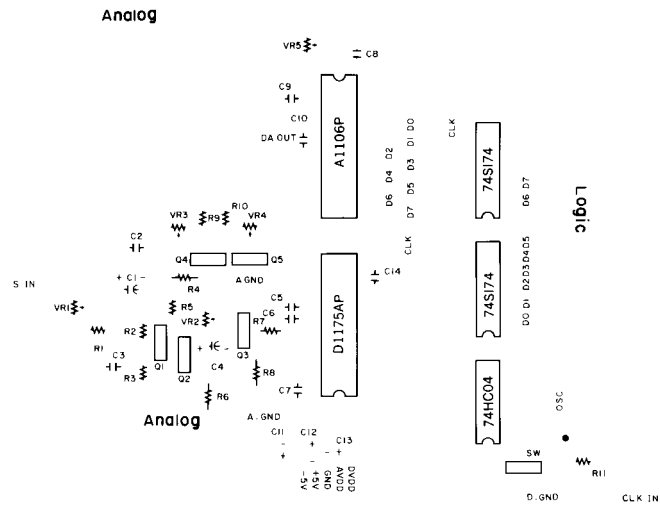
(i)



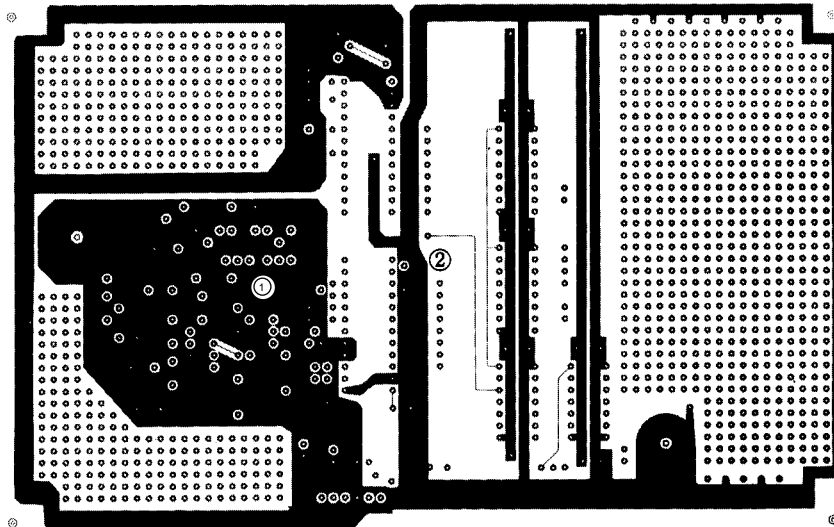
(ii)



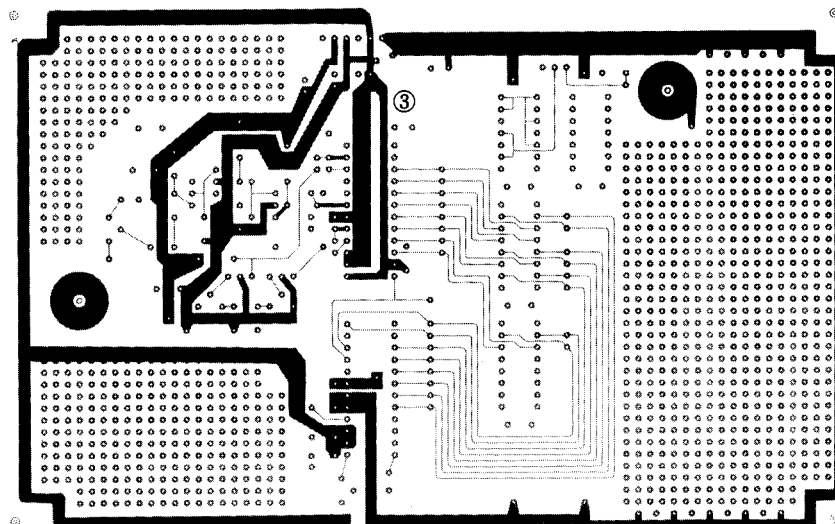
Silk Side



Component side



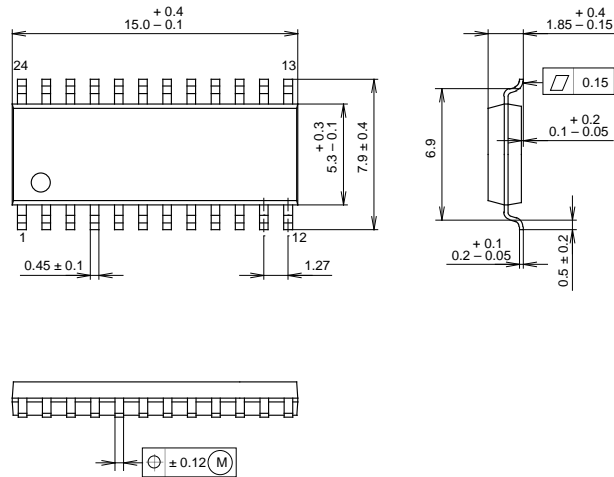
Soldering side



Package Outline Unit: mm

CXD1175AM

24PIN SOP (PLASTIC)



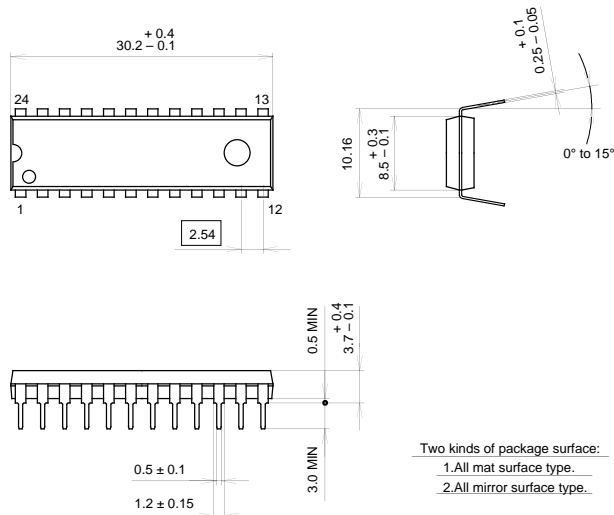
SONY CODE	SOP-24P-L01
EIAJ CODE	+SOP024-P-0300-A
JEDEC CODE	

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY / 42ALLOY
PACKAGE WEIGHT	0.3g

CXD1175AP

24PIN DIP(PLASTIC)



Two kinds of package surface:  
 1. All mat surface type.  
 2. All mirror surface type.

SONY CODE	DIP-24P-01
EIAJ CODE	DIP024-P-0400
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	2.0g