SONY

CXD1177Q

8-bit 40MSPS YC 2-channel D/A Converter

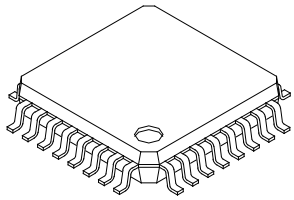
Description

The CXD1177Q is an 8-bit high-speed D/A converter for video band use. It has an input/output equivalent to 2 channels of Y and C. It is suitable for use of digital TV, graphic display, and others.

Features

- Resolution 8-bit
- Maximum conversion speed 40MSPS
- YC 2-channel input/output
- Differential linearity error ±0.3LSB
- Low power consumption 160mW
  (200Ω load at 2Vp-p output)
- Single 5V power supply
- Low glitch noise

32 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

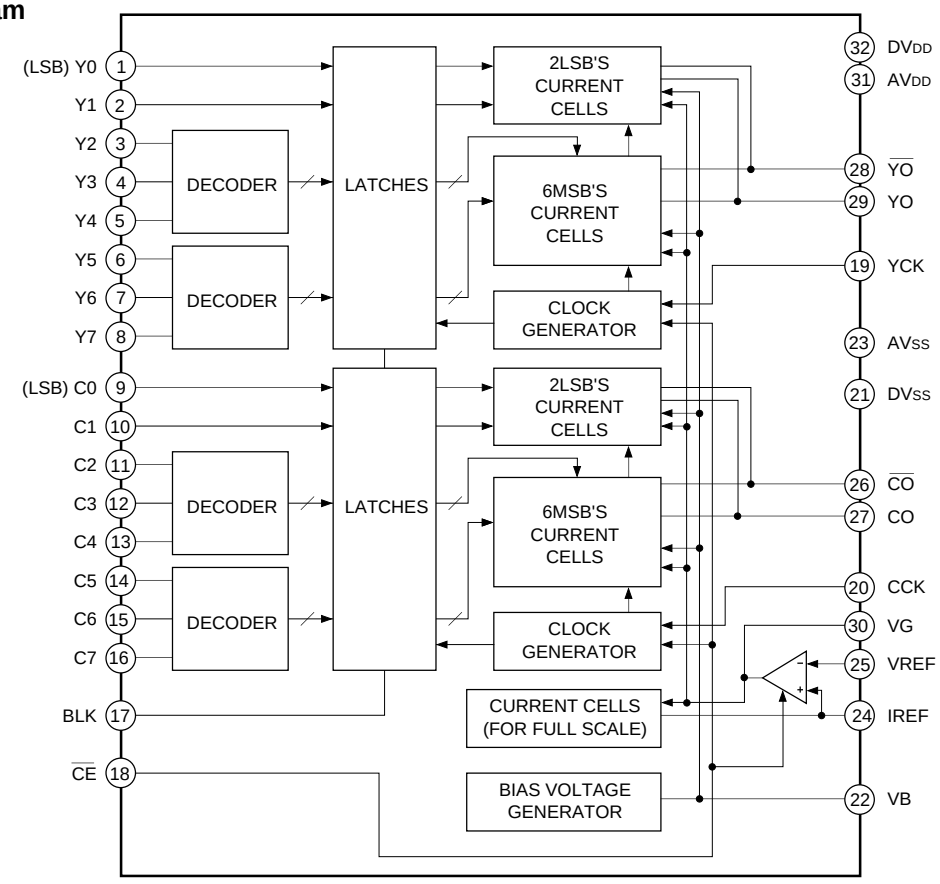
Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}	4.75 to 5.25	V
• Reference input voltage	V_{REF}	2.0	V
• Clock pulse width	Tpw_1	12.5 (Min.)	ns
	Tpw_0	12.5 (Min.)	ns
• Operating temperature	Topr	–20 to +75	°C

Absolute Maximum Ratings (Ta = 25°C)

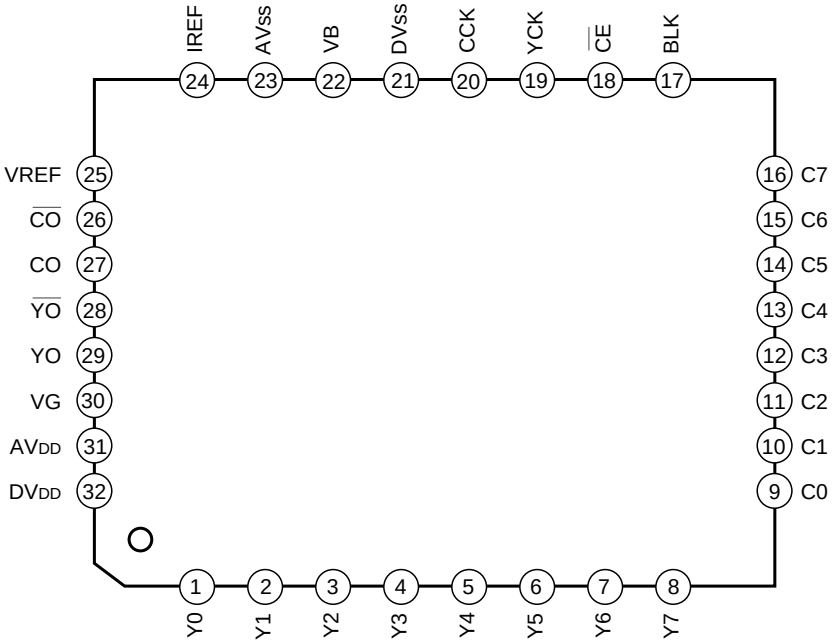
• Supply voltage	V_{DD}	7	V
• Input voltage	V_{IN}	V_{DD} to V_{SS}	V
• Output current (Every each channel)	I_{OUT}	0 to 15	mA
• Storage temperature	Tstg	–55 to +150	°C

Block Diagram

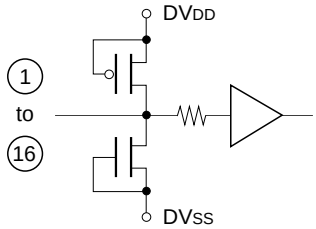
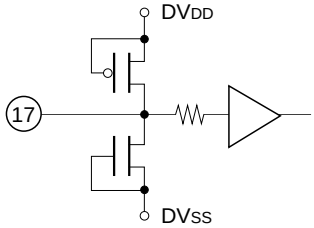
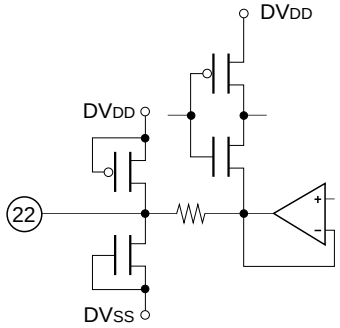


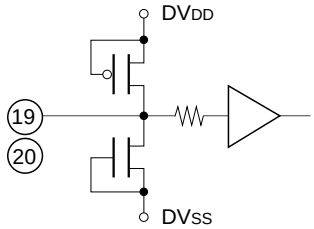
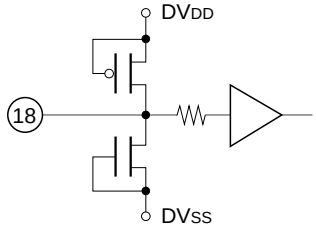
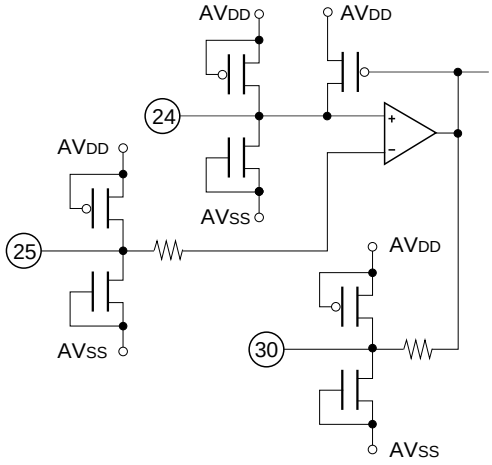
E90602C6X-PS

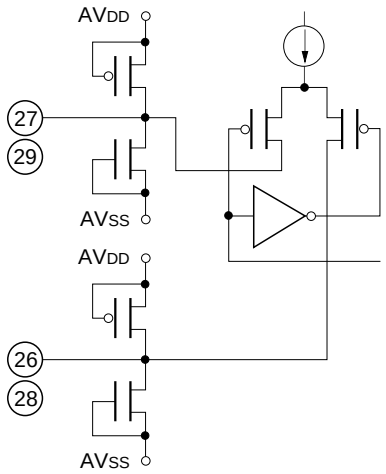
Pin Configuration



Pin Description and I/O Pins Equivalent Circuit

Pin No.	Symbol	Equivalent circuit	Description
1 to 8	Y0 to Y7		Digital input
9 to 16	C0 to C7		
17	BLK		Blanking pin. No signal at “H” (Output 0V). Output condition at “L”.
22	VB		Connect a capacitor of about 0.1µF.

Pin No.	Symbol	Equivalent circuit	Description
19	YCK		Clock pin. Moreover all input pins are TTL-CMOS compatible.
20	CCK		
21	DVSS		Digital GND
23	AVSS		Analog GND
18	$\overline{CE}$		Chip enable pin. No signal (Output 0V) at “H” and minimizes power consumption.
24	IREF		Connect a resistance 16 times “16R” that of output resistance value “R”.
25	VREF		Set full scale output value.
30	VG		Connect a capacitor of about 0.1µF.
31	AVDD		Analog VDD

Pin No.	Symbol	Equivalent circuit	Description
27	CO		Current output pin. Voltage output can be obtained by connecting a resistance.
29	YO		
26	$\overline{CO}$		Inverted current output pin. Normally dropped to analog GND.
28	$\overline{YO}$		
32	DV_{DD}		Digital V_{DD}

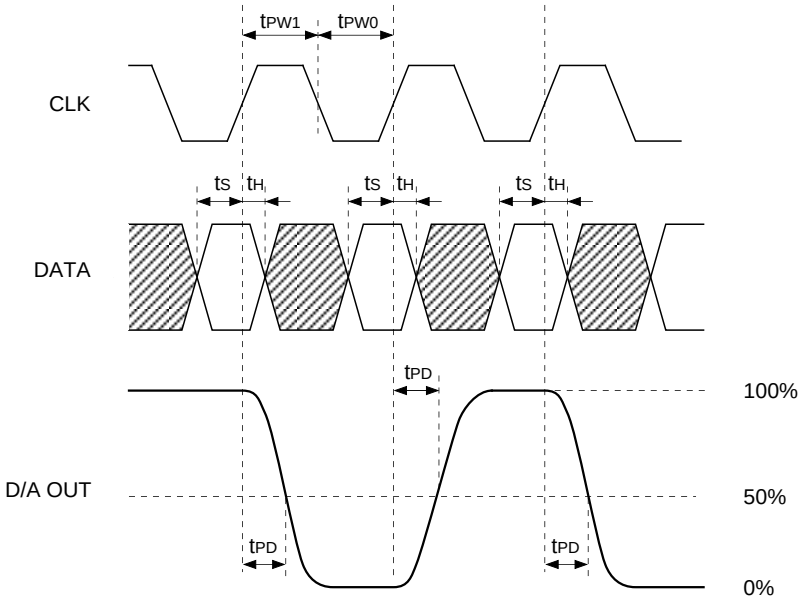
Electrical Characteristics (f_{CLK} = 40MHz, V_{DD} = 5V, R_{OUT} = 200Ω, V_{REF} = 2.0V, Ta = 25°C)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution		n			8		bit
Maximum conversion speed		f_{MAX}				40	MSPS
Minimum conversion speed		f_{MIN}		0.5			MHz
Linearity error		E_L		–2.5		2.5	LSB
Differential linearity error		E_D		–0.3		0.3	LSB
Full-scale output voltage		V_{FS}		1.9	2.0	2.2	V
Full-scale output ratio *1		F_{SR}		0	1.5	3	%
Full-scale output current		I_{FS}			10	15	mA
Offset output voltage		V_{OS}				1	mV
Power supply current		I_{DD}	14.3MHz at COLOR BAR DATA input			32	mA
Digital input current	High level	I_{IH}				5	µA
	Low level	I_{IL}		–5			µA
Setup time		t_S		5			ns
Hold time		t_H		10			ns
Propagation delay time		t_{PD}			10		ns
Glitch energy		GE	Rout = 75Ω		30		pV-s
Crosstalk		CT	1MHz Sin WAVE output		57		dB

*1 Full-scale output ratio = $\left| \frac{\text{Full-scale voltage of channel}}{\text{Average of the full-scale voltage of the channels}} - 1 \right| \times 100\ (\%)$

Description of Operation

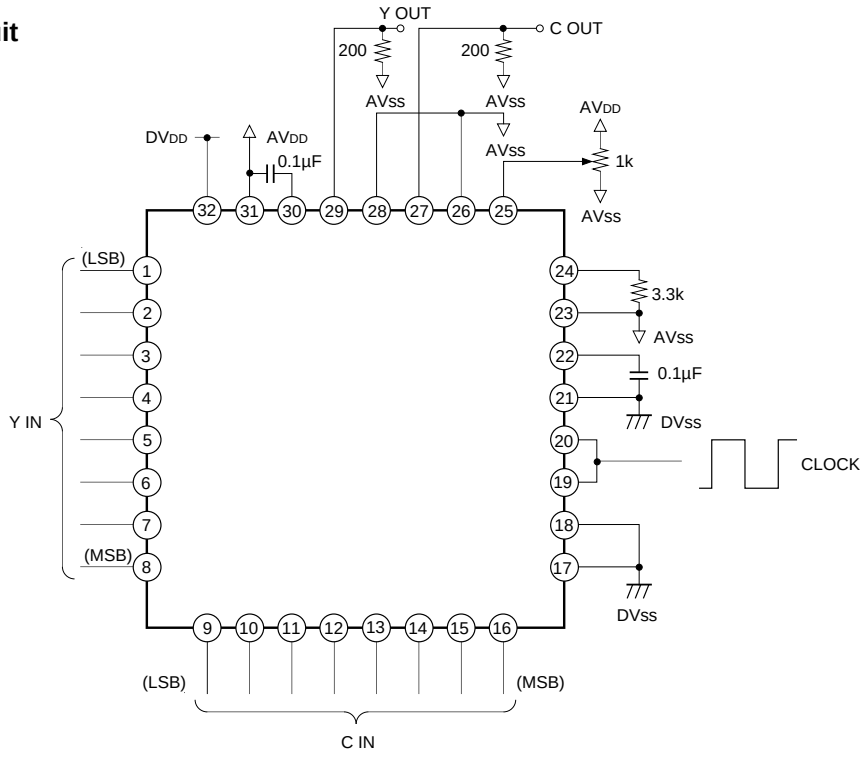
Timing Chart



I/O Chart (When full scale output voltage at 2.00V)

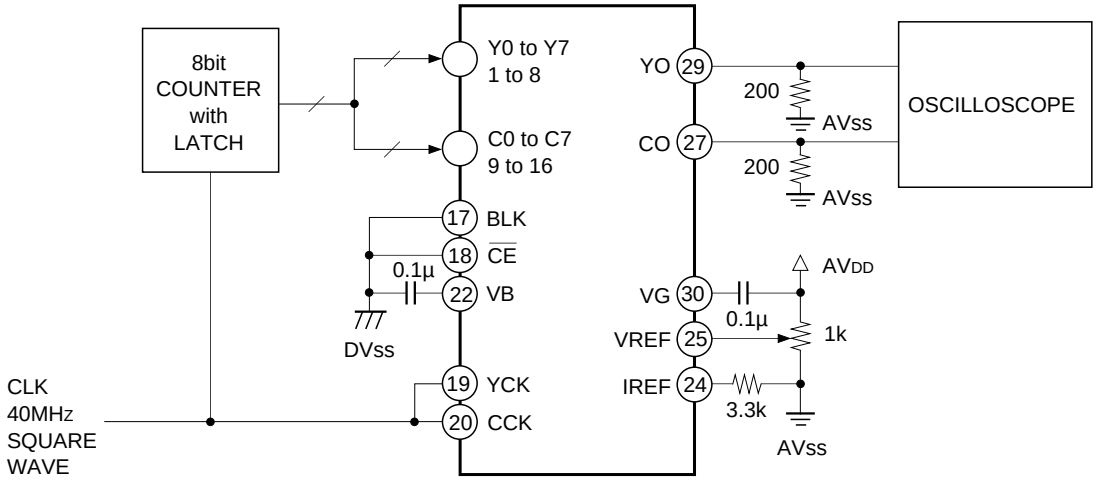
Input code	Output voltage
MSB LSB 1 1 1 1 1 1 1 1	2.0V
:	
1 0 0 0 0 0 0 0	1.0V
:	
0 0 0 0 0 0 0 0	0V

Application Circuit

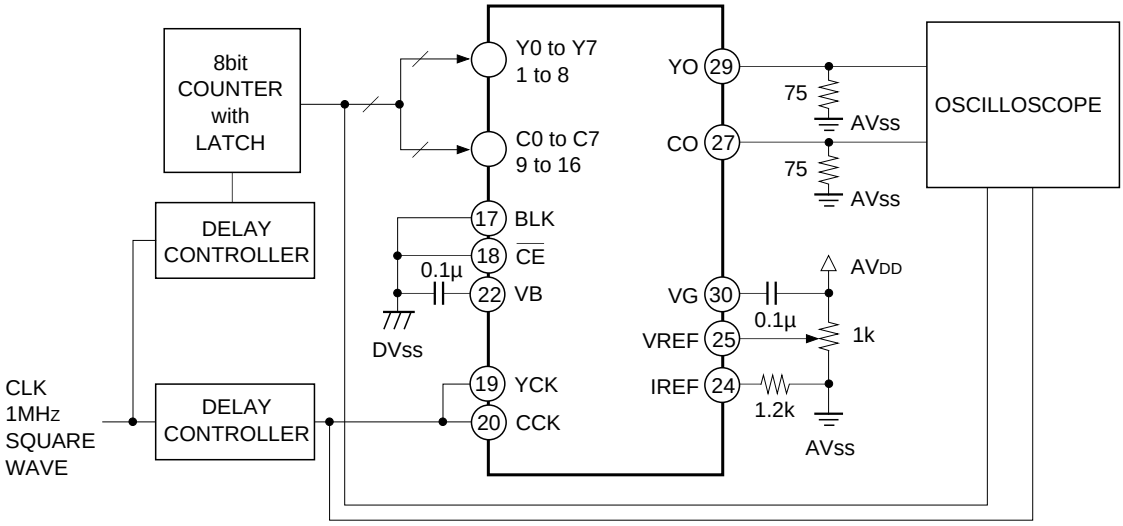


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

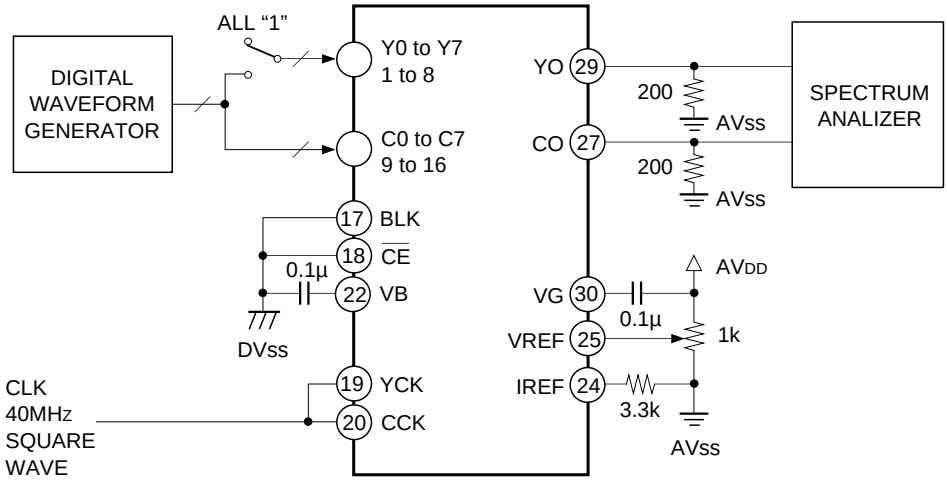
Maximum Conversion Velocity Test Circuit



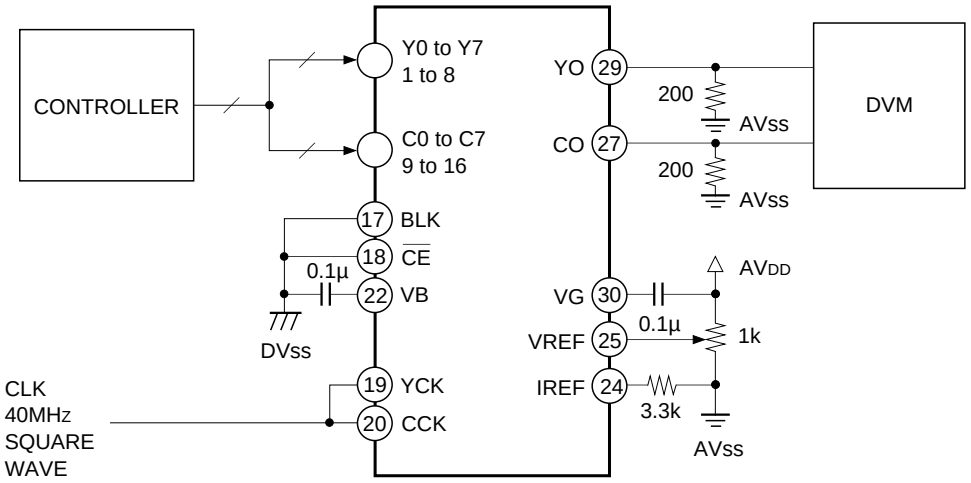
Setup Hold Time
Glitch Energy **Test Circuit**



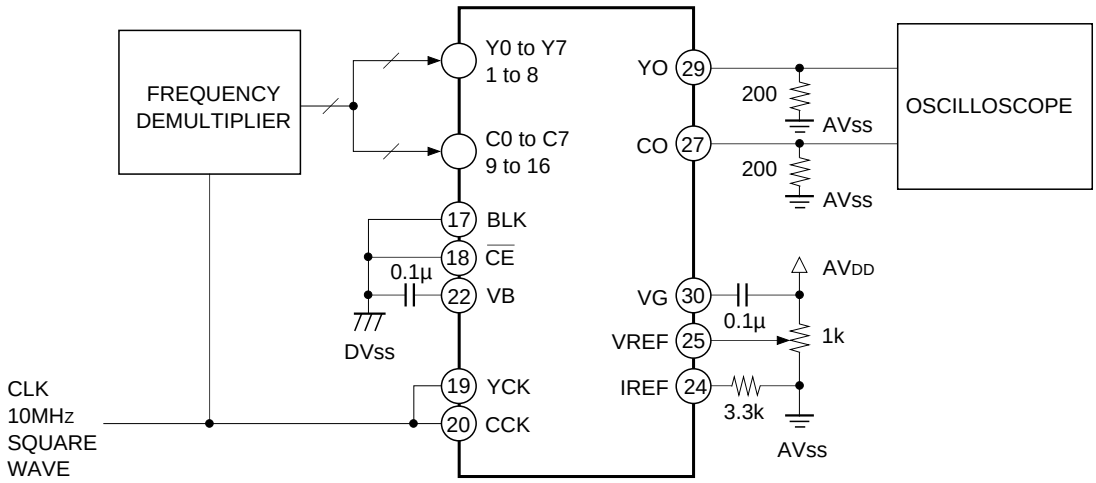
Crosstalk Test Circuit



DC Characteristics Test Circuit



Propagation Delay Time Test Circuit



Notes on Operation

- How to select the output resistance

  The CXD1177Q is a D/A converter of the current output type. To obtain the output voltage connect the resistance to IO pin (Y0, C0). For specifications we have;

  Output full scale voltage V_{FS} = less than 2.0 [V]

  Output full scale current I_{FS} = less than 15 [mA]

  Calculate the output resistance value from the relation of $V_{FS} = I_{FS} \times R$. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS} = V_{REF} \times 16R/R'$. R is the resistance connected to IO while R' is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

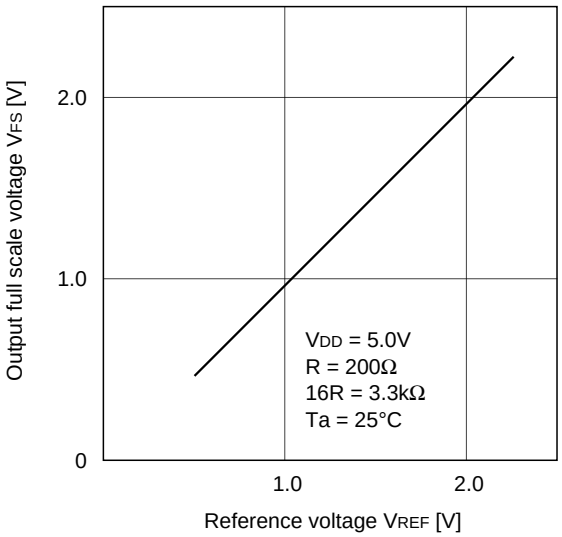
  To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the setup time (t_S) and hold time (t_H) as stipulated in the Electrical Characteristics.

- V_{DD}, V_{SS}

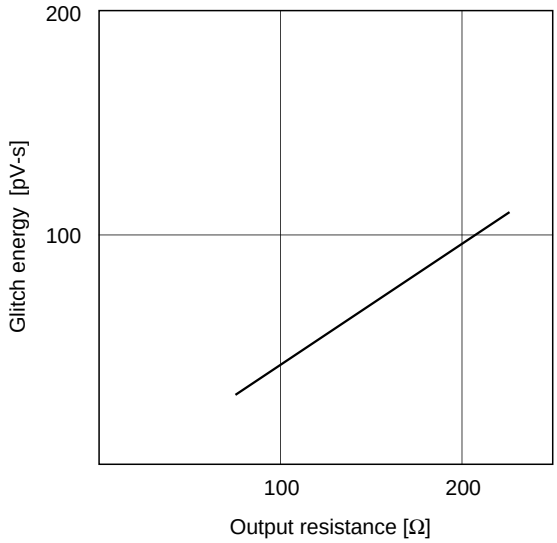
  To reduce noise effects separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of about 0.1µF, as close as possible to the pin.

Example of Representative Characteristics

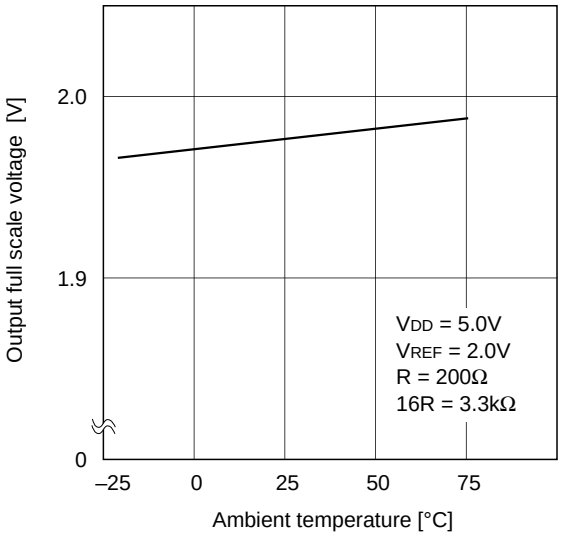
Output full scale voltage vs. Reference voltage



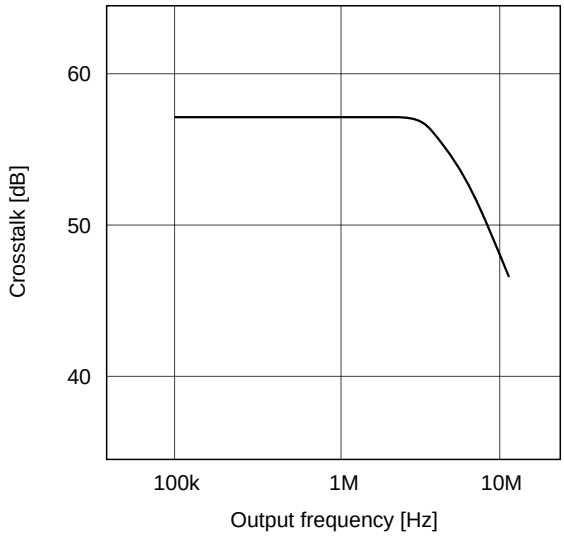
Giitch energy vs. Output resistance



Output full scale voltage vs. Ambient temperature

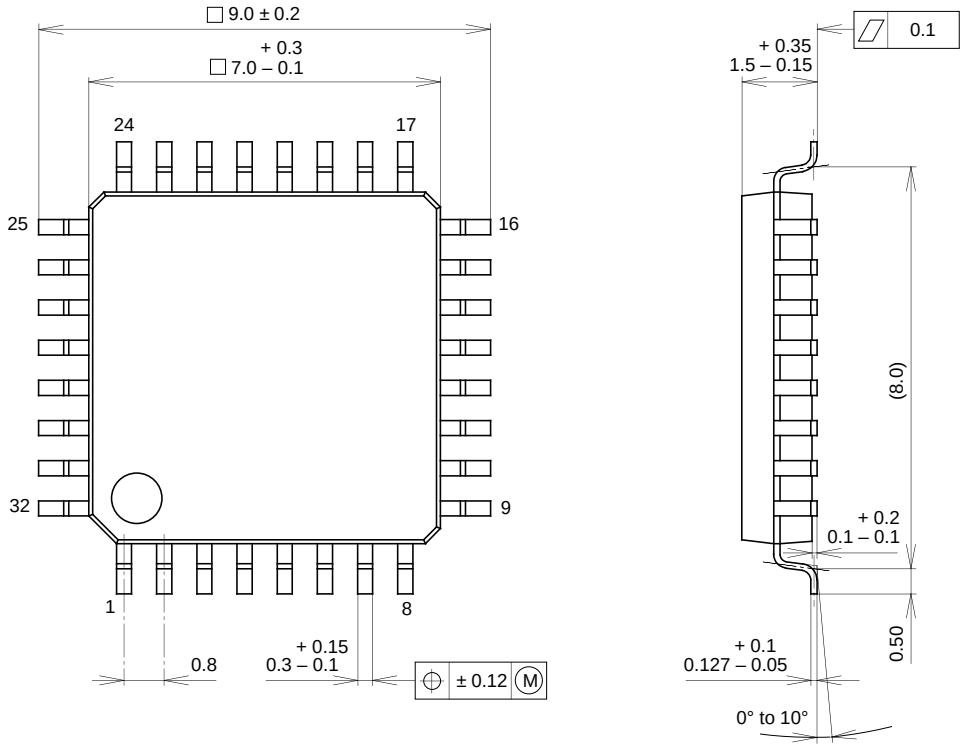


Crosstalk vs. Output frequency



Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	∗QFP032-P-0707-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g