IEEE1394 3-port 200Mbps Cable Transceiver/Arbiter

Description

The CXD1944R is a PHY chip which supports 100/200Mbps speeds and performs cable interface and bus arbitration. It conforms to the high performance serial bus IEEE1394-1995 standard. The structure is 0.4µm CMOS and it operates on a single 3.3V power supply.

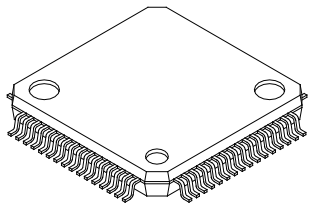
Features

- Conforms to IEEE1394-1995
- Single 3.3V power supply
- Supports 100/200Mbps speeds
- Automatic power down for unused ports
- Power down mode to conserve energy
- Supports short reset operation
- Supports ping for optimization of a Gap_count

Absolute Maximum Ratings

• Supply voltage	V_{DD}	–0.5 to +4.6	V
• Input voltage	V_I	V_{SS} –0.5 to V_{DD} +0.5	V
• Output voltage	V_O	V_{SS} –0.5 to V_{DD} +0.5	V
• Operating temperature	Ta	–20 to +70	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	1000	mW

64 pin LQFP (plastic)



Operating Conditions

• Supply voltage	V_{DD}	3.0 to 4.5	V
• Operating temperature	Ta	–20 to +75	°C

Package

64-pin plastic LQFP (VQFP)

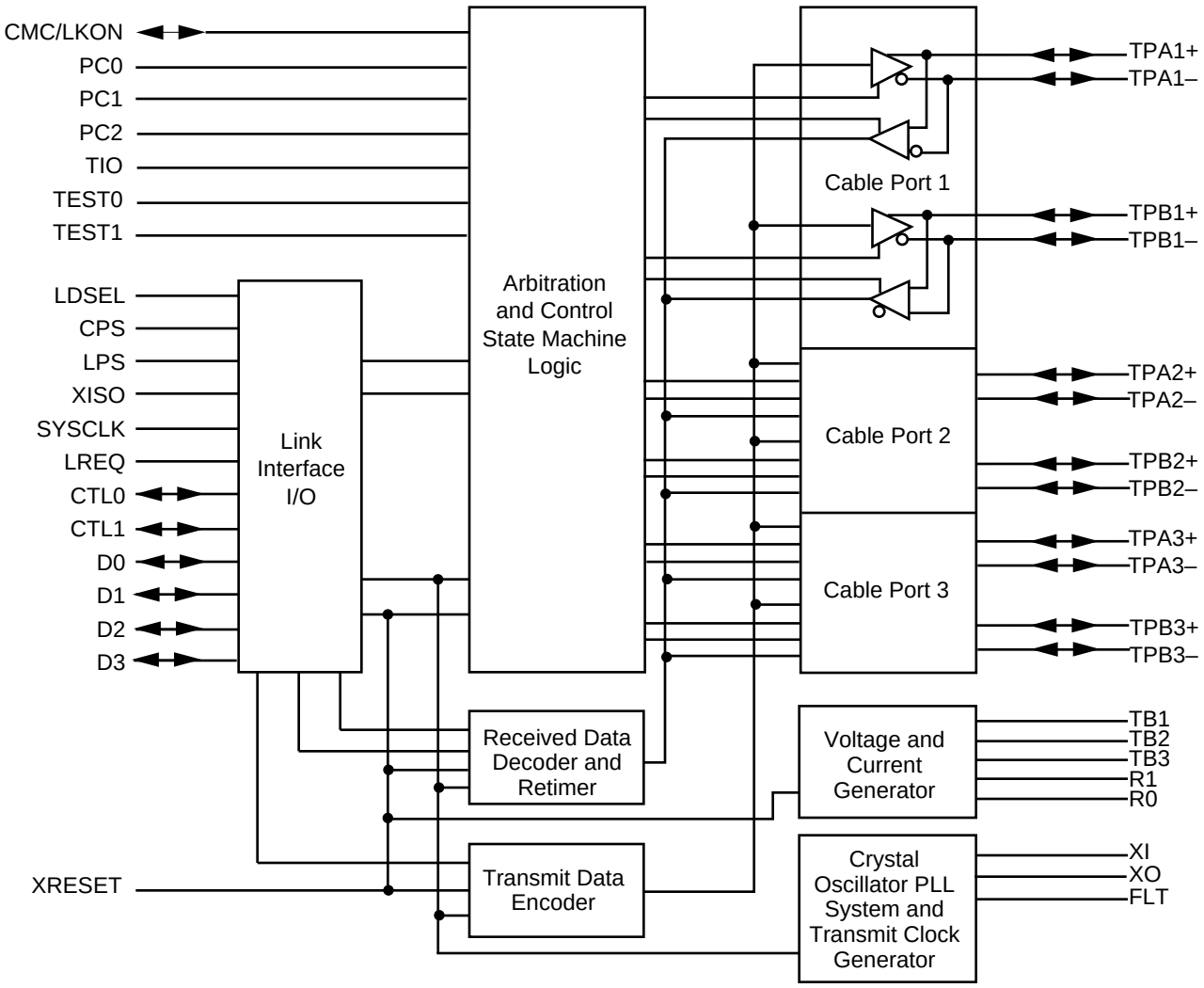
Applications

When used with a LINK chip (e.g. CXD1940R), allows configuration of a high-speed digital serial interface.

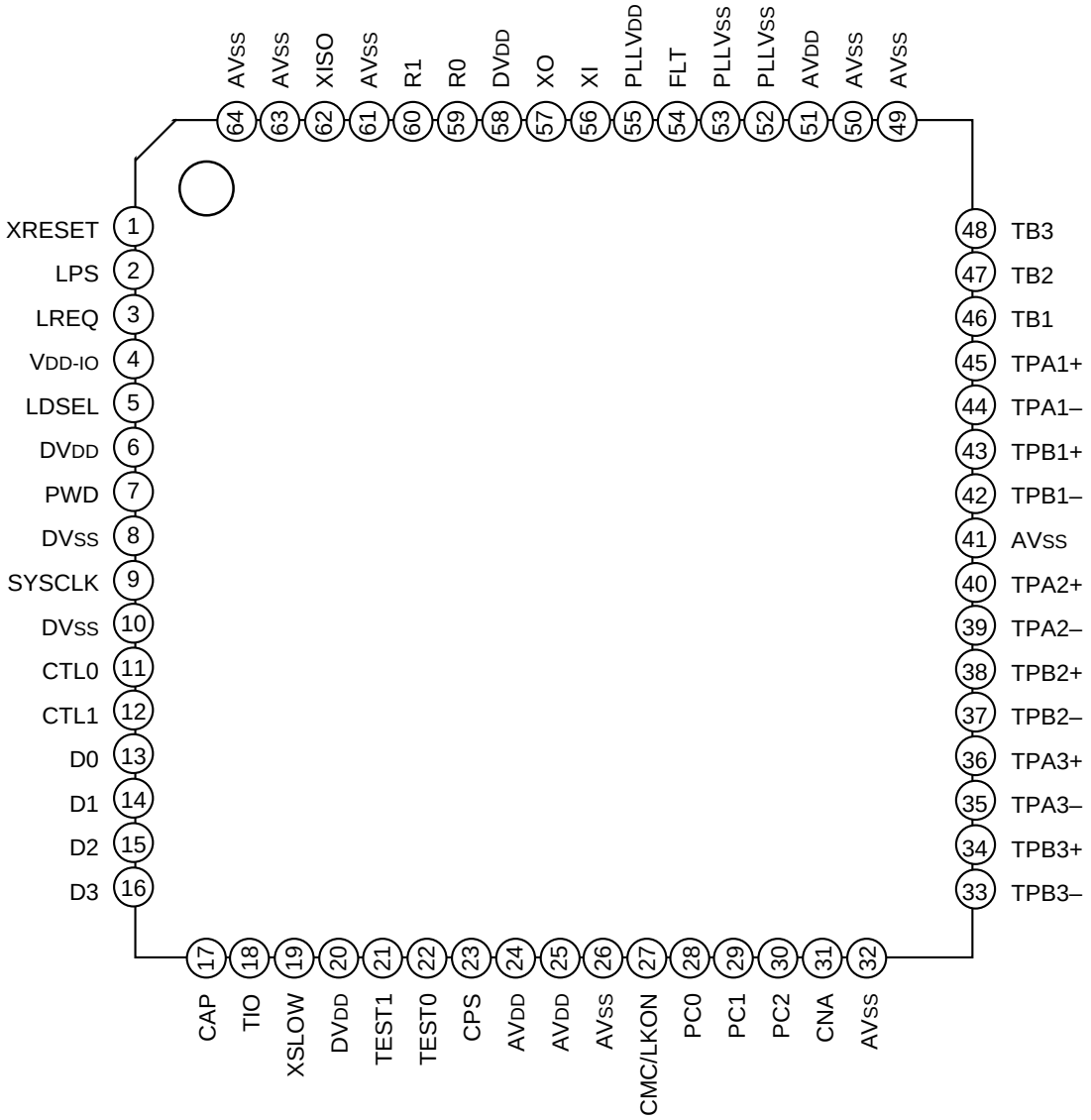
Structure

0.4µm CMOS monolithic IC

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	XRESET	I	Reset input. Asserts at LOW. A power-on reset signal can be generated by adding a 0.1µF capacitor.
2	LPS	I	LINK power supply status. LINK power supply is connected.
3	LREQ	I	LINK request input.
4	V_{DD-IO}	Supply	IO power supply.
5	LDSEL	I	LINK delay select.
6	DV_{DD}	Supply	Digital circuit power supply.
7	PWD	I	Power down input.
8	DV_{SS}	Supply	Digital circuit ground.
9	SYSCLK	OUT	System clock output; 49.152MHz clock to LINK.
10	DV_{DD}	Supply	Digital circuit power supply.
11	CTL0	I/O	I/O of bidirectional control signals for LINK.
12	CTL1	I/O	I/O of bidirectional control signals for LINK.
13	D0	I/O	I/O of bidirectional data signals for LINK.
14	D1	I/O	I/O of bidirectional data signals for LINK.
15	D2	I/O	I/O of bidirectional data signals for LINK.
16	D3	I/O	I/O of bidirectional data signals for LINK.
17	CAP	I	Connect to ground via 0.1µF capacitor when a 5V LINK is used.
18	TIO	I/O	Connect to V_{SS} or V_{DD}. If then connected to V_{DD}, short reset mode is selected.
19	XSLOW	I	When XSLOW = LOW, a device acts as a 100M PHY. Normally connected to V_{DD}.
20	DVDD	Supply	Digital power supply.
21	TEST1	I	Test mode control. Normally connected to ground.
22	TEST0	I	Test mode control. Normally connected to ground.
23	CPS	I(A)	Cable power status input. Normally connected to cable power.
24	AV_{DD}	Supply	Analog circuit power supply.
25	AV_{DD}	Supply	Analog circuit power supply.
26	AV_{SS}	Supply	Analog circuit power ground.
27	CMC/LKON	I/O	Configuration Manager Capable input, LINK ON clock (6MHz) output. When LPS = LOW and a LinkOn packet is received, the 6MHz clock signal continues to be output. Connect to V_{DD} or V_{SS} with a 10KΩ resister. The configuration management function is indicated when connected to V_{DD}.
28	PC0	I	Power Class input (LSB).
29	PC1	I	Power Class input.
30	PC2	I	Power Class input (MSB).
31	CNA	O	Cable Not Active output. This output is debounced.
32	AV_{SS}	Supply	Analog circuit power ground.
33	TPB3–	I/O(A)	Port3, Cable Pair B–.
34	TPB3+	I/O(A)	Port3, Cable Pair B+.

Pin No.	Symbol	I/O	Description
35	TPA3–	I/O(A)	Port3, Cable Pair A–.
36	TPA3+	I/O(A)	Port3, Cable Pair A+.
37	TPB2–	I/O(A)	Port2, Cable Pair B–.
38	TPB2+	I/O(A)	Port2, Cable Pair B+.
39	TPA2–	I/O(A)	Port2, Cable Pair A–.
40	TPA2+	I/O(A)	Port2, Cable Pair A+.
41	AV_{SS}	Supply	Analog circuit power ground.
42	TPB1–	I/O(A)	Port1, Cable Pair B–.
43	TPB1+	I/O(A)	Port1, Cable Pair B+.
44	TPA1–	I/O(A)	Port1, Cable Pair A–.
45	TPA1+	I/O(A)	Port1, Cable Pair A+.
46	TB1	O(A)	Tp bias output. Output 1.85V (typ.), and Hi-Z during chip reset and power down. Corresponds to one port.
47	TB2	O(A)	Tp bias output. Output 1.85V (typ.), and Hi-Z during chip reset and power down. Corresponds to one port.
48	TB3	O(A)	Tp bias output. Output 1.85V (typ.), and Hi-Z during chip reset and power down. Corresponds to one port.
49	AV_{SS}	Supply	Analog circuit power ground.
50	AV_{SS}	Supply	Analog circuit power ground.
51	AV_{DD}	Supply	Analog circuit power supply.
52	$PLLV_{SS}$	Supply	PLL circuit power ground.
53	$PLLV_{SS}$	Supply	PLL circuit power ground.
54	FLT	O(A)	PLL loop filter.
55	$PLLV_{DD}$	Supply	PLL circuit power supply.
56	XI	I(A)	Crystal oscillator (24.576MHz±100ppm). The optimum values for the 100kΩ resistor and 20pF capacitor.
57	XO	O(A)	Crystal oscillator (24.576MHz±100ppm). The optimum values for the 100kΩ resistor and 20pF capacitor.
58	DV_{DD}	Supply	Digital circuit power supply.
59	R0	I(A)	Reference resistance pin. Connect R1 and R0 with 6.8kΩ±5% resistor. R0 may be connected to ground.
60	R1	O(A)	Reference resistance pin. Connect R1 and R0 with 6.8kΩ±5% resistor. R0 may be connected to ground.
61	AV_{SS}	Supply	Analog circuit power ground.
62	XISO	I	XISO = LOW indicates isolation barrier which enables digital differentiator.
63	AV_{SS}	Supply	Analog circuit power ground.
64	AV_{SS}	Supply	Analog circuit power ground.

Recommended Operating Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		3.0	3.3	3.6	V
High level input	V_{IH}	XRESET, LPS, LREQ, CTL0	0.8V_{DD}			V
Low level input	V_{IL}	XRESET, LPS, LREQ, CTL0			0.2V_{DD}	V
Differential input	V_{ID-100}	Cable input, 100Mbps	142		260	mV
Differential input	V_{ID-200}	Cable input, 200Mbps	132		260	mV
Differential input	V_{ID-ARB}	Cable input, Arbitration	171		260	mV
Common input	V_{CM-100}	TpB Cable input, 100Mbps or speed signaling off	1.165		2.515	V
Common input	V_{CM-200}	TpB Cable input, 200Mbps, speed signaling on	0.935		2.515	V
Differential input jitter	JTT100	Cable input, 100Mbps			±1.08	ns
Differential input skew	SKW100	Between TpA and TpB, 100Mbps			±0.80	ns
Differential input jitter	JTT200	Cable input, 200Mbps			±0.50	ns
Differential input skew	SKW200	Between TpA and TpB, 200Mbps			±0.55	ns
Output current (1)	I_{OH}/I_{OL}	SYSCLK, CTL0, CTL1, D0, D1, D2, D3, CMC/LKON	±12			mA
	I_O	TB1, TB2, TB3	–1.3		9.68	mA

Electrical Characteristics

Driver

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Differential output voltage	V_{OD}	55Ω load	172		265	mV
Common mode current (2)	I_{CM}	Driver on, speed signaling off	–0.40		0.22	mA
Speed signal common mode current (2)	I_{CM-SP}	200Mbps speed signaling on	–4.84		–2.53	mA
Common mode voltage when driver is off (2)	V_{OFF}	Driver off, speed signaling off			20	mV

NOTES:
1. For output current, all source current is positive (+) and sink current is negative (–).
2. Common mode current is the average value of the currents output from TPB+ and TPB–. The same applies to TPA+ and TPA–.

Receiver

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Common mode input current	I_{IC}	Driver off	–20		20	µA
Differential input impedance	Z_{ID}	Driver off	15			kΩ
					24	pF
Differential input threshold	V_{TH}		–30		30	mV
Arbitration differential input threshold	V_{TH+}	“1” input	168			mV
	V_{THZ}	“Z” input	–89		89	mV
	$V_{TH–}$	“0” input			–168	mV
Speed signal detection threshold	V_{TH-SP}	TB-TPA common mode potential	49		131	mV
Cable bias detection threshold	V_{TH-CB}	TPB common mode input	0.6		1.0	V

Device

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{DD}	V_{DD} = 3.6V			100	mA
		V_{DD} = 3.6V when cable is not connected			50	mA
	I_{DD-PD}	V_{DD} = 3.6V, Power down mode			10	mA
I/O supply voltage	V_{DD-IO}	When a 5V LINK is used	4.5		5.5	V
		When a 3V LINK is used	3.0		3.6	V
High level output	V_{OH}	SYSCLK, CTL0, CTL1, D0, D1, D2, D3, CMC/LKON, I_{OH} = 12mA, V_{DD} = min.	V_{DD}–0.4			V
Low level output	V_{OL}	SYSCLK, CTL0, CTL1, D0, D1, D2, D3, CMC/LKON, I_{OL} = 12mA, V_{DD} = max.			0.4	V
High level input threshold	V_{TH+}	XRESET, LPS, LREQ, PWD, CTL0, CTL1, D0, D1, D2, D3	0.6V_{DD}			V
Low level input threshold	V_{TH-}	XRESET, LPS, LREQ, PWD, CTL0, CTL1, D0, D1, D2, D3			0.4V_{DD}	V
Input leak current	I_{IL}	XRESET, LPS, LREQ, PWD, CTL0, CTL1, D0, D1, D2, D3, V_I = 0V or V_{DD}			±10	µA
Output leak current when output is off	I_{OZ}	SYSCLK, CTL0, CTL1, D0, D1, D2, D3, CMC/LKON			±40	µA
Power up reset time	T_{PWR}		2			ms
CPS input threshold	V_{TH-CPS}	200kΩ resistor	5.5		7.5	V
CPS input current	I_{CPS}	CPS pin at 1.85V	20		30	µA
TB output voltage	V_O		1.665		2.015	V
R1 pin output voltage	V_{R1}	I_{R1} = 100µA	0.635		0.761	V

I/O Pin Capacitance

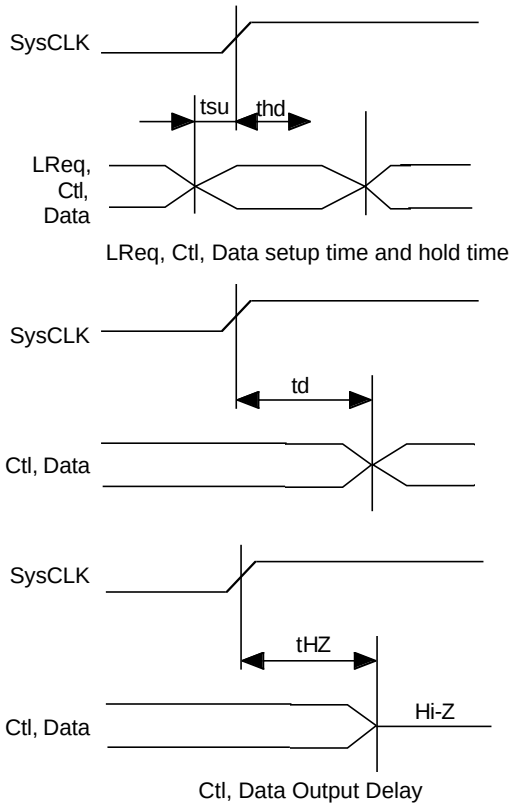
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin capacitance	CIN	XRESET, LPS, LREQ, PC0, PC1, PC2, CPS			11	pF
Output pin capacitance	COUT	SYSCLK			11	pF
Input/Output capacitance	CI/O	CTL0, CTL1, D0, D1, D2, D3, CMC/LKON			11	pF

AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output jitter	JTT	TPA, TPB			±0.25	ns
Output skew	SKW	Between TPA and TPB			±0.15	ns
Output rise time	Tr	TPA, TPB, 10 to 90%, RL = 55Ω, CL = 10pF			2.2	ns
Output fall time	Tf	TPA, TPB, 90 to 10%, RL = 55Ω, CL = 10pF			2.2	ns
Setup time	Tsu	LREQ, CTL0, CTL1, D0, D1, D2, D3 relative to SYSCLK, LDSEL = HIGH	5			ns
		LREQ, CTL0, CTL1, D0, D1, D2, D3 relative to SYSCLK, LDSEL = LOW	0			ns
Hold time	Thd	LREQ, CTL0, CTL1, D0, D1, D2, D3 relative to SYSCLK, LDSEL = HIGH	2			ns
		LREQ, CTL0, CTL1, D0, D1, D2, D3 relative to SYSCLK, LDSEL = LOW	7			ns
Output delay time	Td	CTL0, CTL1, D0, D1, D2, D3 from SYSCLK	2.5		11	ns
Output disable time(1)	Thz	CTL0, CTL1, D0, D1, D2, D3 from SYSCLK	1.5		0.0	ns

NOTE:
1. When control of CTL0, CTL1 and D0 to 3 passes from PHY to LINK. Refer to the section on Transmit.

Switching Waveforms



LReq, Ctl, Data setup time and hold time

Ctl, Data Output Delay

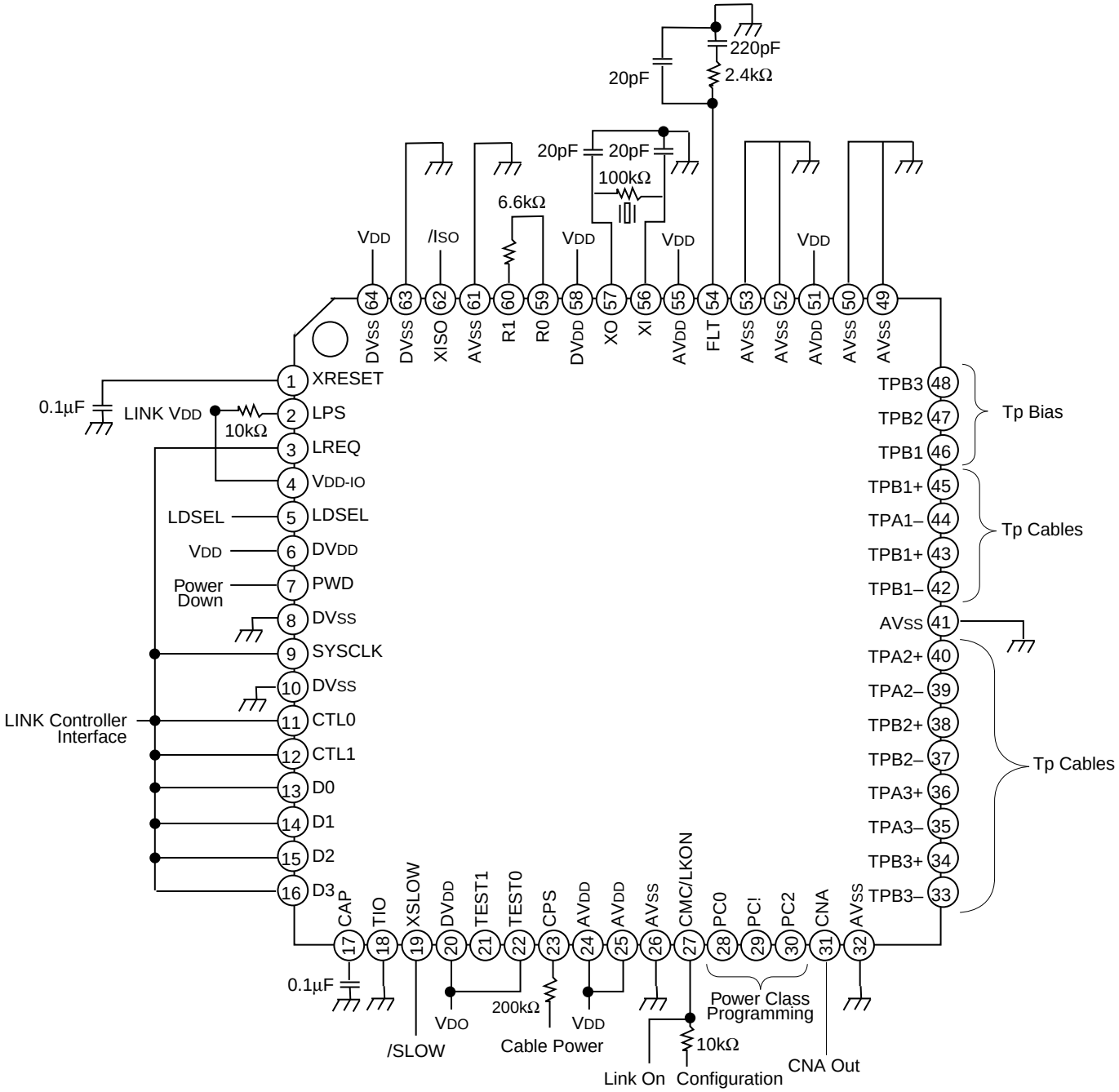
Internal Register

MSB LSB

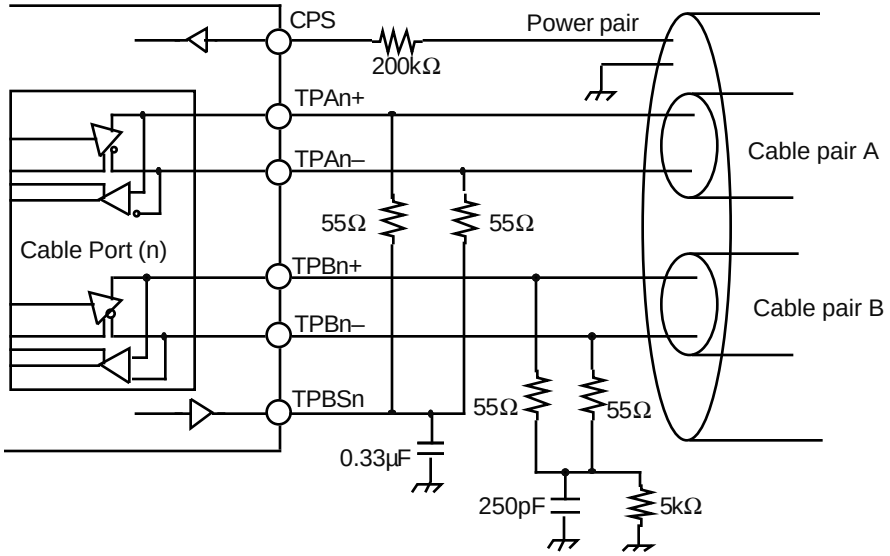
Address	0	1	2	3	4	5	6	7
0000	Physical-ID						R	CPS
0001	RHB	IBR	GC					
0010	SPD = 01		0	NP = 00011				
0011	ASTAT1		BSTAT1		Ch1	Con1	0	P1Fast
0100	ASTAT2		BSTAT2		Ch2	Con2	0	P2Fast
0101	ASTAT3		BSTAT3		Ch3	Con3	0	P3Fast
0110	LoopInt	CPStatInt	CPStat	IDidIt	Illegal LReq	0	0	0
0111	Reserved				Chip Rev			
1000	Reserved							
1001	0	0	0	0	0	Slow Pin	Slow Bit	ArbRstReq
1010	Ping Timer [15 : 8]							
1011	Ping Timer [7 : 0]							

Name	Size	Type	Description
Physical-ID	6	R	The address number of this node. Determined during Self-ID.
R	1	R	Indicates that this node is the root.
CPS	1	R	Cable power status.
RHB	1	R/W	Root Holding Bit. Attempts to become the root during next bus reset if set to “1”.
IBR	1	R/W	Initiate Bus Reset. Generates bus reset when possible after being set to “1”. Cleared after bus reset.
GC	6	R/W	Gap Count. Used to optimize gap time according to bus scale.
SPD	2	R	Indicates this node’s highest speed; 200Mbps when “01”, 100Mbps when “00”.
NP	4	R	Indicates the number of ports on this node.
ASTAT(n)	2	R	Indicates port n TPA status. 11 = Z, 01 = 1, 10 = 0, 00 = invalid
BSTAT(n)	2	R	Indicates port n TPB status. 11 = Z, 01 = 1, 10 = 0, 00 = invalid
Ch(n)	1	R	When the value is “1”, indicates that port n is the Child. “0” indicates Parent.
Con(n)	1	R	When the value is “1”, indicates that the active cable is connected to port n.
P(n) Fast	1	R	When the value is “1”, indicates that port n supports 200Mbps.
LoopInt	1	R/W	This is set to “1” when Tree-ID is not completed in time, which means that the bus may be forming a loop.
CPStatInt	1	R/W	Indicates a drop in cable power line voltage.
CPStat	1	R	Same as CPS.
IDidIt	1	R	Indicates that this node generates the last bus reset. More than one node may set this value.
IllegalReq	1	R	Indicates an illegal LReq is detected.
ChipRev	4	R	Indicates the chip revision number.
Slow Pin	1	R	Indicates XSLOW pin is set to LOW.
Slow Bit	1	R/W	When set to “1”, the node acts as a 100Mbps PHY. Default is “0”.
ArbRstReq	1	R/W	Initiate the arbitrated bus reset. Cleared after bus reset.
Ping Timer	16	R	50MHz Ping Timer count. A count starts when a configuration packet is transmitted and stops when the first packet is received. The value may not be cleared until the next configuration packet is sent.

External Components and Pin Connection



Twisted Pair Cable Connection



Description of Operation

The CXD1994R is used with LINK controllers such as the CXD1940R to configure a high speed serial bus. It has three ports which support speeds of 100M/200Mbps.

There are four basic operations which may occur in the interface: request, status, transmit, and receive. All bit request are initiated by the PHY. The LINK uses the request operation to read or write an internal PHY register or to ask the PHY to initiate a transmit action. The PHY initiates a receive action whenever a packet is received from the serial bus.

The serial bus is always 2 bits wide, independent of speed.

The encoding of these pins is as follows:

CTL [0 : 1] When PHY is Driving

CTL [0: 1]	Name	Meaning
00	Idle	No activity.
01	Status	The PHY is sending status information to the LINK.
10	Receive	An incoming packet is being transferred from the PHY to the LINK.
11	Transmit	The LINK is granted the bus to send a packet.

CTL [0 : 1] When the LINK is Driving (upon a grant from PHY)

CTL [0: 1]	Name	Meaning
00	Idle	Transmission complete, release bus.
01	Hold	The LINK is holding the bus while preparing data or indicating it wishes to reacquire the bus without arbitration to send another packet.
10	Transmit	The LINK is sending a packet to the PHY.
11	Reserved	Unused.

LINK Request

To request the bus or access a PHY register, the LINK sends a short stream to the PHY on the LREQ pin. The information sent includes the type of request to which the packet is to be sent, or a read or write command. The transfer can be either 7 bits, 9 bits or 17 bits, depending on whether it is a bus request, a read access, or a write access, repectively. A stop bit of 0 is required after each request transfer before another transfer may begin.

Bus Request Format

Bit(s)	Name	Description
0	Start Bit	Indicates start of transfer. Always 1.
1 to 3	Request Type	Indicates which type of bus request is being performed. See the table below for the encoding of this field.
4 to 5	Request Speed	The speed at which the PHY will be sending the packet for this request. This field has the same encoding as the speed code from the first symbol of the receive packet. See the following table for the encoding of this field.
6	Stop Bit	Indicates end of transfer. Always 0.

If the transfer is a read request, it is 9 bits long and has the following format:

Read Request Format

Bit(s)	Name	Description
0	Start Bit	Indicates start of transfer. Always 1.
1 to 3	Request Type	Indicates that this is a register read. See the following table for the encoding of this field.
4 to 7	Address	The internal PHY register address to be read.
8	Stop Bit	Indicates end of transfer. Always 0.

If the transfer is a write request, it is 17 bits long and has the following format:

Write Request Format

Bit(s)	Name	Description
0	Start Bit	Indicates start of transfer. Always 1.
1 to 3	Request Type	Indicates that this is a register read. See the following table for the encoding of this field.
4 to 7	Address	The internal PHY register address to be written.
8 to 15	Data	The data to be written to the specified address.
16	Stop Bit	Indicates end of transfer. Always 0.

The request type field is encoded as follows:

Request Type Field

LREQ [1 : 3]	Name	Meaning
000	ImmReq	Take control of the bus immediately upon detecting idle; do not arbitrate. Used for acknowledge transfers.
001	IsoReq	Arbitrate for the bus; no gaps. Used for isochronous transfers.
010	PriReq	Arbitrate after a subaction gap; ignore fair protocol. Used for cycle start packet.
011	FairReq	Arbitrate after a subaction gap, following fair prototcol. Used for fair transfers.
100	RdReq	Return specified register contents through status transfer.
101	WrReg	Write to specified register.
110 to 111	Reserved	Ignored.

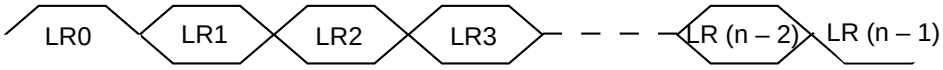
The request speed field is encoded as follows:

Request Speed Field

LREQ [4 : 5]	Data Rate
00	100Mbps
01	200Mbps
10	400Mbps
11	>400Mbps

NOTE:
The CXD1944R does not support 400Mbps and over.

LREQ Timing



FairReq and PrioReq:

To request the bus for fair or priority access, the LINK sends the request at least one clock after the interface becomes idle. The LINK interprets the receive state on the CTL pins as a lost request. If the LINK sees the receive state anytime during or after it sends the request transfer, it assumes the request is lost and reissues the request on the next idle. The PHY will ignore a fair or priority request if it asserts the receive state anytime during the request transfer. Note that the minimum length of a packet is two clock cycles in the case of 400Mbps acknowledge packet. The minimum request packet is 8 clock cycles. It is important that the LINK and PHY agree to interpret a lost request the same way.

The cycle master node uses a priority request (PriReq) to send the cycle start message. To request the bus to send isochronous data, the LINK can issue the request at any time after receiving the cycle start. The PHY will clear an isochronous request only when the bus has been won.

ImmReq:

To send an acknowledge, the LINK must issue an ImmReq request during the reception of the packet addressed to it. This is required because the delay from end of packet to acknowledge request adds directly to the minimum delay every PHY must wait after every packet to allow an acknowledge to occur. After the packet ends, the PHY immediately takes control of the bus and grants the bus to the LINK. If the header CRC of the packet turns out to be bad, the LINK releases the bus immediately. The LINK cannot use this grant to send another type of packet. To ensure this, the LINK must wait 160ns after the end of the received packet to allow the PHY to grant it the bus for the acknowledge, then release the bus and proceed with another request.

Though highly unlikely, it is conceivable that two different nodes can perceive (one correctly, one mistakenly) that an incoming packet is intended for them and both issue an acknowledge request before checking the CRC. Both nodes' PHYs would grab control of the bus immediately after the packet is complete. This condition will cause a temporary, localized collision of the data-on line states somewhere between two PHYs intending to acknowledge. All other PHYs on the bus would see the data-on state. This collision would appear as a "zz" line state, and would not be interpreted as a bus reset. The mistaken node would drops its request as soon as it has checked the CRC and spurious "zz" line states would go away. The only side effect of such a collision would be the loss of the intended acknowledge packet, which would be handled by the higher-layer protocol.

IsoReq:

To send an isochronous packet, the LINK is recommended to issue an IsoReq request during the reception or transmission (if root) of a cycle start packet or another isochronous packet. This is required to keep an isochronous gap short. Any IsoReq will be cleared when a packet is transmitted or a certain time (80ns) is passed in idle after the bus seized. (This timeout is not a part of the IEEE1394-1995 standard.) When the LINK issues an IsoReq before CRC check of a cycle start packet and the CRC is found wrong after the IsoReq, the LINK may release the bus without sending a packet when the bus is granted.

Read/Write Request:

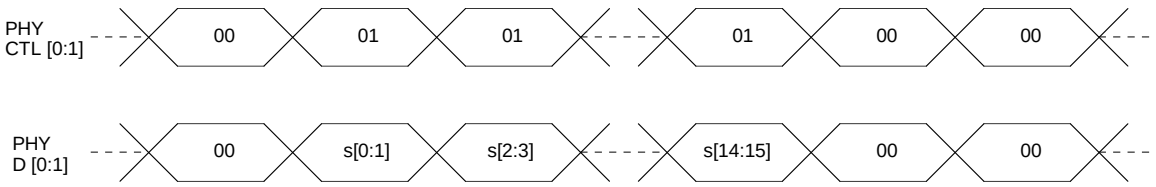
For write requests, the PHY takes the value in the data field of the transfer and loads it into the addressed register as soon as the transfer is complete. For read requests, the PHY returns the contents of the addressed register at the next opportunity through a status transfer. The LINK is allowed to perform a read or write operation at any time. If the status transfer is interrupted by an incoming packet, the PHY continues to attempt the transfer of the requested register until it is successful.

Once the LINK issues a request for access to the bus (immediate, iso, fair, or priority) it cannot issue another request until the PHY indicates "lost" (incoming packet) or "won" (transmit). The PHY ignores new requests while a previous request is pending.

Status Transfer

When the PHY has status information to transfer to the LINK, it will initiate a status transfer. The PHY will wait until the interface is idle to perform the transfer. The PHY initiates the transfer by asserting status (01b) on the CTL pins, along with the first two bits of status information on D [0 : 1]. The PHY maintains CTL = status for the duration of the status transfer. The PHY may prematurely end a status transfer by asserting something other than status on the CTL pins. This should be done in the event that a packet arrives before the status transfer completes. There must be at least one cycle in between consecutive status transfers.

Status Transfer Timing



Transmit:

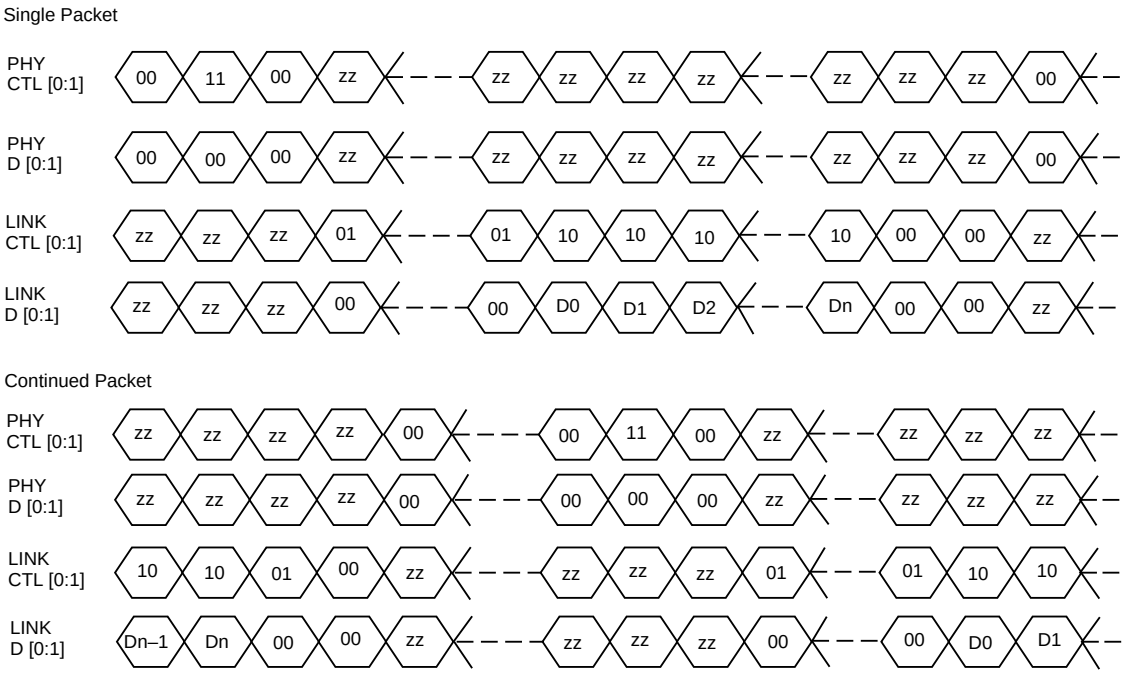
When the LINK requests access to the serial bus through the LREQ pin, the PHY arbitrates for access to the serial bus. If the PHY wins the arbitration, it grants the bus to the LINK by asserting transmit on the CTL pin for one SCLK cycle, followed by idle for one cycle. After sampling the transmit state from the PHY, the LINK takes over control of the interface by asserting either hold or transmit on the CTL pins. The LINK asserts hold to keep ownership of the bus while preparing data. The PHY asserts the data-on state on the serial bus during this time. When it is ready to begin transmitting a packet, the LINK asserts transmit on the CTL pins along with the first bits of the packet. After sending the last bits of the packet, the link asserts either idle or hold on the on the CTL pins for one cycle, and then idle for one additional cycle before tristating those pins.

The hold state here indicates to the PHY that the LINK needs to send another packet without releasing the bus. The PHY responds to this hold state by waiting the required minimum time and then asserting transmit as before. This function would be used after sending an acknowledge if the LINK intends to send a unified response, or to send consecutive isochronous packets during a single cycle. The only requirement when sending multiple packets during a single bus ownership is that all must be transmitted at the same speed, since the speed of the packet transmission is set before the first packet.

As noted above, when the LINK has finished sending the last packet for the current bus ownership, it releases the bus by asserting idle on the CTL pins for two SCLK cycles. The PHY begins asserting idle on the CTL pins one clock after sampling idle from the link. Note that whenever the D and CTL lines change “ownership” between the PHY and the LINK, there is an extra clock period allowed so that both sides of the interface can operate on registered versions of the interface signals, rather than having to respond to a CTL state on the next cycle.

Note that it is not required that the LINK enter the hold state before sending the first packet if implementation permits the LINK to be ready to transmit as soon as bus ownership is granted. The timing for a single packet transmit operation is shown below. In the diagram, D0 through Dn are the data symbols of the packet; zz represents high impedance state.

Transmit Timing



NOTES:
zz = Hi-Z
D0 to Dn = Packet data
This figure is for 100Mbps. For 200Mbps, D [0:3] is used.

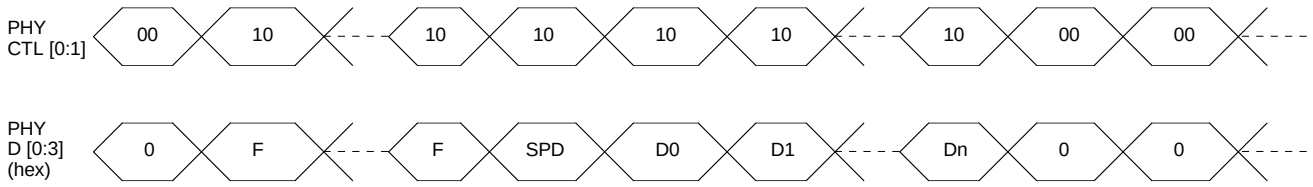
Receive:

Whenever the PHY sees the “data-on” state on the serial bus, it initiates a receive operation by asserting receive on the CTL pins and “1” on each of the D pins. The PHY indicates the start of a packet by placing the speed code (encoding shown below) on the D pins, followed by the contents of the packet, holding the CTL pins in receive until the last symbol of the packet has been transferred. The PHY indicates the end of the packet by asserting idle on the CTL pins. Note that the speed code is a PHY-LINK protocol and is not included in the calculation of the CRC or other data protection mechanisms.

It is possible that a PHY can see date-on appear and then disappear on the serial bus without seeing a packet. This is the case when a packet of a higher speed than the PHY can receive is being transmitted. In this case, the PHY will end the packet by asserting idle when the data-on state goes away.

If the PHY is capable of a higher data rate than the LINK, the LINK detects the speed code as such and ignores the packet until it sees the idle state again.

Receive Timing



NOTES:
SPD = speed code
D0 to Dn = data symbols of the packet; for 100Mbps, packet data is output to D [0 : 1] only.

The speed code for the receive operation is defined as follows:

Receive Speed Code

D[0 : 3]	Data Rate
00xx	100Mbps
0100	200Mbps

NOTE:
The “xx” means transmitted as 00, ignored on receive.

Power Class Programming

Power use or power supply from the cable requires certain settings. PC [2 : 0] is used for this setting.

The power classes are defined as follows:

PC [2 : 0]	Definition
000	The node does not consume cable power. Also, power does not repeat.
001	The node operates on its own power, and a minimum of 15W is supplied to the cable.
010	The node operates on its own power, and a minimum of 30W is supplied to the cable.
011	The node operates on its own power and a minimum of 45W is supplied to the cable.
100	The node may use cable power. Maximum required power is 1W.
101	The node may use cable power. Maximum required power is 1W. A further 2W are required to operate LINK and upper layer.
110	The node may use cable power. Maximum required power is 1W. A further 5W are required to operate LINK and upper layer.
111	The node may use cable power. Maximum required power is 1W. A further 9W are required to operate LINK and upper layer.

Additional Features

Short Bus Reset:

The short bus reset or arbitrated bus reset were proposed in the 1394 Trade Association by Apple Computer. The standardization, however, has not been done yet. The CXD1944R supports a short bus reset mode whose reset pulse width is 1.4µs instead of the normal bus reset pulse width of 166µs. This mode can be selected by connecting the TIO pin to V_{DD}. When the node needs to send a reset pulse, it will first arbitrate the bus according to the fair protocol as a FairReq. If it gets the bus grant, it will send a short bus reset pulse instead of a packet. This is called “arbitrated bus reset”, which ensures all nodes can detect the short bus reset pulse. Since it follows Fair protocol, it won’t disturb the isochronous cycle. This arbitrated bus reset can only work after the bus is initialized. Before the bus initialization, the node will send a short bus reset pulse immediately. In both cases, if a short bus reset fails, the node will send a normal long bus reset, so that the short bus reset mode can be used with an older PHY which does not support a short bus reset mode.

If the IBR bit of the internal PHY register is set to 1, the device will send a long reset pulse. To request a short arbitrated bus reset, write 1 to the ArbRsrReq bit in the reset mode.

Slow Mode:

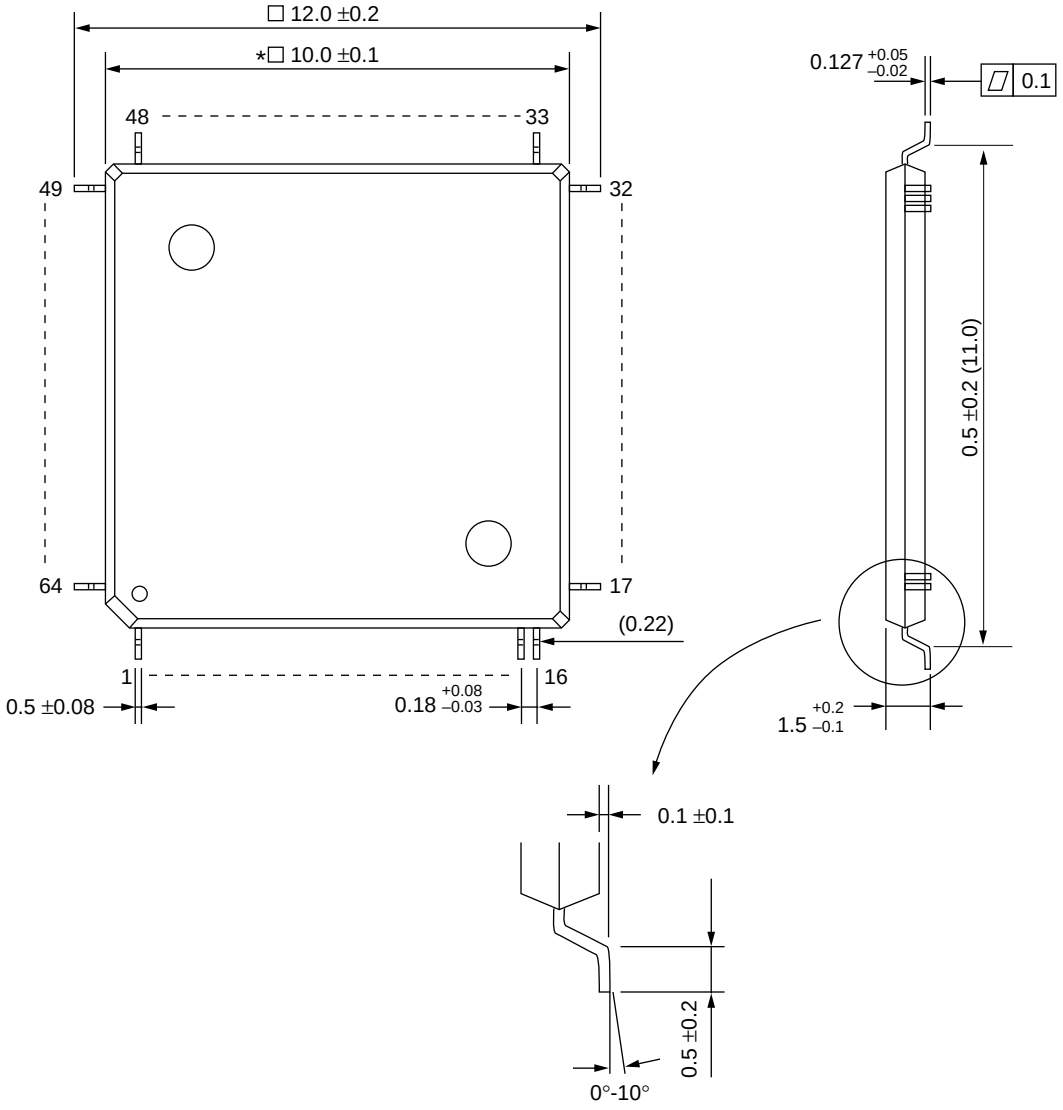
The CXD1944R supports 200Mbps. In some cable environments, however, 200Mbps may be difficult to operate; thus we have added the Slow Mode operation. By connecting XSLOW pin to ground, or writing a “1” to the Slow Bit of the internal PHY register, the device will act as a 100Mbps PHY. D[2:3] is still active in the slow mode.

Ping and Ping Timer:

Ping is used to measure a node-node packet delay. If the node received an R=0 and T=0 configuration packet, it will send a Self-ID packet immediately as an acknowledge. Since a LINK is not involved in this Self-ID transmission, and it is very quick, a sender can know the exact packet delay between the node and the remote node. LINK can read a Ping timer count after a Self-ID acknowledge. The Ping timer will be cleared and starts a count only when a configuration packet is sent from the node. The counter runs at 50MHz clock cycle. This feature is thought useful to optimize a gap count of the bus.

Package Outline Unit: mm

64 pin LQFP (Plastic)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-64P-L01
EIAJ CODE	*QFP064-P-1010-A
JEDEC CODE	—

Package Structure

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g