SONY

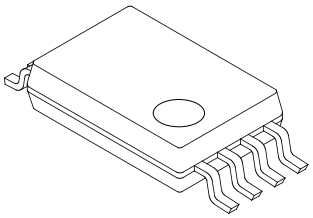
CXG1020AN

Power Amplifier for PHS

Description

The CXG1020AN is a power amplifier MMIC for PHS. This IC is designed using the Sony's GaAs J-FET process and operates at a single 3 V power supply.

8 pin SSOP (Plastic)



Features

- Single positive power supply operation
  V_{DD}=3.2 V
- Low current consumption 140 mA
- Gain 29 dB Typ.
- Distortion –58 dBc Typ.
  (for P_{OUT}=21 dB)
- Small mold package 8-pin SSOP

Structure

GaAs J-FET MMIC

Applications

Power amplifiers for PHS

Electrical Characteristics

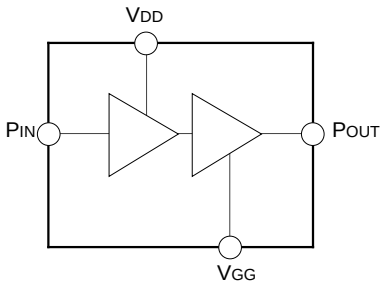
V_{DD}=3.2 V, f=1.90 GHz, P_{OUT}=21 dBm (Ta=25 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
*1 Current consumption	I_{DD}		140		mA
*1 Gate voltage adjustment value	V_{GG}	0	0.5	1.0	V
Power gain	G_P	26	29		dB
Average leak power level (600 kHz±100 kHz)	$P_{LEAK}600$		–58	–54	dBc
Average leak power level (900 kHz±100 kHz)	$P_{LEAK}900$		–60	–58	dBc

*1 Adjust V_{GG} so that I_{DD} becomes 140 mA for 21 dBm output.

E97120-TE

Block Diagram



Pin Configuration

Recommended Current Adjustment Method

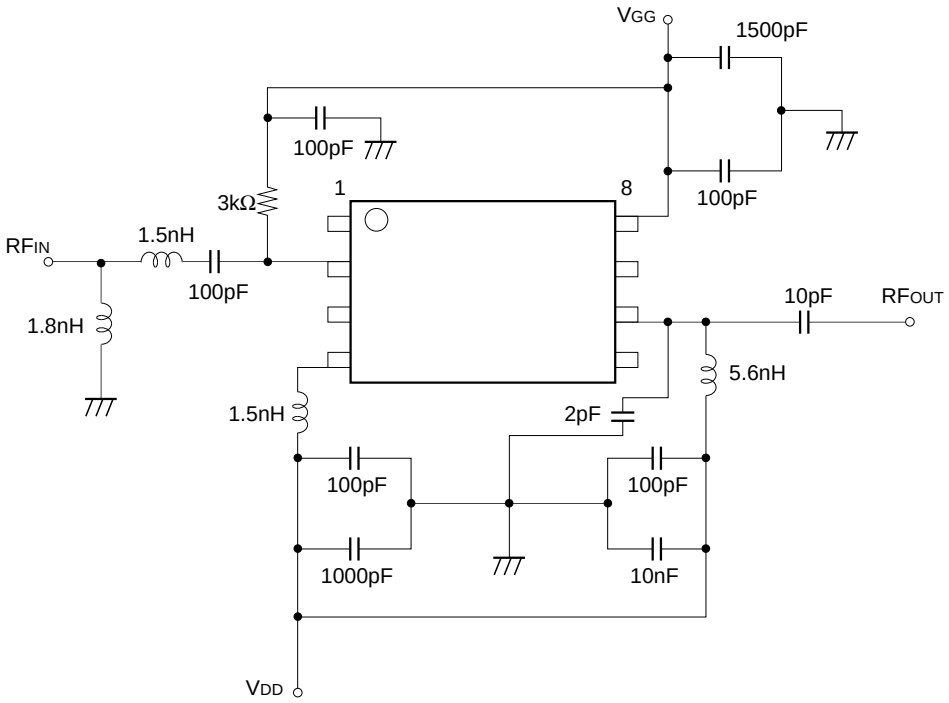
(1) V_{GG}/P_{IN} separate adjustment

(V_{GG} adjustment 1)	(P_{IN} adjustment 1)	(V_{GG} adjustment 2)	(P_{IN} adjustment 2)
When the RF input (P_{IN}) is off, the current consumption (I_{DD}) is adjusted to 135 mA.	The output power (P_{OUT}) is adjusted to 21.0 dBm.	The current consumption (I_{DD}) is finely adjusted to 140 mA.	The output power (P_{OUT}) is finely adjusted to 21.0 dBm.
Variation of I_{DD} and P_{OUT} due to adjustment	I_{DD}=140±10 mA P_{OUT}=21.0 dBm	I_{DD}=140 mA P_{OUT}=21.0±0.2 dBm	I_{DD}=140±3 mA P_{OUT}=21.0 dBm

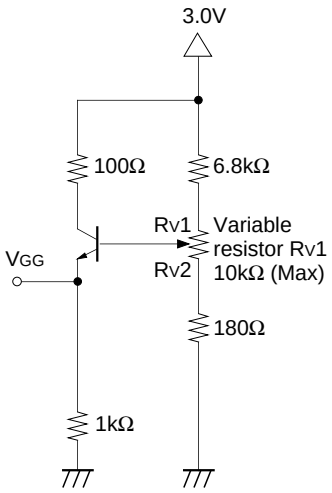
(2) Simple adjustment

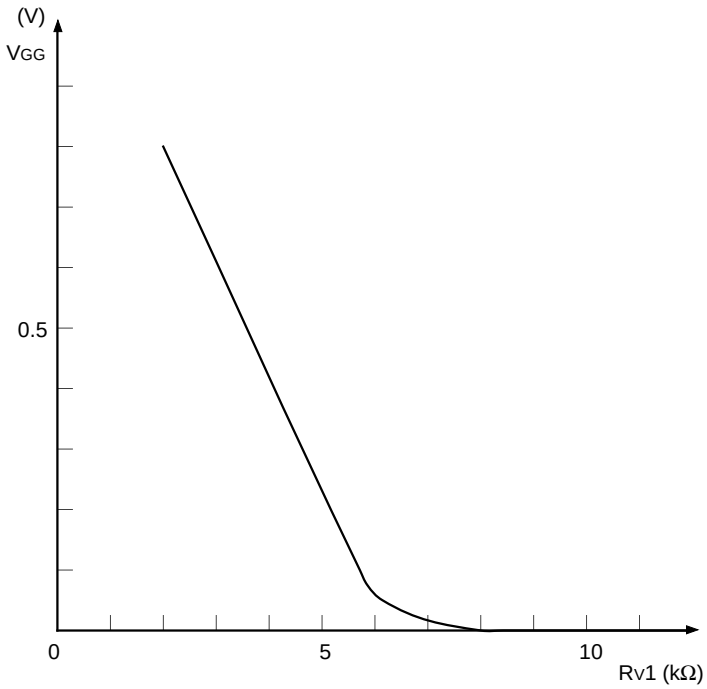
(I_{DD} read)	(V_{GG} setting)	(P_{IN} adjustment)
When the RF input (P_{IN}) is off, the gate voltage (V_{GG}) is set to 0.3 V and it is read.	The formula*1 where V_{GG}=f (I_{DD}: V_{GG}= 0.3 V) is used to set V_{GG}.	The output power (P_{OUT}) is adjusted to 21.0 dBm.
Variation of I_{DD} and P_{OUT} due to adjustment	*1 e.g. V_{GG}=a – b×I_{DD}	I_{DD}=140±5 mA P_{OUT}=21.0 dBm

Application Circuit Configuration (1.9 GHz-band PHS)



Recommended Gate Bias Circuit and Circuit Characteristics





Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

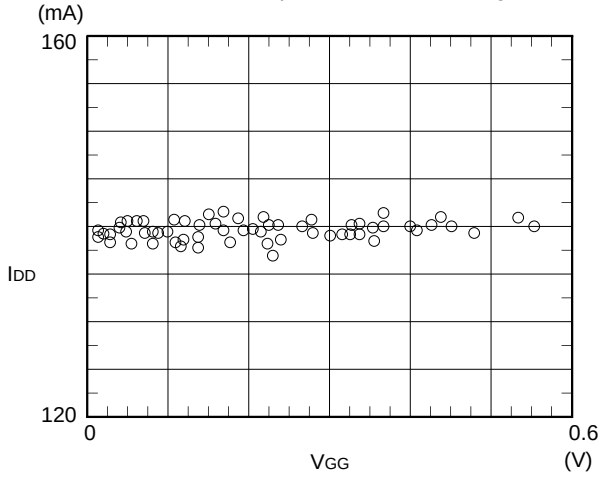
Current Consumption Variation with Recommended Current Adjustment Method

(For P_{OUT}=21 dBm output)

(1) Separate adjustment

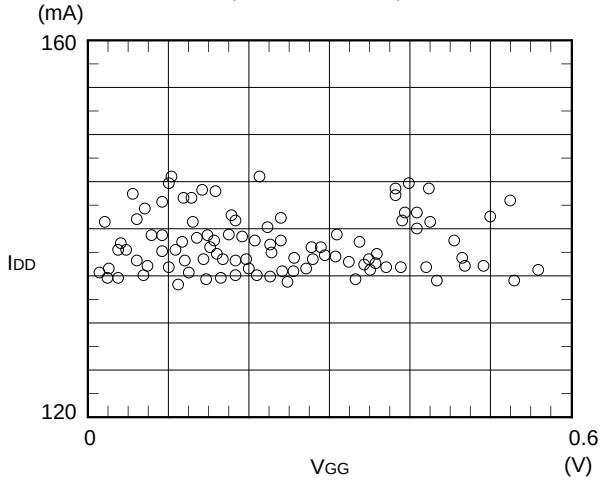
V_{GG}/P_{IN} separate adjustment method
(I_{DD} distribution after executing the P_{IN} adjustment 1)

V_{GG}/P_{IN} separate adjustment method
(I_{DD} distribution after executing the P_{IN} adjustment 1)



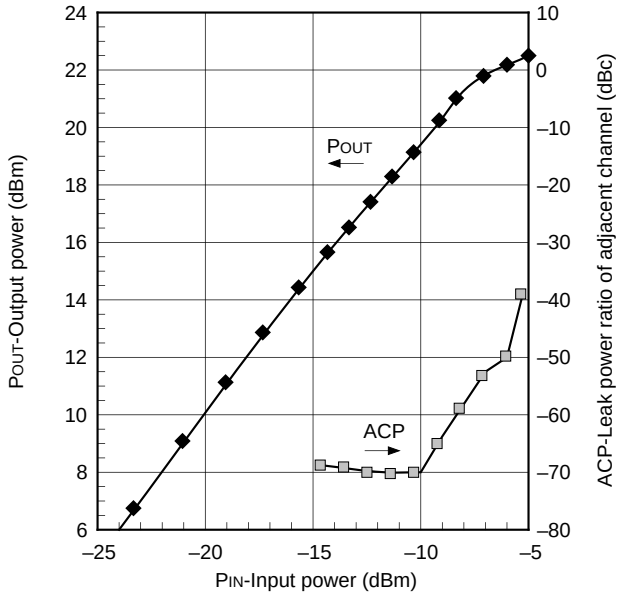
(2) Simple adjustment

Simple adjustment method
(I_{DD} distribution after executing the P_{IN} adjustment)
$V_{GG}=a-b \times I_{DD}$ (P_{IN} off/V_{GG}=0.3V) : a=0.8021, b=0.003

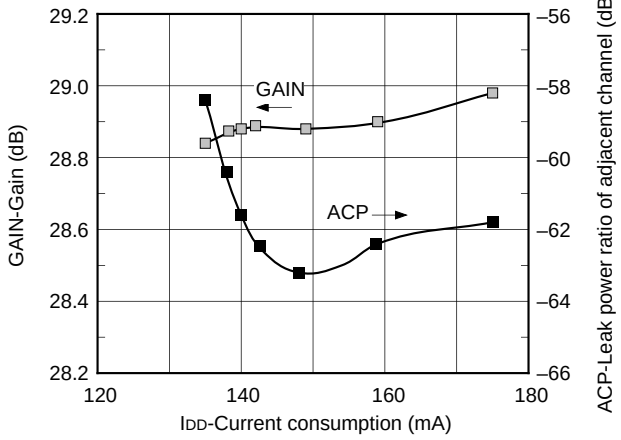


Example of Representative Characteristics (Ta=25 °C, Freq=1.9 GHz)

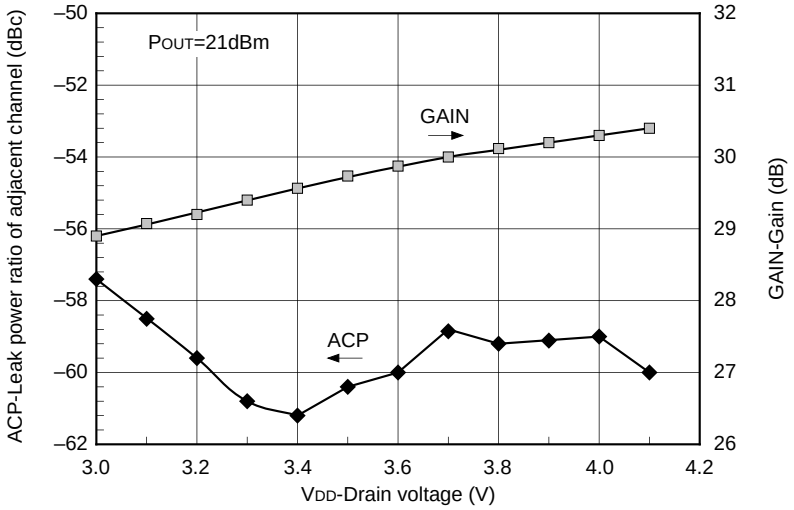
Input/output characteristics (P_{OUT}/ACP)
V_{DD}=3.2V, I_{DD}=140mA@P_{OUT}=21dBm



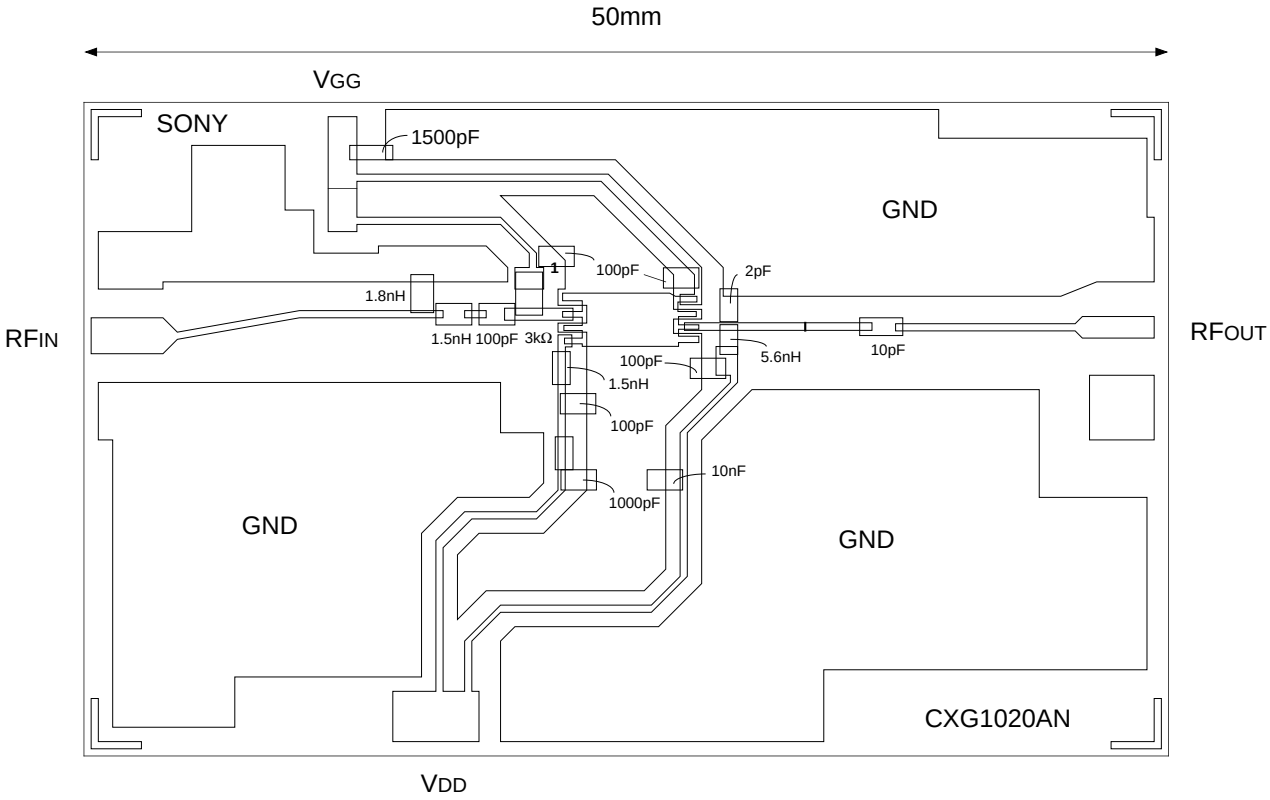
GAIN, ACP vs. I_{DD}
V_{DD}=3.2V, P_{OUT}=21dBm



GAIN, ACP vs. V_{DD}
P_{OUT}/V_{GG} constant (P_{OUT}=21dBm, I_{DD}=140mA@V_{DD}=3.6V)



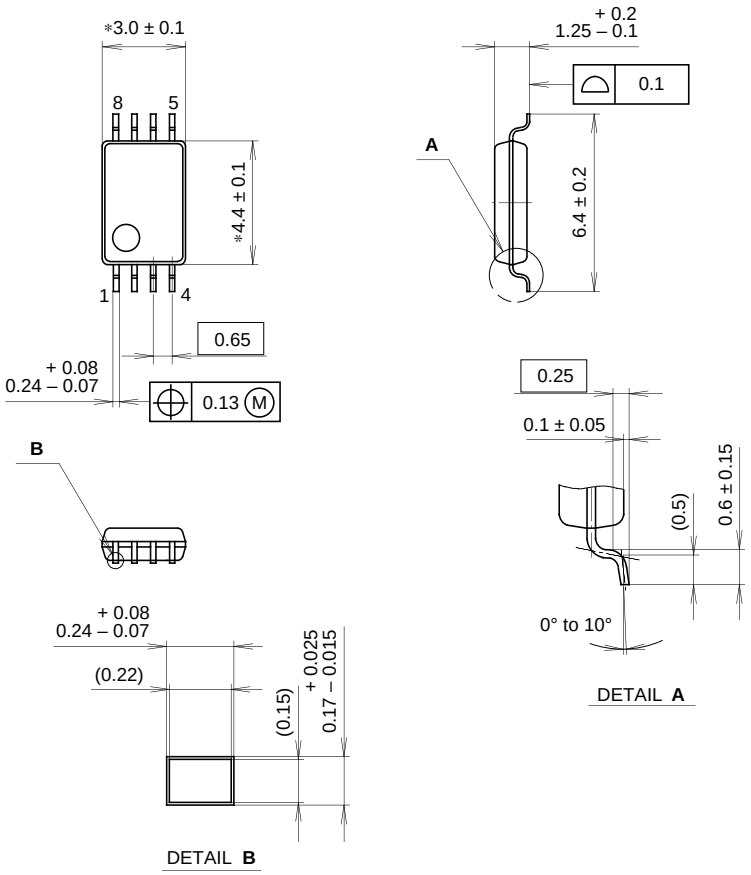
Recommended Evaluation Board



Material : Glass fabric-base epoxy
Thickness : 0.2 mm
Back side : Overall GND

Package Outline Unit : mm

8PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-8P-L01
EIAJ CODE	SSOP008-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.04g