SONY

SP10T Antenna Switch for GSM/UMTS Dual Mode Handsets

CXM3567XR

Description

The CXM3567XR is SP10T antenna switch for GSM and UMTS dual mode handsets.
The CXM3567XR has a 1.8 V CMOS compatible decoder.
The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity.
(Applications: GSM (2bands)/UMTS (6bands) Dual-Mode Handsets)

Features

◆ Low Insertion Loss: 0.40 dB (Typ.) Tx1 (GSM Low Band Tx)
0.55 dB (Typ.) Tx2 (GSM High Band Tx)
0.65 dB (Typ.) TRx (UMTS)

◆ Low Voltage Operation: V_{DD} = 2.3 V
◆ No DC Blocking Capacitors
◆ Small package size: XQFN-24P-02 (2.2 mm × 2.9 mm × 0.4 mm Max.)
◆ Lead-Free and RoHS Compliant

Structure

GaAs Junction Gate pHEMT JPHEMT MMIC Switch, CMOS Decoder

Absolute Maximum Ratings

(Ta = 25 ℃)

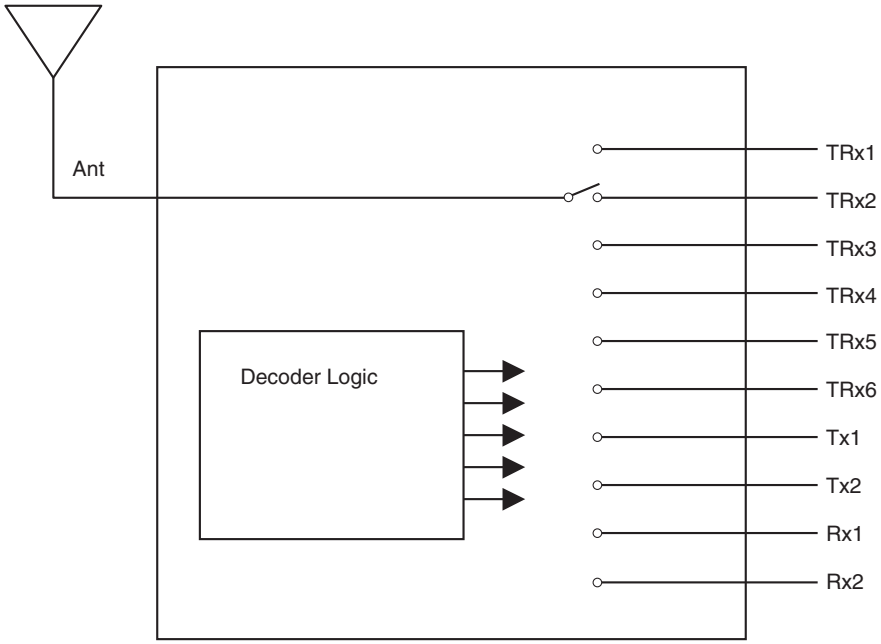
◆ Bias voltage	V_{DD}	4	V
◆ Control voltage (CTL-A/B/C/D)	Vctl	4	V
◆ Input power max. [Tx1]		36	dBm (Duty cycle = 12.5 to 50 %)
◆ Input power max. [Tx2]		34	dBm (Duty cycle = 12.5 to 50 %)
◆ Input power max. [TRx1, 2, 3, 4, 5, 6]		32	dBm
◆ Input power max. [Rx1, 2]		13	dBm
◆ Operating temperature range		–35 to +85	℃
◆ Storage temperature range		–65 to +150	℃

Note on Handling
GaAs MMIC's are ESD sensitive devices. Special handling precautions are required.

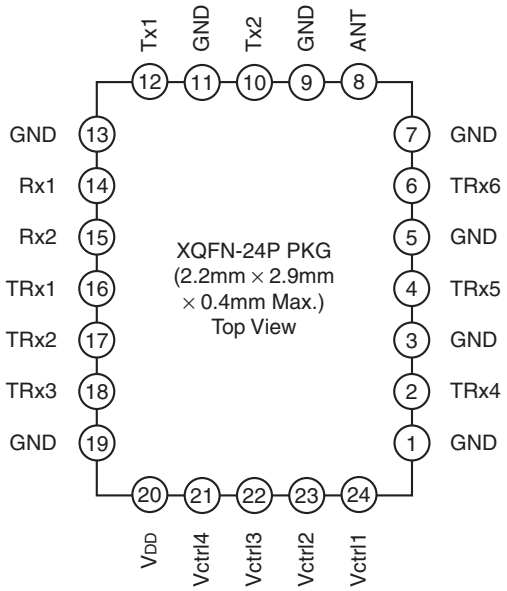
E10807

Block Diagram

SP10T Antenna Switch Module



Pin Configuration



Pin Description

Pin No.	Name	Pin No.	Name
1	GND	13	GND
2	TRx4	14	Rx1
3	GND	15	Rx2
4	TRx5	16	TRx1
5	GND	17	TRx2
6	TRx6	18	TRx3
7	GND	19	GND
8	Ant	20	V_{DD}
9	GND	21	Vctrl4
10	Tx2 (DCS/PCS)	22	Vctrl3
11	GND	23	Vctrl2
12	Tx1 (GSM850/900M)	24	Vctrl1

Truth Table

State	Active Path	Vctl State			
		1	2	3	4
1	Tx1	H	H	L	L
2	Tx2	H	L	L	L
3	Rx1	L	L	L	L
4	Rx2	L	L	H	L
5	TRx1	L	H	H	L
6	TRx2	L	H	L	L
7	TRx3	H	L	H	L
8	TRx4	H	H	H	L
9	TRx5	H	L	H	H
10	TRx6	H	H	H	H
11	Sleep	L	L	L	H

Electrical Characteristics

Supply Voltage Value

(Ta = 25 °C)

Item	Min.	Typ.	Max.	Unit
Bias voltage (V_{DD})	+2.3	+2.65	+3.3	V

Logic Value

(Ta = 25 °C)

Item	State	Min.	Typ.	Max.	Unit
Control voltage (CTL-A/B/C/D)	High	+1.5	+1.8	+3.3	V
	Low	0	—	+0.3	

Specification

(Ta = 25 °C, V_{DD} = 2.3 V, Vctl = 1.5 V)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Ant-Tx1	*1	—	0.40	0.55	dB
		Ant-Tx2	*2	—	0.55	0.70	
		Ant-Rx1	*3	—	0.80	0.95	
			*4	—	1.00	1.15	
		Ant-Rx2	*3	—	0.85	1.00	
			*4	—	1.05	1.20	
		Ant-TRx1	*5	—	0.50	0.65	
			*6	—	0.70	0.85	
		Ant-TRx2	*5	—	0.50	0.65	
			*6	—	0.70	0.85	
		Ant-TRx3	*5	—	0.45	0.60	
			*6	—	0.60	0.75	
		Ant-TRx4	*5	—	0.50	0.65	
			*6	—	0.60	0.75	
		Ant-TRx5	*5	—	0.50	0.65	
			*6	—	0.60	0.75	
		Ant-TRx6	*5	—	0.50	0.65	
			*6	—	0.65	0.80	
VSWR	VSWR	All ports in Active Paths	824 to 2170 MHz	—	1.20	—	—
Harmonics	2fo	Tx1-Ant	*1	—	–46	–36	dBm
	3fo			—	–45	–36	
	2fo	Tx2-Ant	*2	—	–67	–36	
	3fo			—	–50	–36	
	2fo	TRx1-Ant	*5,*6	—	–62	–39	
	3fo			—	–63	–39	
	2fo	TRx2-Ant	*5,*6	—	–62	–39	
	3fo			—	–63	–39	
	2fo	TRx3-Ant	*5,*6	—	–64	–39	
	3fo			—	–68	–39	
	2fo	TRx4-Ant	*5,*6	—	–70	–39	
	3fo			—	–65	–39	
	2fo	TRx5-Ant	*5,*6	—	–68	–39	
	3fo			—	–62	–39	
	2fo	TRx6-Ant	*5,*6	—	–70	–39	
	3fo			—	–64	–39	
Inter modulation product power in Rx band	IMD2	TRx1-Ant	*7, *9	—	–104	–102	dBm
		TRx2-Ant	*7, *9	—	–105	–102	
		TRx3-Ant	*7, *9	—	–107	–102	
		TRx4-Ant	*7, *9	—	–111	–102	
		TRx5-Ant	*7, *9	—	–109	–102	
		TRx6-Ant	*7, *9	—	–109	–102	
	IMD3	TRx1-Ant	*8, *9	—	–110	–102	
		TRx2-Ant	*8, *9	—	–109	–102	
		TRx3-Ant	*8, *9	—	–113	–102	
		TRx4-Ant	*8, *9	—	–110	–102	
		TRx5-Ant	*8, *9	—	–106	–102	
		TRx6-Ant	*8, *9	—	–108	–102	

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Switching time	Ts		50 %Ctl to 90 %RF	—	3	5	μS
Control current	Ictl		Vctl = 1.80 V	—	1	5	μA
Supply current	Idd		V_{DD} = 2.65 V	—	0.19	0.40	mA
Sleep current	Isleep		Sleep mode *state11 V_{DD} = 2.65 V	—	4	10	μA

Electrical Characteristics are measured with all RF ports terminated in 50Ω.

*1 Pin on Tx1: 34 dBm, 915 MHz, Tx1 enabled

*2 Pin on Tx2: 32 dBm, 1910 MHz, Tx2 enabled

*3 Pin on Ant: 10 dBm, 960 MHz, Rx1, Rx2 enabled

*4 Pin on Ant: 10 dBm, 1990 MHz, Rx1, Rx2 enabled

*5 Pin on TRx1, TRx2, TRx3, TRx4,TRx5, TRx6: 26 dBm, 900 MHz, TRx1, TRx2, TRx3, TRx4, TRx5, TRx6 enabled

*6 Pin on TRx1, TRx2, TRx3, TRx4,TRx5, TRx6: 26 dBm, 1980 MHz, TRx1, TRx2, TRx3, TRx4, TRx5, TRx6 enabled

*7 Pin on TRx1, TRx2, TRx3, TRx4,TRx5, TRx6: 20 dBm, 1950 MHz, Pin on Ant: –15 dBm, 190 MHz, TRx1, TRx2, TRx3, TRx4, TRx5, TRx6 enabled

*8 Pin on TRx1, TRx2, TRx3, TRx4,TRx5, TRx6: 20 dBm, 1950 MHz, Pin on Ant: –15 dBm, 1760 MHz, TRx1, TRx2, TRx3, TRx4, TRx5, TRx6 enabled

*9 Measured with the recommended circuit

Specification Isolation1

(Ta = 25 °C, V_{DD} = 2.3 V, Vctl = 1.5 V)

Item	Symbol	Path		Condition	Min.	Typ.	Max.	Unit
		Active	Isolation					
Isolation	ISO	Tx1	Tx1-Rx1	824 to 915 MHz	30	51	—	dB
			Tx1-Rx2		30	54	—	
			Tx1-TRx1		30	53	—	
			Tx1-TRx2		30	53	—	
			Tx1-TRx3		30	55	—	
			Tx1-TRx4		30	55	—	
			Tx1-TRx5		30	55	—	
			Tx1-TRx6		30	54	—	
			Tx1-Tx2		24	34	—	
			Tx1-Tx2	1648 to 1830 MHz	18	27	—	
		Tx2	Tx2-Rx1	1710 to 1910 MHz	30	55	—	
			Tx2-Rx2		30	55	—	
			Tx1-TRx1		30	53	—	
			Tx1-TRx2		30	54	—	
			Tx1-TRx3		30	49	—	
			Tx1-TRx4		30	46	—	
			Tx1-TRx5		30	47	—	
			Tx1-TRx6		30	51	—	
			Tx2-Tx1		19	29	—	
		TRx1	TRx1-Rx1	900 MHz	30	49	—	
			TRx1-Rx2		23	33	—	
			TRx1-Tx1		30	47	—	
			TRx1-Tx2		30	49	—	
			TRx1-TRx2		23	33	—	
			TRx1-TRx3		30	46	—	
			TRx1-TRx4		30	55	—	
			TRx1-TRx5		30	55	—	
			TRx1-TRx6		30	54	—	
			TRx1-Rx1	1980 MHz	30	41	—	
			TRx1-Rx2		18	27	—	
			TRx1-Tx1		24	34	—	
			TRx1-Tx2		27	37	—	
			TRx1-TRx2		18	26	—	
			TRx1-TRx3		21	31	—	
			TRx1-TRx4		30	48	—	
			TRx1-TRx5		30	52	—	
			TRx1-TRx6		30	55	—	

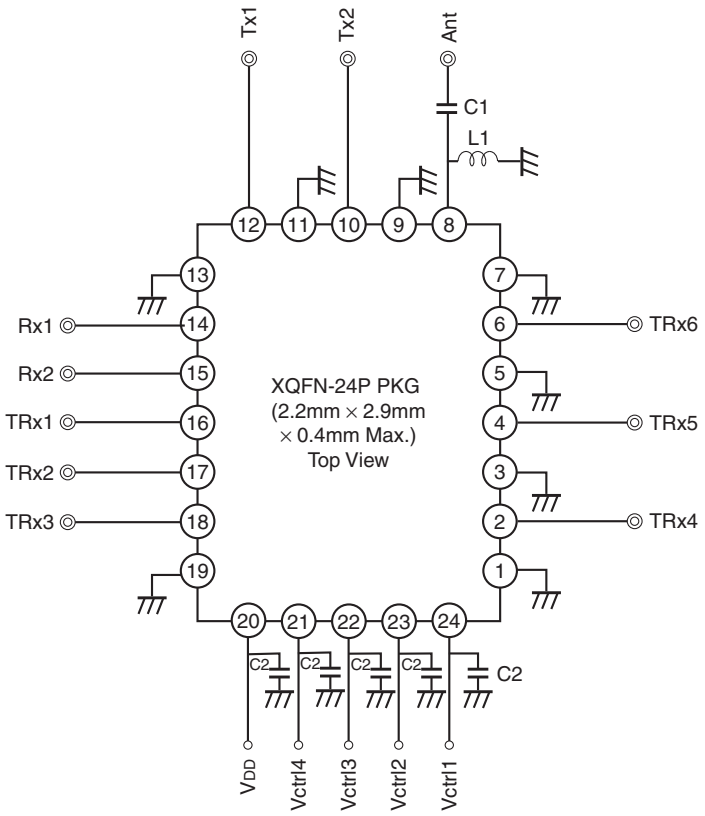
Item	Symbol	Path		Condition	Min.	Typ.	Max.	Unit
		Active	Isolation					
Isolation	ISO	TRx2	TRx2-Rx1	900 MHz	30	53	—	dB
			TRx2-Rx2		30	48	—	
			TRx2-Tx1		30	49	—	
			TRx2-Tx2		30	50	—	
			TRx2-TRx1		22	32	—	
			TRx2-TRx3		24	34	—	
			TRx2-TRx4		30	55	—	
			TRx2-TRx5		30	55	—	
			TRx2-TRx6		30	54	—	
			TRx2-Rx1	1980 MHz	30	50	—	
			TRx2-Rx2		30	41	—	
			TRx2-Tx1		25	35	—	
			TRx2-Tx2		28	38	—	
			TRx2-TRx1		18	25	—	
			TRx2-TRx3		18	25	—	
			TRx2-TRx4		30	47	—	
			TRx2-TRx5		30	51	—	
			TRx2-TRx6		20	55	—	
		TRx3	TRx3-Rx1	900 MHz	30	54	—	
			TRx3-Rx2		30	52	—	
			TRx3-Tx1		30	55	—	
			TRx3-Tx2		30	51	—	
			TRx2-TRx1		30	45	—	
			TRx2-TRx2		23	33	—	
			TRx2-TRx4		30	55	—	
			TRx2-TRx5		30	55	—	
			TRx2-TRx6		30	54	—	
			TRx3-Rx1	1980 MHz	30	55	—	
			TRx3-Rx2		30	53	—	
			TRx3-Tx1		30	40	—	
			TRx3-Tx2		28	38	—	
			TRx2-TRx1		27	37	—	
			TRx2-TRx2		18	26	—	
			TRx2-TRx4		30	46	—	
			TRx2-TRx5		30	50	—	
			TRx2-TRx6		30	55	—	

Item	Symbol	Path		Condition	Min.	Typ.	Max.	Unit
		Active	Isolation					
Isolation	ISO	TRx4	TRx4-Rx1	900 MHz	30	55	—	dB
			TRx4-Rx2		30	55	—	
			TRx4-Tx1		30	53	—	
			TRx4-Tx2		30	45	—	
			TRx4-TRx1		30	55	—	
			TRx4-TRx2		30	54	—	
			TRx4-TRx3		30	55	—	
			TRx4-TRx5		28	38	—	
			TRx4-TRx6		30	52	—	
			TRx4-Rx1	1980 MHz	30	55	—	
			TRx4-Rx2		30	55	—	
			TRx4-Tx1		30	42	—	
			TRx4-Tx2		23	33	—	
			TRx4-TRx1		30	52	—	
			TRx4-TRx2		30	50	—	
			TRx4-TRx3		30	45	—	
			TRx4-TRx5		18	28	—	
			TRx4-TRx6		30	41	—	
		TRx5	TRx5-Rx1	900 MHz	30	55	—	
			TRx5-Rx2		30	55	—	
			TRx5-Tx1		30	54	—	
			TRx5-Tx2		30	45	—	
			TRx5-TRx1		30	55	—	
			TRx5-TRx2		30	55	—	
			TRx5-TRx3		30	55	—	
			TRx5-TRx4		29	39	—	
			TRx5-TRx6		30	45	—	
			TRx5-Rx1	1980 MHz	30	55	—	
			TRx5-Rx2		30	55	—	
			TRx5-Tx1		30	42	—	
			TRx5-Tx2		23	33	—	
			TRx5-TRx1		30	53	—	
			TRx5-TRx2		30	51	—	
			TRx5-TRx3		30	45	—	
			TRx5-TRx4		18	28	—	
			TRx5-TRx6		25	35	—	

Item	Symbol	Path		Condition	Min.	Typ.	Max.	Unit
		Active	Isolation					
Isolation	ISO	TRx6	TRx6-Rx1	900 MHz	30	55	—	dB
			TRx6-Rx2		30	55	—	
			TRx6-Tx1		30	55	—	
			TRx6-Tx2		30	45	—	
			TRx6-TRx1		30	55	—	
			TRx6-TRx2		30	53	—	
			TRx6-TRx3		30	55	—	
			TRx6-TRx4		30	53	—	
			TRx6-TRx5		30	46	—	
			TRx6-Rx1	1980 MHz	30	55	—	
			TRx6-Rx2		30	55	—	
			TRx6-Tx1		30	41	—	
			TRx6-Tx2		23	33	—	
			TRx6-TRx1		30	54	—	
			TRx6-TRx2		30	40	—	
			TRx6-TRx3		30	46	—	
			TRx6-TRx4		30	40	—	
			TRx6-TRx5		25	35	—	

Electrical Characteristics are measured with all RF ports terminated in 50Ω.

Recommended Circuit



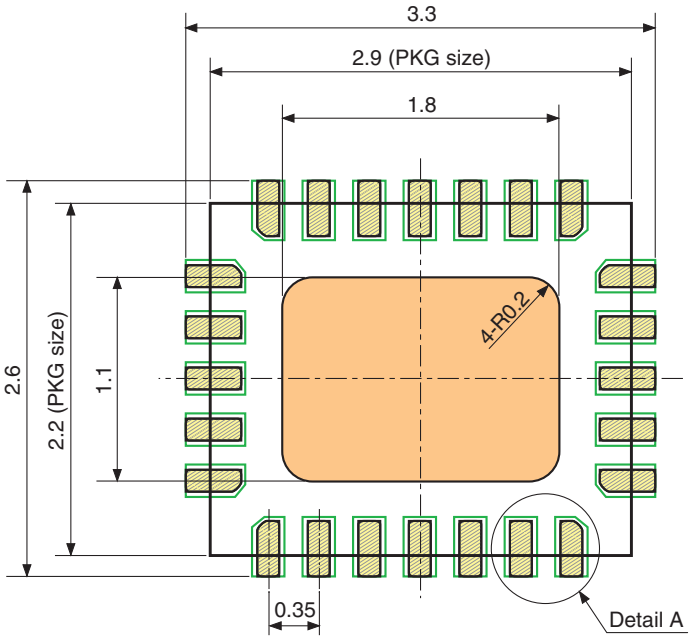
Note) 1. No DC blocking Capacitors are required on all RF ports.
2. DC levels of all RF ports are GND.
3. L1 Inductor(22nH) and C1 Capacitor(22pF) are recommended on Ant port for ESD protection.
4. C2 Capacitor (100pF) is recommended.

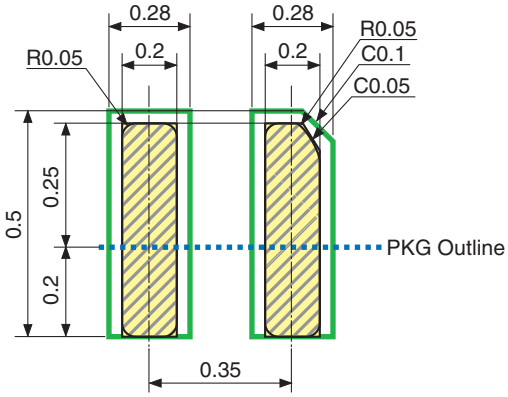
PCB Layout Template

XQFN-24P-02 Macro for MMIC (Reference)

Specification

- PKG size: 2.9 mm × 2.2 mm t0.35 mm
- Terminal pitch: 0.35 mm
- Terminal length: 0.25 mm
- Mask thickness: 0.11 mm





Detail A

: Land area

: Mask open area (Solder printing area)

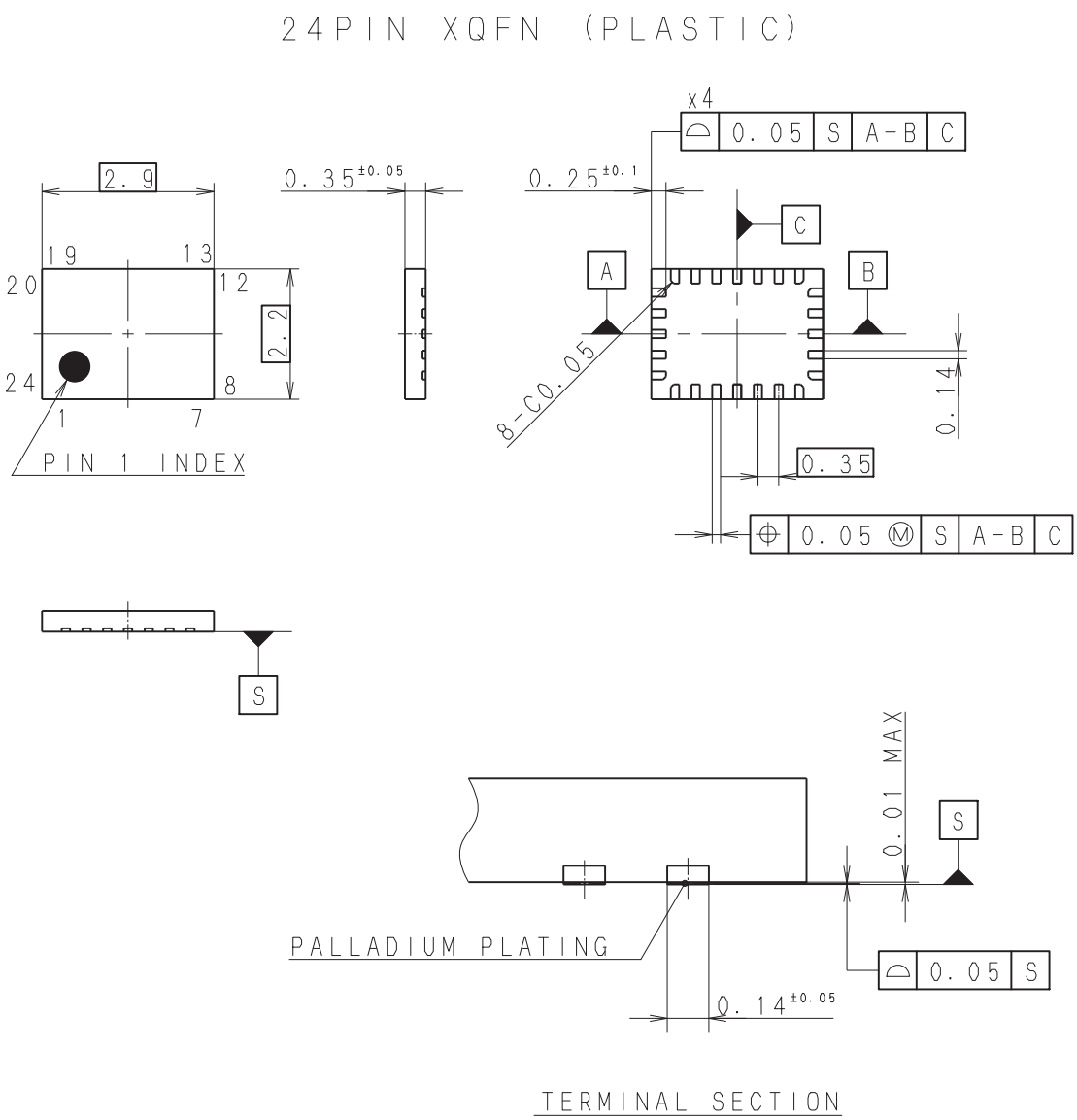
: Board resist open area

: Metal area in board (GND plane is recommended.)

: PKG outline

Package Outline

(Unit: mm)



Note:Terminal burr height 0.05mm MAX.

SONY CODE	XQFN-24P-02
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.006g

PART No. AP-4000-24047S	Rev. 1
ISSUED '10.06.03	REVISED '10.07.27
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR KYUSHU
REMARKS PKG CODE:XR-024-P	