

## Features

- Low-voltage operation  $V_{DD} = 3.3\text{ V}$
- 1:8 fanout
- Operation to 350 MHz
- Single input configurable for LVDS, LVPECL, or LVTTTL
- 8 pair of LVPECL outputs
- Drives a 50 ohm load
- Low input capacitance
- Low output skew
- Low propagation delay ( $t_{pd} = 4\text{ ns}$ , typical)
- Industrial temperature range
- 38-pin TSSOP Package

## Description

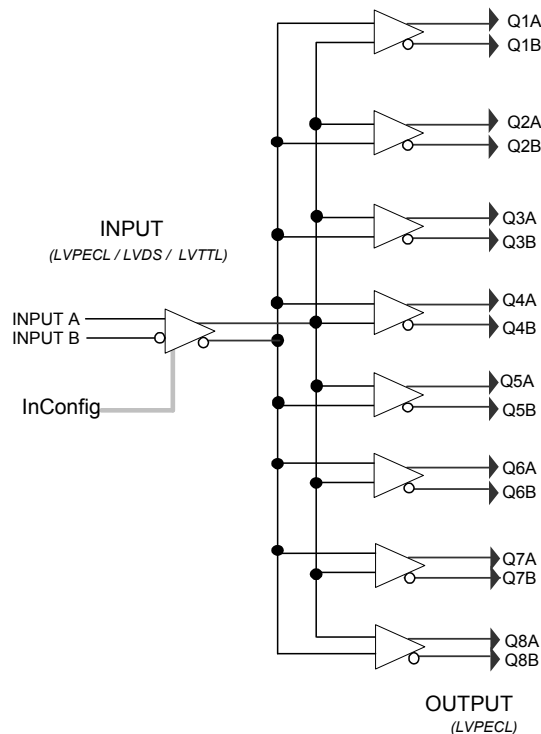
The Cypress CY2DP818 fanout buffer features a single LVDS or a single ended LVTTTL compatible input and eight LVPECL output pairs.

Designed for data-communications clock management applications, the large fanout from a single input reduces loading on the input clock.

The CY2DP818 is ideal for both level translations from single ended to LVPECL and/or for the distribution of LVPECL based clock signals.

The Cypress CY2DP818 has configurable input functions. The input is user configurable via the InConfig pin for single ended or differential input.

## Logic Block Diagram

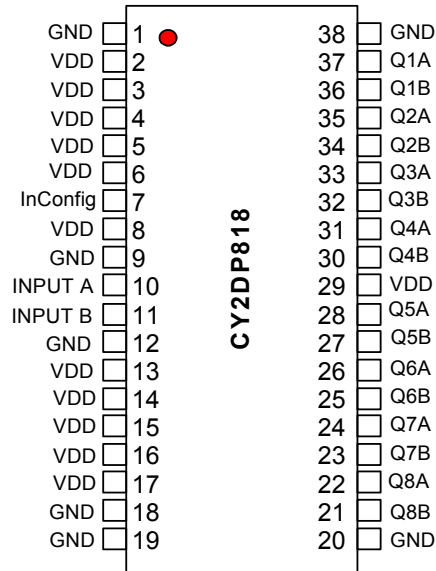


## Contents

<b>Pin Configuration</b> .....	<b>3</b>	<b>Acronyms</b> .....	<b>11</b>
<b>Pin Description</b> .....	<b>3</b>	<b>Document Conventions</b> .....	<b>11</b>
<b>Maximum Ratings</b> .....	<b>5</b>	Units of Measure .....	11
<b>DC Electrical Specifications</b> .....	<b>6</b>	<b>Document History Page</b> .....	<b>12</b>
<b>AC Switching Characteristics</b> .....	<b>7</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>13</b>
<b>Ordering Information</b> .....	<b>9</b>	Worldwide Sales and Design Support .....	13
Ordering Code Definitions .....	9	Products .....	13
<b>Package Drawing and Dimensions</b> .....	<b>10</b>	PSoC Solutions .....	13

## Pin Configuration

Figure 1. 38-pin TSSOP pinout



## Pin Description

Pin Number	Pin Name	Type	Description
1, 9, 12, 18, 19, 20, 38	GND	POWER	Ground
2, 3, 4, 5, 6, 8, 13, 14, 15, 16, 17, 29	VDD	POWER	Power Supply
10, 11	Input A, Input B	Default: LVPECL/LDVS Optional: LVTTTL/LVCMOS single pin	Clock Input. Either differential LVPECL/LVDS or single-ended LVTTTL/LVCMOS, as determined by InConfig. See <a href="#">Table 1</a> and <a href="#">Table 2</a> for details.
37, 36, 35, 34, 33, 32, 31, 30, 28, 27, 26, 25, 24, 23, 22, 21	Q1(A,B), Q2(A,B), Q3(A,B), Q4(A,B), Q5(A,B), Q6(A,B), Q7(A,B), Q8(A,B)	LVPECL	Differential Output Clocks
7	InConfig	LVTTTL/LVCMOS	Control Input. Selects input type: either differential LVPECL/LVDS or single-ended LVTTTL/LVCMOS. See <a href="#">Table 1</a> and <a href="#">Table 2</a> for details.

**Table 1. Input Receiver Configuration for Differential or LVTTTL/LVCMOS**

InConfig (Pin 7)	Input Receiver Family	Input Receiver Type
1	LVTTTL or LVCMOS	Single ended, non-inverting or inverting, void of bias resistors
0	LVDS or LVPECL	Differential, void of internal termination

**Table 2. Single ended LVTTTL/LVCMOS Input Logic (InConfig = 1)**

Input A (+) Pin 10	Input B (-) Pin 11	Output Clock QnA Pins
Input	Ground	True
Input	VDD	Invert
Ground	Input	Invert
VDD	Input	True

## Maximum Ratings

Exceeding maximum ratings <sup>[1]</sup> may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature: ..... -65 °C to +150 °C

Ambient Temperature: ..... -40 °C to +85 °C

Supply Voltage to Ground Potential  
(Inputs and V<sub>DD</sub> only) ..... -0.3 V to 4.6 V

Supply Voltage to Ground Potential  
(Outputs only) ..... -0.3 V to V<sub>DD</sub> + 0.3 V

DC Input Voltage ..... -0.3 V to V<sub>DD</sub> + 0.3 V

DC Output Voltage ..... -0.3 V to V<sub>DD</sub> + 0.9 V

Power Dissipation ..... 0.75 W

**Table 3. Power Supply Characteristics**

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I <sub>CC</sub>	Dynamic Power Supply Current	V <sub>DD</sub> = Max Input toggling 50% Duty Cycle, Outputs Open	–	1.5	2.0	mA
I <sub>C</sub>	Total Power Supply Current	V <sub>DD</sub> = Max Input toggling 50% Duty Cycle, Outputs 50 ohms f <sub>L</sub> = 100 MHz	–	–	350	mA
I <sub>C(Core)</sub>	Core current when output loads are disabled	V <sub>DD</sub> = Max Input toggling 50% Duty Cycle, Outputs not connected to VTT f <sub>L</sub> = 100 MHz	–	–	50	mA

**Note**

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC Electrical Specifications

**Table 4. LVDS Input,  $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$** 

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{ID}$	Magnitude of Differential Input Voltage		100	–	600	mV
$V_{IC}$	Common-mode of Differential Input Voltage $ V_{ID} $ (min and max)		$ V_{ID} /2$	$2.4 - ( V_{ID} /2)$		V
$V_{IH}$	Input High Voltage	Guaranteed Logic High Level	2	–	–	V
$V_{IL}$	Input Low Voltage	Guaranteed Logic Low Level	–	–	0.8	V
$I_{IH}$	Input High Current	$V_{DD} = \text{Max}$ , $V_{IN} = V_{DD}$	–	$\pm 10$	$\pm 20$	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{DD} = \text{Max}$ , $V_{IN} = V_{SS}$	–	$\pm 10$	$\pm 20$	$\mu\text{A}$

**Table 5. LVPECL Input,  $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$** 

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{ID}$	Differential Input Voltage p-p	Guaranteed Logic High Level	400	–	2600	mV
$V_{IH}$	Input High Voltage	Guaranteed Logic High Level	2.15	–	2.4	V
$V_{IL}$	Input Low Voltage	Guaranteed Logic Low Level	1.5	–	1.8	V
$I_{IH}$	Input High Current	$V_{DD} = \text{Max}$ , $V_{IN} = V_{DD}$	–	$\pm 10$	$\pm 20$	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{DD} = \text{Max}$ , $V_{IN} = V_{SS}$	–	$\pm 10$	$\pm 20$	$\mu\text{A}$
$V_{CM}$	Common-mode Voltage		–	–	225	mV

**Table 6. LVTTTL/LVC MOS Input,  $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$** 

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{IH}$	Input High Voltage		2	–	–	V
$V_{IL}$	Input Low Voltage		–	–	0.8	V
$I_{IH}$	Input High Current	$V_{DD} = \text{Max}$ , $V_{IN} = 2.7\text{ V}$	–	–	1	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{DD} = \text{Max}$ , $V_{IN} = 0.5\text{ V}$	–	–	–1	$\mu\text{A}$
$I_I$	Input High Current	$V_{DD} = \text{Max}$ , $V_{IN} = V_{DD(\text{Max})}$	–	–	20	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{DD} = \text{Min}$ , $I_{IN} = -18\text{ mA}$	–	–0.7	–1.2	V
$V_H$	Input Hysteresis		–	80	–	mV

**Table 7. LVPECL Output,  $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$** 

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OD}$	Driver Differential Output voltage p-p	$V_{DD} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $R_L = 50\ \Omega$	1000	–	3600	mV
$V_{OC}$	Driver common-mode p-p	$V_{DD} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $R_L = 50\ \Omega$	–	–	300	mV
$t_R$	Rise Time	Differential 20% to 80%, $C_L = 10\ \text{pF}$ to GND, $R_L = 50\ \Omega$ to GND	300	–	1200	ps
$t_F$	Fall Time					
$V_{OH}$	Output High Voltage	$V_{DD} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OH} = -12\ \text{mA}$	2.1	–	3.0	V
$V_{OL}^{[2]}$	Output Low Voltage	$V_{DD} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	0.8	–	1.3	V
$I_{OS}$	Short Circuit Current	$V_{DD} = \text{Max}$ , $V_{OUT} = \text{GND}$	-125	–	-150	mA

## AC Switching Characteristics

**Table 8.  $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$** 

Parameter	Description	Conditions	Min	Typ	Max	Unit
$t_{PLH}$	Propagation Delay – Low to High	$V_{ID} = 100\ \text{mV}$	3	4	5	ns
$t_{PHL}$	Propagation Delay – High to Low	$V_{ID} = 100\ \text{mV}$	3	4	5	ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)		–	–	0.2	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ( $t_{PHL} - t_{PLH}$ )		–	0.2	–	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. Same input signal level and output load.	$V_{ID} = 100\ \text{mV}$	–	–	1	ns

**Table 9. High frequency Parametrics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
Fmax	Maximum frequency $V_{DD} = 3.3\ \text{V}$	45%–55% duty cycle Standard load circuit	–	–	350	MHz

**Note**

2.  $V_{OL}$  levels are dependent on the termination voltage  $V_{TT}$  and termination resistance  $R_{TT}$ . Changing either of these values will affect  $V_{OL}$ .

Figure 2. Driver Design

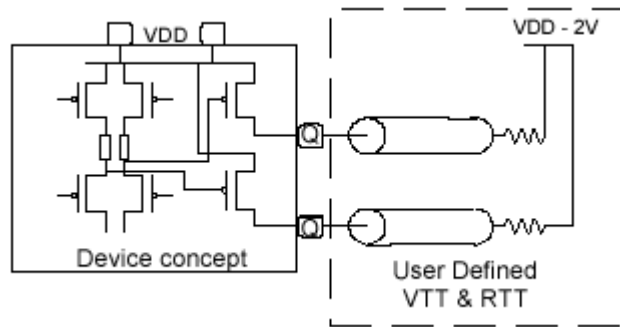


Figure 3. Standard Termination

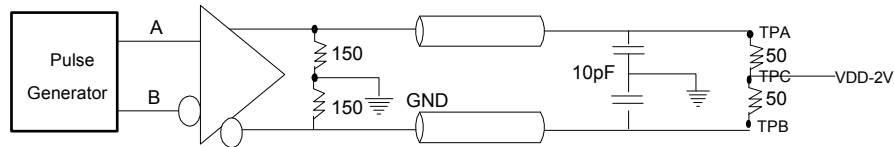


Figure 4. Differential Receiver to Driver Propagation Delay and Driver Transition Time [3, 4, 5, 6]

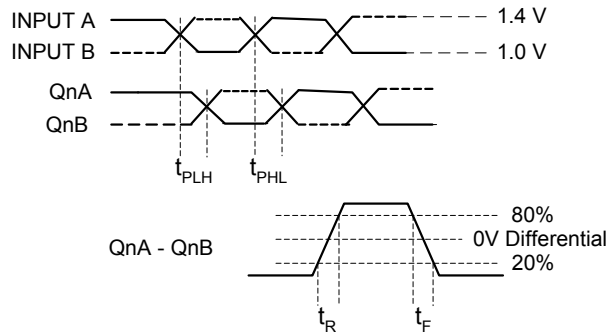
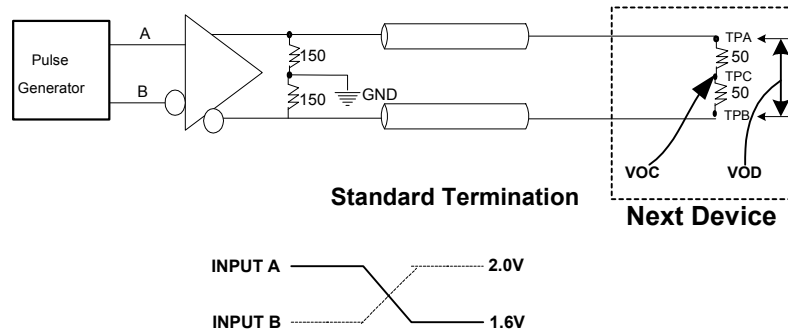


Figure 5. Test Circuit and Voltage Definitions for the Driver Common Mode Output Voltage [3, 4, 5, 6]



Notes

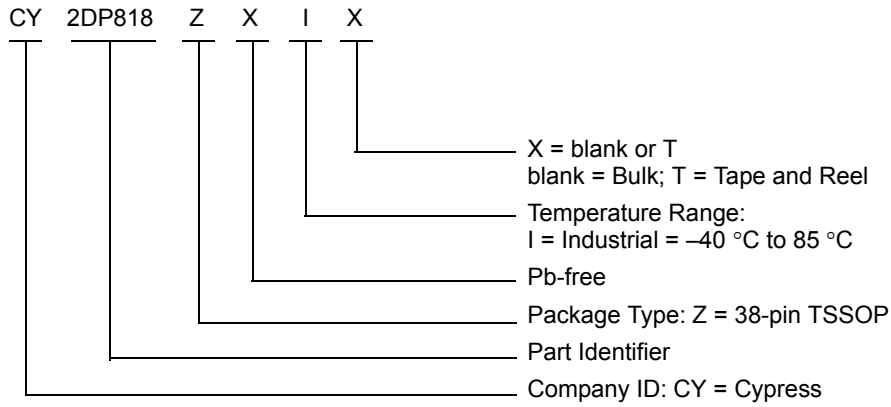
3. All input pulses are supplied by a frequency generator with the following characteristics:  $t_R$  and  $t_F \leq 1$  ns; pulse rerate = 50 Mpps; pulse width =  $10 \pm 0.2$  ns.
4.  $R_L = 50 \text{ ohm} \pm 1\%$ ;  $Z_{line} = 50 \text{ ohm} 6''$ .
5. CL includes instrumentation and fixture capacitance within 6 mm of the UT.
6. TPA and B are used for prop delay and Rise/Fall measurements. TPC is used for VOC measurements only and is otherwise connected to  $V_{DD} - 2V$ .



**Ordering Information**

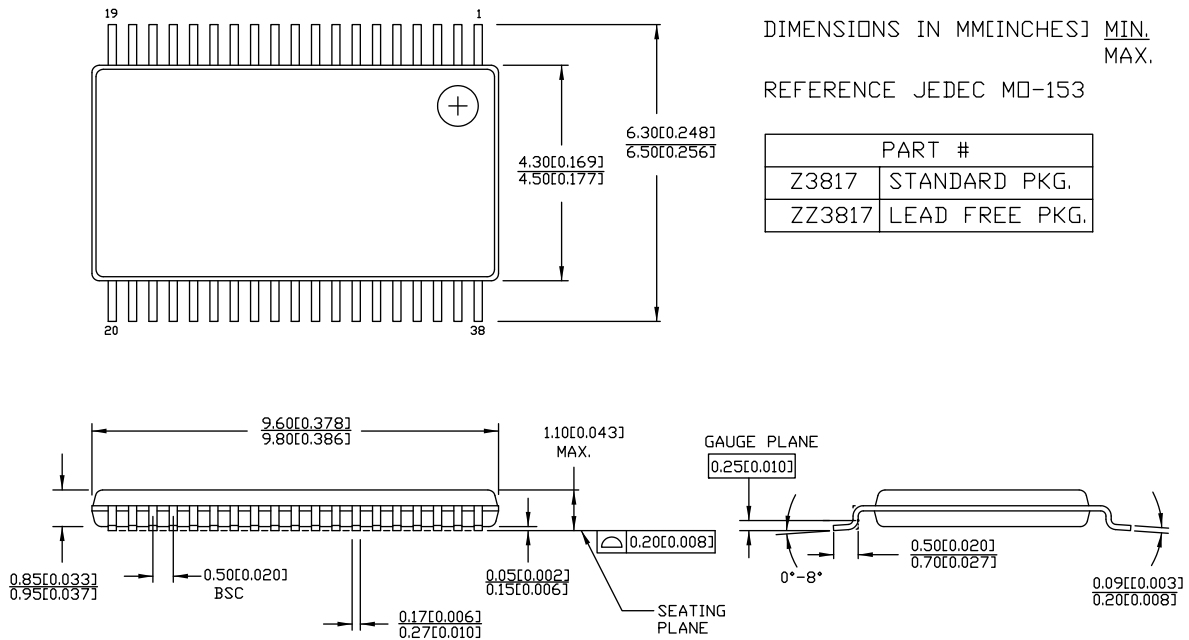
Part Number	Package Type	Product Flow
<b>Pb-free</b>		
CY2DP818ZXI	38-pin TSSOP	Industrial, -40 °C to 85 °C

**Ordering Code Definitions**



### Package Drawing and Dimensions

Figure 6. 38-pin TSSOP (9.7 × 4.4 × 1.1 mm) Z3817 / ZZ3817 Package Outline, 51-85151



51-85151 \*C

## Acronyms

Acronym	Description
LVC MOS	low-voltage complementary metal oxide semiconductor
LVDS	low-voltage differential signaling
LVPECL	low-voltage pseudo (positive) emitter-coupled logic
LVTTTL	low-voltage transistor-transistor logic
TSSOP	thin shrink small outline package

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2DP818, 1:8 Clock Fanout Buffer				
Document Number: 38-07061				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	107086	06/07/01	IKA	New Data Sheet
*A	115913	07/11/02	CTK	IC, VCM, VOC, Rise/Fall Time Fmax (20)
*B	2748606	08/05/09	KVM	Deleted references to ComLink Minor edits to page 1 text Instances of VCC changed to VDD Changed table sequence to be more logical Edited <a href="#">Table 1 on page 4</a> and reformatted <a href="#">Table 2 on page 4</a> for clarity Added voltage and temperature specs to heading of all DC and AC tables Added commercial temp range to DC and AC table headings Clarified wording for IC Core Removed duplicate I <sub>I</sub> (input high current) parameter from LVPECL & LVDS Removed T <sub>PE</sub> and T <sub>PD</sub> parameters from AC table Cleaned up waveform drawings Removed figures showing inputs for different InConfig values because <a href="#">Table 1 on page 4</a> and <a href="#">Table 2 on page 4</a> are more complete Updated <a href="#">Ordering Information</a> (Added part numbers CY2DP818ZXC, CY2DP818ZXCT, CY2DP818ZXI and CY2DP818ZXIT to the ordering information table). Updated <a href="#">Package Drawing and Dimensions</a> .
*C	2899846	KVM	03/26/10	Updated <a href="#">Ordering Information</a> (Removed inactive parts in ordering information table). Updated <a href="#">Package Drawing and Dimensions</a> .
*D	3717888	PURU	08/20/2012	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Drawing and Dimensions</a> (spec 51-85151 (Changed revision from *B to *C)). Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated in new template.
*E	3864478	PURU	01/16/2013	Updated <a href="#">Features</a> : Removed Commercial Temperature related information.  Updated <a href="#">DC Electrical Specifications</a> : Removed Commercial Temperature related information.  Updated <a href="#">Ordering Information</a> (Updated part numbers).

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