TEXAS INSTRUMENTS

CY74FCT163373

SCCS053 - March 1997 - Revised March 2000

16-Bit Latch

Features

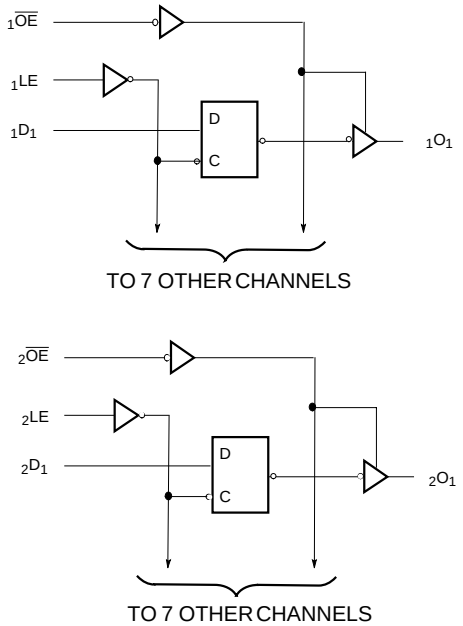
- **Low power, pin-compatible replacement for LCX and LPT families**
- **5V tolerant inputs and outputs**
- **24 mA balanced drive outputs**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for reduced noise**
- **FCT-C speed at 4.2 ns**
- **Latch-up performance exceeds JEDEC standard no. 17**
- **Typical output skew < 250 ps**
- **Industrial temperature range of –40˚C to +85˚C**
- **TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)**
- **Typical V_{olp} (ground bounce) performance exceeds Mil Std 883D**
- **V_{CC} = 2.7V to 3.6V**
- **ESD (HBM) > 2000V**

Functional Description

This device is a 16-bit, D-type latch, designed for use in bus applications requiring high speed and low power. It can either be used as two independent 8-bit latches, or as a single 16-bit latch by connecting the Output Enable ($\overline{OE}$) and Latch (LE) inputs. The outputs are 24-mA balanced output drivers with current limiting resistors to reduce the need for external terminating resistors and provide for minimal undershoot and reduced ground bounce. Flow-through pinout and small shrink packaging aid in simplifying board layout.

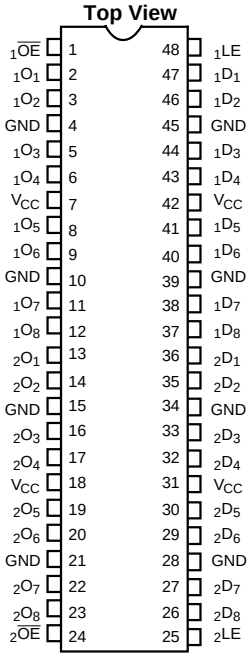
The CY74FCT163373 is designed with inputs and outputs capable of being driven by 5.0V buses, allowing its use in mixed voltage systems as a translator. The outputs are also designed with a power off disable feature enabling its use in applications requiring live insertion.

Logic Block Diagrams CY74FCT163373



Pin Configuration

SSOP/TSSOP
Top View



Pin Description

Name	Description
D	Data Inputs
LE	Latch Enable Inputs (Active HIGH)
$\overline{OE}$	Output Enable Inputs (Active LOW)
O	Three-State Outputs

Function Table[1]

Inputs			Outputs
D	**LE**	**$\overline{OE}$**	**O**
H	H	L	H
L	H	L	L
X	L	L	Q_0
X	X	H	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage Range ..... 0.5V to +4.6V

DC Input Voltage ..... –0.5V to +7.0V

DC Output Voltage ..... –0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... –60 to +120 mA

Power Dissipation 1.0W

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	2.7V to 3.6V

Electrical Characteristics for Non Bus Hold Devices Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description	Test Conditions		Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage	All Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Input Hysteresis[5]				100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA			–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=5.5				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND				±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=5.5V				±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=GND				±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=GND		–60	–135	–240	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V				±100	µA
I_{CC}	Quiescent Power Supply Current	V_{IN}≤0.2V, V_{IN}≥V_{CC}–0.2V	V_{CC}=Max.		0.1	10	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{IN}=V_{CC}–0.6V[7]	V_{CC}=Max.		2.0	30	µA

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance. Q_0=Previous state of flip-flop.
2. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. With the exception of inputs with bus hold, unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}=3.3V, T_A = +25˚C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. Per TTL driven input; all other inputs at V_{CC} or GND.

Electrical Characteristics For Balanced Drive Devices Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
I_{ODL}	Output LOW Dynamic Current[6]	V_{CC}=3.3V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	45		180	mA
I_{ODH}	Output HIGH Dynamic Current[6]	V_{CC}=3.3V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–45	–	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}= –0.1 mA	V_{CC}–0.2			V
		V_{CC}=Min., I_{OH}= –8 mA	2.4[8]	3.0		V
		V_{CC}=3.0V, I_{OH}= –24 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}= 0.1mA			0.2	V
		V_{CC}=Min., I_{OL}= 24 mA		0.3	0.55	

Note:
8. V_{OH}=V_{CC}–0.6 V at rated current.

Capacitance[5] (T_A = +25˚C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[4]	Max.	Unit
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	50	75	µA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	0.5	0.8	mA
			V_{IN}=V_{CC}–0.6V or V_{IN}=GND	0.5	0.8	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	2.0	3.0[11]	mA
			V_{IN}=V_{CC}–0.6V or V_{IN}=GND	2.0	3.3[11]	mA

Switching Characteristics Over the Operating Range V_{CC}=3.0V to 3.6V[12,13]

Parameter	Description	CY74FCT163373C		Unit	Fig. No.[14]
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Q Output	1.5	4.1	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LE to Q Output	2.0	5.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.2	ns	1, 7, 8
t_{SU}	Input Setup time	2.0	-	ns	1, 4
t_H	Input Hold time	1.5	-	ns	1, 4
$t_{SK(O)}$	Output Skew[15]		0.5	ns	—

Notes:

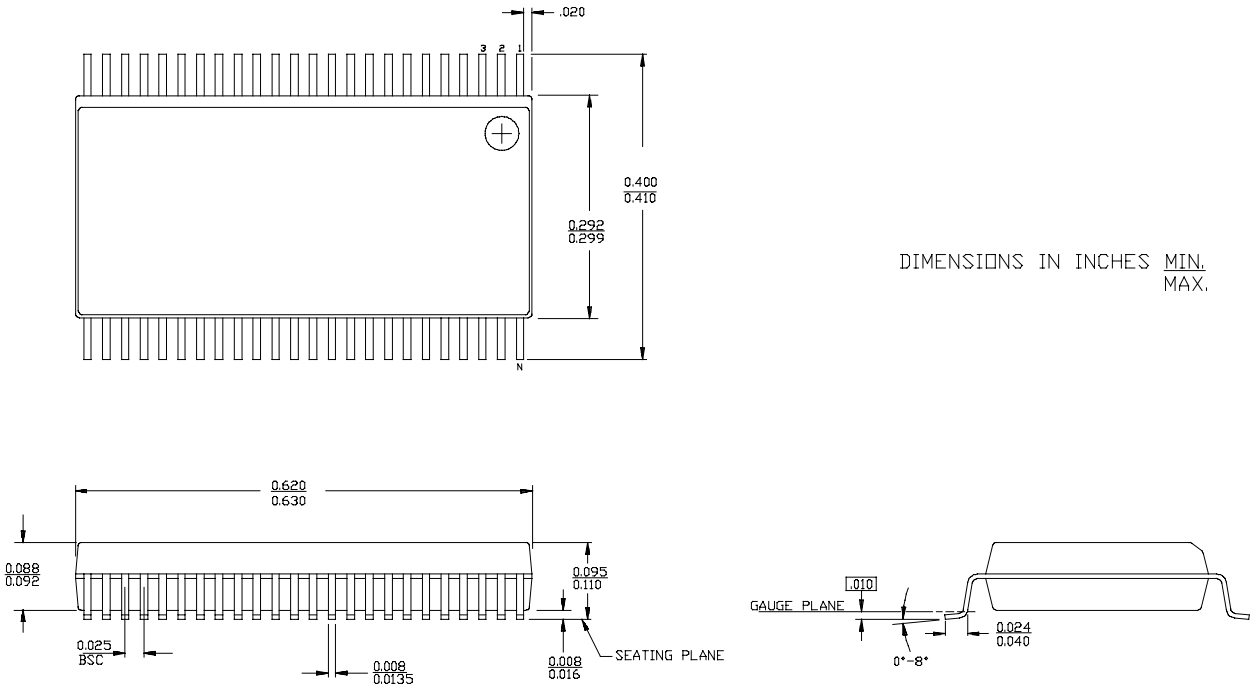
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.
12. Minimum limits are specified but not tested on Propagation Delays.
13. For V_{CC} =2.7, propagation delay, output enable and output disable times should be degraded by 20%.
14. See “Parameter Measurement Information” in the General Information section.
15. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT163373

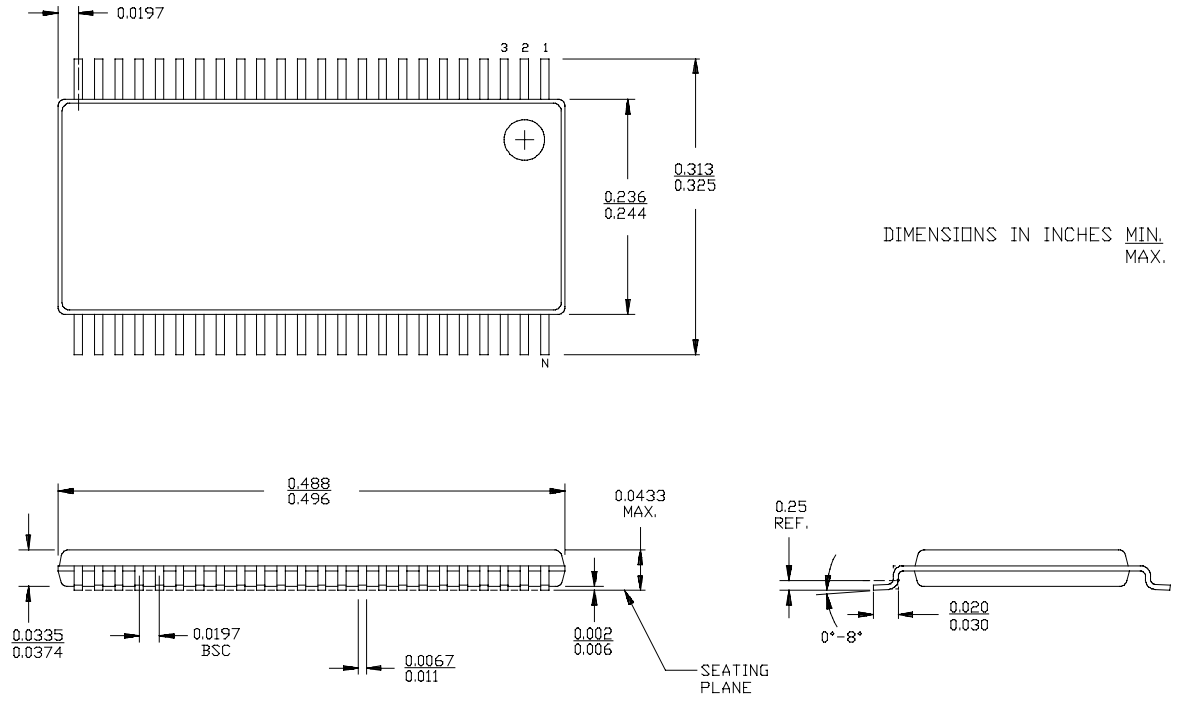
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT163373CPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163373CPVC/PVCT	O48	48-Lead (300-Mil) SSOP	

Package Diagrams

48-Lead Shrunk Small Outline Package O48



48-Lead Thin Shrunk Small Outline Package Z48



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CY74FCT163373CPAC	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI
CY74FCT163373CPACT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI
CY74FCT163373CPVC	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
CY74FCT163373CPVCT	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI

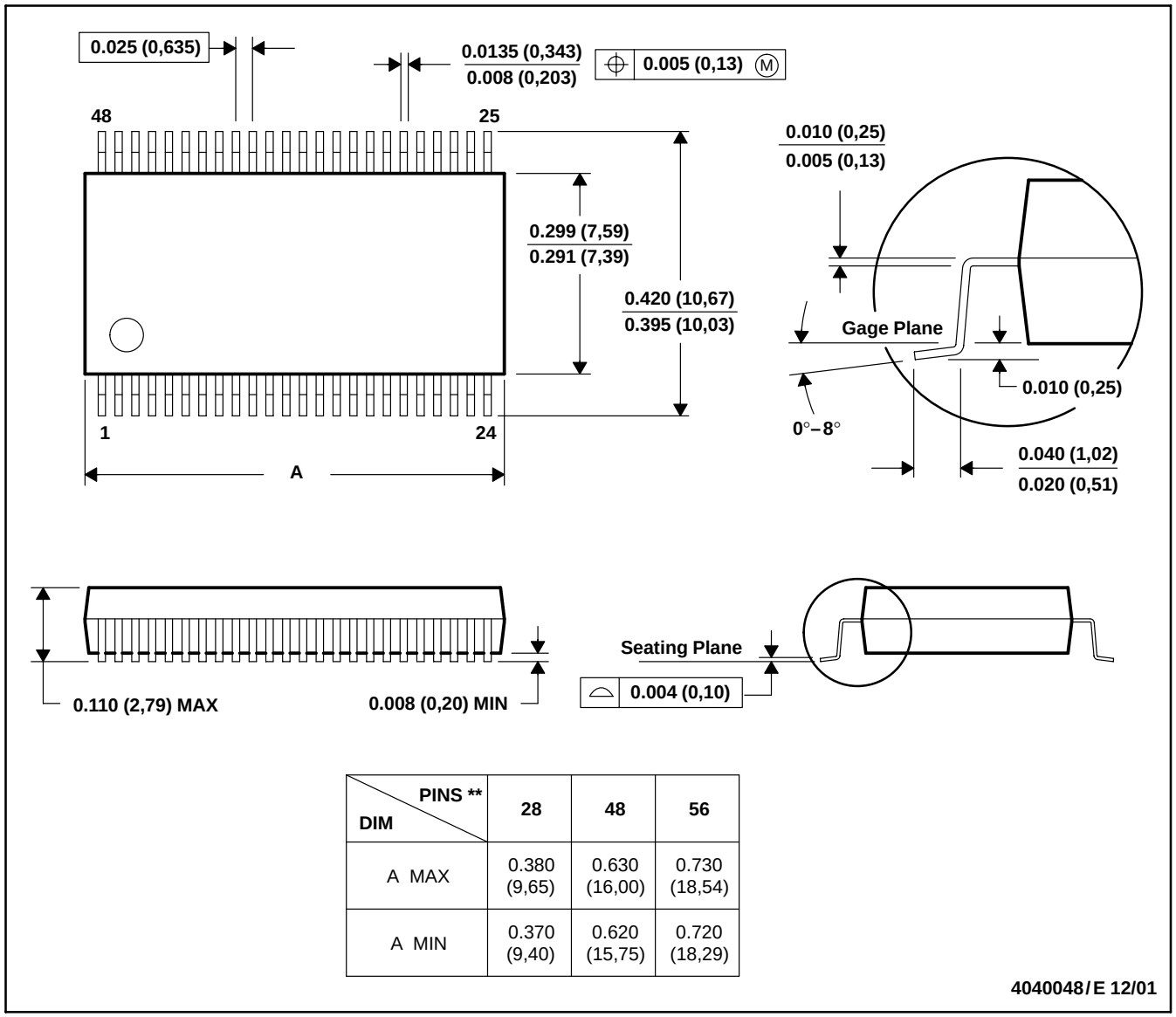
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



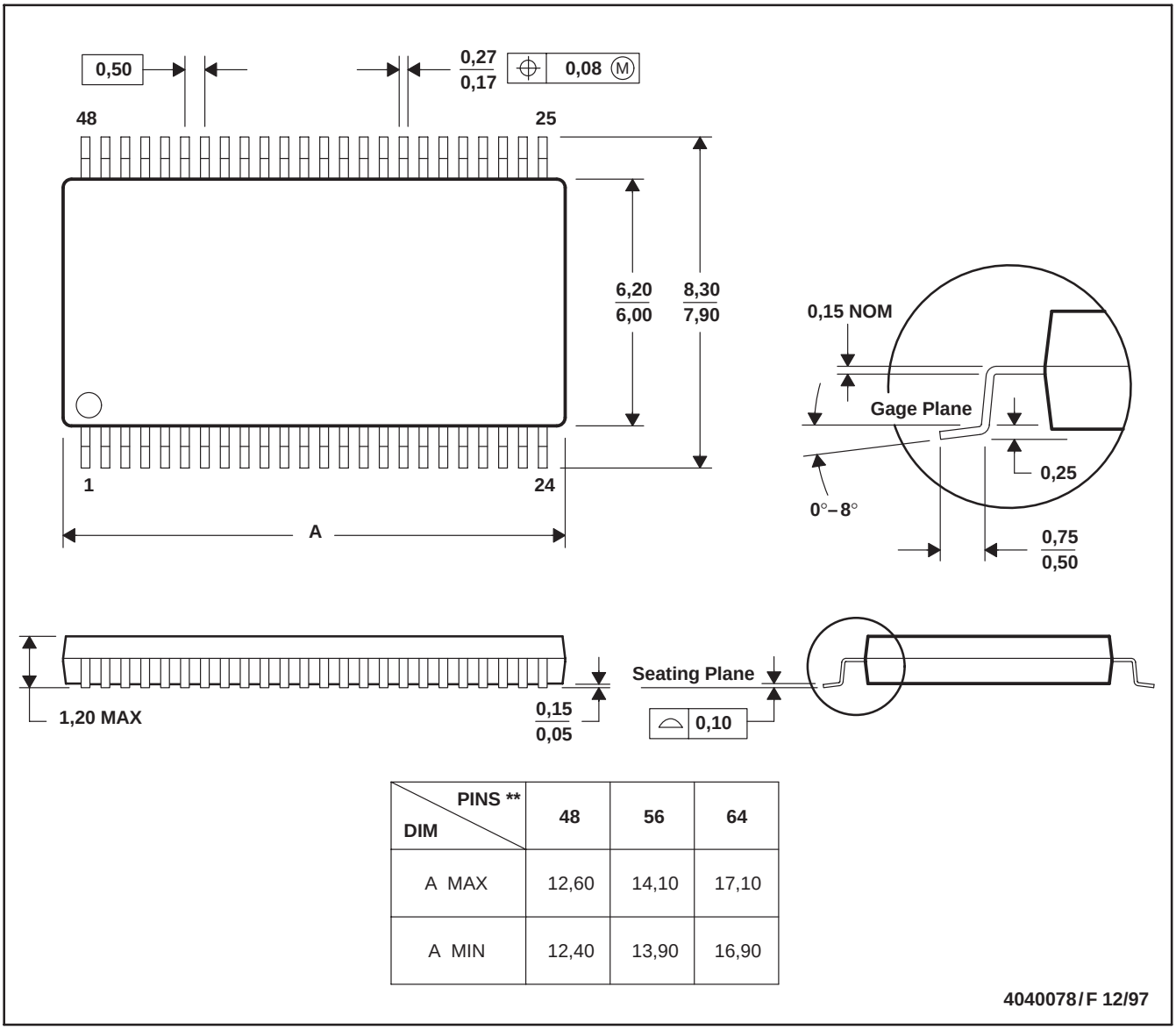
DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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