



CY54/74FCT257T

Quad 2-Input Multiplexer

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 4.3 ns max. (Com'I)
- FCT-A speed at 5.0 ns max. (Com'I)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

- Sink current 64 mA (Com'I), 32 mA (Mil)
- Source current 32 mA (Com'I), 12 mA (Mil)

Functional Description

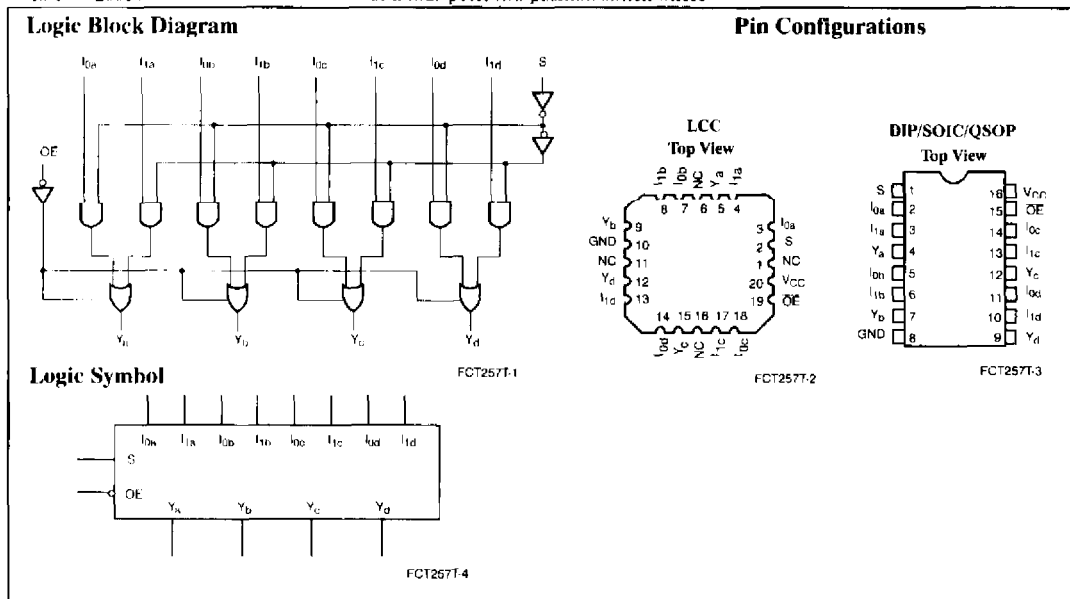
The FCT257T has four identical two-input multiplexers which select four bits of data from two sources under the control of a common data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the output in true non-inverted form for the FCT257T.

The FCT257T is a logic implementation of a four-pole, two position switch where

the position of the switch is determined by the logic levels supplied to the select input. Outputs are forced to a high-impedence "OFF" state when the Output Enable input (OE) is HIGH.

All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of three-state devices are tied together.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.



Pin Description

Name	Description
I	Data Inputs
S	Common Select Input
OE	Enable Inputs (Active LOW)
Y	Data Outputs

Function Table^[1]

Inputs				Output
OE	S	I ₀	I ₁	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Note:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = High impedance (OFF) state



Switching Characteristics Over the Operating Range

Parameter	Description	FCT257T				FCT257AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay 1 to Y	1.5	7.0	1.5	6.0	1.5	5.8	1.5	5.0	ns	1, 3
t _{PLS} t _{PHS}	Propagation Delay S to O	1.5	12.0	1.5	10.5	1.5	8.1	1.5	7.0	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	10.0	1.5	8.5	1.5	8.0	1.5	7.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	8.0	1.5	6.0	1.5	5.8	1.5	5.5	ns	1, 7, 8

Parameter	Description	FCT257CT				Unit	Fig. No. ^[13]
		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay 1 to Y	1.5	5.0	1.5	4.3	ns	1, 3
t _{PLS} t _{PHS}	Propagation Delay S to O _n	1.5	6.0	1.5	5.2	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	6.8	1.5	6.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.3	1.5	5.0	ns	1, 7, 8

Notes:

- 12. Minimum limits are guaranteed but not tested on Propagation Delays.
- 13. See "Parameter Measurement Information" in the General Information Section.



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT257CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT257CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT257CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.0	CY54FCT257CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT257CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.0	CY74FCT257ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT257ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT257ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.8	CY54FCT257ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT257ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.0	CY74FCT257TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT257TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT257TSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.0	CY54FCT257TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT257TLMB	L61	20-Pin Square Leadless Chip Carrier	

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