CY7B923, CY7B933

HOTLink® Transmitter/Receiver

Features

- Fibre Channel-compliant
- IBM ESCON®-compliant
- DVB-ASI-compliant
- ATM-compliant
- 8B/10B-coded or 10-bit unencoded
- Standard HOTLink®: 160 to 330 Mbps
- High-speed HOTLink: 160 to 400 Mbps for high-speed applications
- Transistor-transistor logic (TTL)-synchronous I/O
- No external phase locked-loop (PLL) components
- Triple positive emitter coupled logic (PECL) 100 K serial outputs
- Dual PECL 100 K serial inputs
- Low-power: 350 mW (Tx), 650 mW (Rx)
- Compatible with fiber-optic modules, coaxial cable, and twisted pair media
- Built-in self-test (BIST)
- Single +5-V supply
- 28-pin small outline integrated circuit (SOIC)/plastic leaded chip carrier (PLCC)
- Pb-free packages available
- 0.8-µ bipolar complementary metal oxide semiconductor (BiCMOS)

Functional Description

The CY7B923 HOTLink, transmitter and CY7B933 HOTLink receiver are point-to-point communications building blocks that transfer data over high-speed serial links (fiber, coax, and twisted pair). Standard HOTLink data rates range from 160 to 330 Mbps. Higher speed HOTLink is also available for high-speed applications (160 to 400 Mbits/second). Figure 1 illustrates typical connections to host systems or controllers.

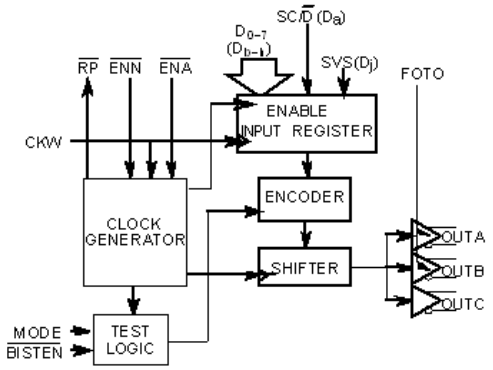
Eight bits of user data or protocol information are loaded into the HOTLink transmitter and are encoded. Serial data is shifted out of the three differential PECL serial ports at the bit rate (which is ten times the byte rate).

The HOTLink receiver accepts the serial bit stream at its differential line receiver inputs and, using a completely integrated PLL clock synchronizer, recovers the timing information necessary for data reconstruction. The bit stream is deserialized, decoded, and checked for transmission errors. Recovered bytes are presented in parallel to the receiving host along with a byte-rate clock.

The 8B/10B encoder/decoder can be disabled in systems that already encode or scramble the transmitted data. I/O signals are available to create a seamless interface with both asynchronous FIFOs (that is, CY7C42X) and clocked FIFOs (that is, CY7C44X). A BIST pattern generator and checker allows testing of the transmitter, receiver, and the connecting link as a part of a system diagnostic check.

HOTLink devices are ideal for a variety of applications where a parallel interface can be replaced with a high-speed point-to-point serial link. Applications include interconnecting workstations, servers, mass storage, and video transmission equipment.

CY7B923 Transmitter Block Diagram



CY7B933 Receiver Block Diagram

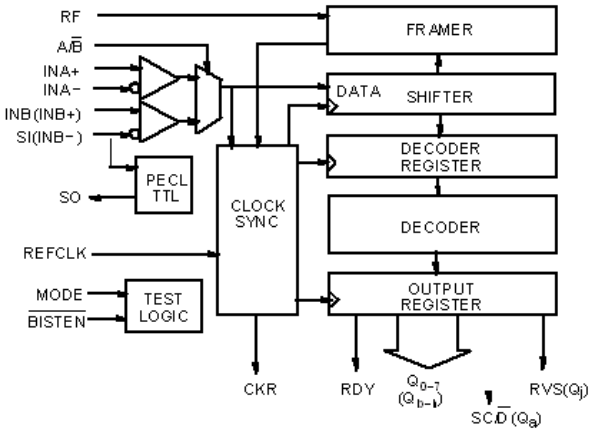
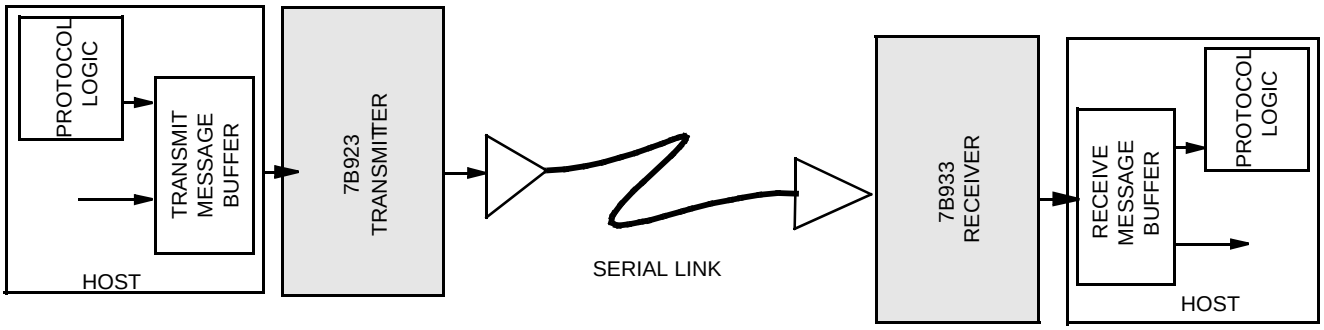


Figure 1. HOTLink System Connections



Contents

Pin Configurations

Figure 2. CY7B923 Transmitter Pin Configurations

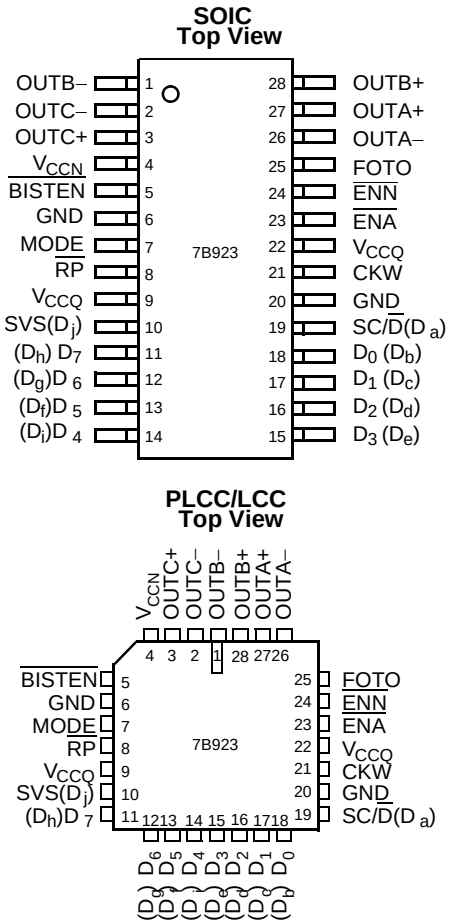
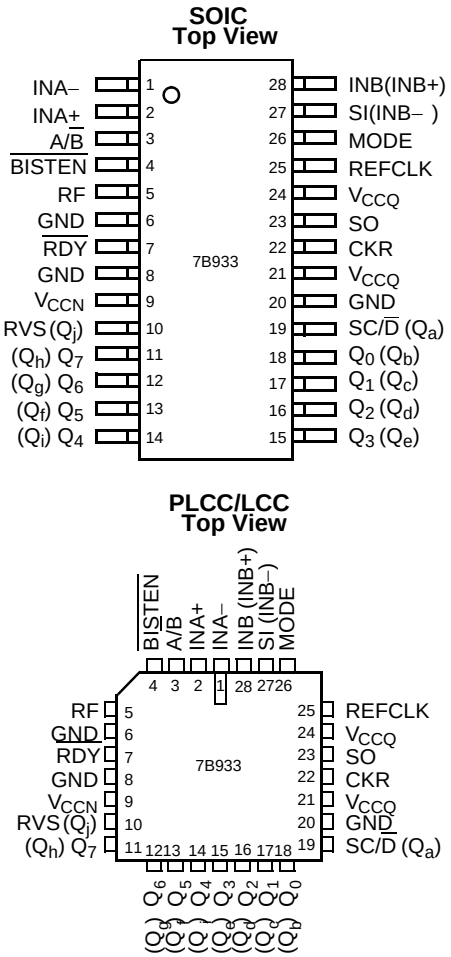


Figure 3. CY7B933 Receiver Pin Configurations



Pin Descriptions

Table 1. CY7B923 HOTLink Transmitter

Name	I/O	Description
D_{0-7} (D_{b-h})	TTL In	Parallel data input. Data is clocked into the Transmitter on the rising edge of CKW if ENA is LOW (or on the next rising CKW with ENN LOW). If ENA and ENN are HIGH, a Null character (K28.5) is sent. When MODE is HIGH, $D_{0, 1, ...7}$ become $D_{b, c,...h}$, respectively.
SC/D (D_a)	TTL In	Special character/data select. A HIGH on SC/D when CKW rises causes the transmitter to encode the pattern on D_{0-7} as a control code (Special Character), while a LOW causes the data to be coded using the 8B/10B data alphabet. When MODE is HIGH, SC/D (D_a) acts as D_a input. SC/D has the same timing as D_{0-7}.
SVS (D_j)	TTL In	Send violation symbol. If SVS is HIGH when CKW rises, a Violation symbol is encoded and sent while the data on the parallel inputs is ignored. If SVS is LOW, the state of D_{0-7} and SC/D determines the code sent. In normal or test mode, this pin overrides the BIST generator and forces the transmission of a Violation code. When MODE is HIGH (placing the transmitter in unencoded mode), SVS (D_j) acts as the D_j input. SVS has the same timing as D_{0-7}.
ENA	TTL In	Enable parallel data. If ENA is LOW on the rising edge of CKW, the data is loaded, encoded, and sent. If ENA and ENN are HIGH, the data inputs are ignored and the Transmitter will insert a Null character (K28.5) to fill the space between user data. ENA may be held HIGH/LOW continuously or it may be pulsed with each data byte to be sent. If ENA is being used for data control, ENN will normally be strapped HIGH, but can be used for BIST function control.
ENN	TTL In	Enable next parallel data. If ENN is LOW, the data appearing on D_{0-7} at the next rising edge of CKW is loaded, encoded, and sent. If ENA and ENN are HIGH, the data appearing on D_{0-7} at the next rising edge of CKW will be ignored and the Transmitter will insert a Null character to fill the space between user data. ENN may be held HIGH/LOW continuously or it may be pulsed with each data byte sent. If ENN is being used for data control, ENA will normally be strapped HIGH, but can be used for BIST function control.
CKW	TTL In	Clock write. CKW is both the clock frequency reference for the multiplying PLL that generates the high-speed transmit clock, and the byte rate write signal that synchronizes the parallel data input. CKW must be connected to a crystal controlled time base that runs within the specified frequency range of the Transmitter and Receiver.
FOTO	TTL In	Fiber optic transmitter off. FOTO determines the function of two of the three PECL transmitter output pairs. If FOTO is LOW, the data encoded by the Transmitter will appear at the outputs continuously. If FOTO is HIGH, OUTA± and OUTB± are forced to their "logic zero" state (OUT+ = LOW and OUT− = HIGH), causing a fiber-optic transmit module to extinguish its light output. OUTC is unaffected by the level on FOTO, and can be used as a loop-back signal source for board-level diagnostic testing.
OUTA± OUTB± OUTC±	PECL Out	Differential serial data outputs. These PECL 100 K outputs (+5 V referenced) are capable of driving terminated transmission lines or commercial fiber optic transmitter modules. Unused pairs of outputs can be left open, or wired to V_{CC} to reduce power, if the output is not required. OUTA± and OUTB± are controlled by the level on FOTO, and will remain at their "logical zero" states when FOTO is asserted. OUTC± is unaffected by the level on FOTO. (OUTA+ and OUTB+ are used as a differential test clock input while in Test mode, that is, MODE = UNCONNECTED or forced to $V_{CC}/2$).
MODE	Three-Level In	Encoder mode select. The level on MODE determines the encoding method to be used. When wired to GND, MODE selects 8B/10B encoding. When wired to V_{CC}, data inputs bypass the encoder and the bit pattern on D_{a-j} goes directly to the shifter. When left floating (internal resistors hold the input at $V_{CC}/2$) the internal bit-clock generator is disabled and OUTA+/OUTB+ become the differential bit clock to be used for factory test. In typical applications MODE is wired to V_{CC} or GND.
BISTEN	TTL In	BIST enable. When BISTEN is LOW and ENA and ENN are HIGH, the transmitter sends an alternating 1–0 pattern (D10.2 or D21.5). When either ENA or ENN is set LOW and BISTEN is LOW, the transmitter begins a repeating test sequence that allows the Transmitter and Receiver to work together to test the function of the entire link. In normal use this input is held HIGH or wired to V_{CC}. The BIST generator is a free-running pattern generator that need not be initialized, but if required, the BIST sequence can be initialized by momentarily asserting SVS while BISTEN is LOW. BISTEN has the same timing as D_{0-7}.
RP	TTL Out	Read pulse. RP is a 60% LOW duty-cycle byte-rate pulse train suitable for the read pulse in CY7C42X FIFOs. The frequency on RP is the same as CKW when enabled by ENA, and duty cycle is independent of the CKW duty cycle. Pulse widths are set by logic internal to the transmitter. In BIST mode, RP will remain HIGH for all but the last byte of a test loop. RP will pulse LOW one byte time per BIST loop.
V_{CCN}		Power for output drivers.
V_{CCQ}		Power for internal circuitry.
GND		Ground.

Table 2. CY7B933 HOTLink Receiver

Name	I/O	Description
$Q_{0–7}$ (Q_{b-h})	TTL Out	$Q_{0–7}$ parallel data output. $Q_{0–7}$ contain the most recently received data. These outputs change synchronously with CKR. When MODE is HIGH, $Q_{0, 1, ...7}$ become $Q_{b, c,...h}$, respectively.
SC/$\overline{D}$ (Q_a)	TTL Out	Special character/data select. SC/$\overline{D}$ indicates the context of received data. HIGH indicates a Control (Special Character) code, LOW indicates a Data character. When MODE is HIGH (placing the receiver in Unencoded mode), SC/$\overline{D}$ acts as the Q_a output. SC/$\overline{D}$ has the same timing as $Q_{0–7}$.
RVS (Q_j)	TTL Out	Received violation symbol. A HIGH on RVS indicates that a code rule violation has been detected in the received data stream. A LOW shows that no error has been detected. In BIST mode, a LOW on RVS indicates correct operation of the Transmitter, Receiver, and link on a byte-by-byte basis. When MODE is HIGH (placing the receiver in Unencoded mode), RVS acts as the Q_j output. RVS has the same timing as $Q_{0–7}$.
$\overline{RDY}$	TTL Out	Data output ready. A LOW pulse on $\overline{RDY}$ indicates that new data has been received and is ready to be delivered. A missing pulse on $\overline{RDY}$ shows that the received data is the Null character (normally inserted by the transmitter as a pad between data inputs). In BIST mode $\overline{RDY}$ will remain LOW for all but the last byte of a test loop and will pulse HIGH one byte time per BIST loop.
CKR	TTL Out	Clock read. This byte rate clock output is phase and frequency aligned to the incoming serial data stream. $\overline{RDY}$, $Q_{0–7}$, SC/$\overline{D}$, and RVS all switch synchronously with the rising edge of this output.
A/$\overline{B}$	PECL in	Serial data input select. This PECL 100K (+5V referenced) input selects INA or INB as the active data input. If A/$\overline{B}$ is HIGH, INA is connected to the shifter and signals connected to INA will be decoded. If A/$\overline{B}$ is LOW INB is selected.
INA±	Diff In	Serial data input A. The differential signal at the receiver end of the communication link may be connected to the differential input pairs INA± or INB±. Either the INA pair or the INB pair can be used as the main data input and the other can be used as a loopback channel or as an alternative data input selected by the state of A/$\overline{B}$. One input of an intentionally unused differential-pair (INA± or INB±) should be terminated to V_{CC} through a 1–5-KΩ resistor to assure that no data transitions are accidentally created.
INB (INB+)	PECL in (Diff In)	Serial data input B. This pin is either a single-ended PECL data receiver (INB) or half of the INB differential pair. If SO is wired to V_{CC}, then INB± can be used as differential line receiver interchangeably with INA±. If SO is normally connected and loaded, INB becomes a single-ended PECL 100K (+5 V referenced) serial data input. INB is used as the test clock while in Test mode.
SI (INB–)	PECL in (Diff In)	Status input. This pin is either a single-ended PECL status monitor input (SI) or half of the INB differential pair. If SO is wired to V_{CC}, then INB± can be used as differential line receiver interchangeably with INA±. If SO is normally connected and loaded, SI becomes a single-ended PECL 100K (+5V referenced) status monitor input, which is translated into a TTL-level signal at the SO pin.
SO	TTL Out	Status out. SO is the TTL-translated output of SI. It is typically used to translate the carrier detect output from a fiber-optic receiver connected to SI. When this pin is normally connected and loaded (without any external pull-up resistor), SO will assume the same logical level as SI and INB will become a single-ended PECL serial data input. If the status monitor translation is not desired, then SO may be wired to V_{CC} and the INB± pair may be used as a differential serial data input.
RF	TTL In	Reframe enable. RF controls the Framer logic in the Receiver. When RF is held HIGH, each SYNC (K28.5) symbol detected in the shifter will frame the data that follows. If it is HIGH for 2,048 consecutive bytes, the internal framer switches to double-byte mode. When RF is held LOW, the reframing logic is disabled. The incoming data stream is then continuously deserialized and decoded using byte boundaries set by the internal byte counter. Bit errors in the data stream will not cause alias SYNC characters to reframe the data erroneously.
REFCLK	TTL In	Reference clock. REFCLK is the clock frequency reference for the clock/data synchronizing PLL. REFCLK sets the approximate center frequency for the internal PLL to track the incoming bit stream. REFCLK must be connected to a crystal-controlled time base that runs within the frequency limits of the Tx/Rx pair, and the frequency must be the same as the transmitter CKW frequency (within CKW ± 0.1%).
MODE	Three-Level In	Decoder mode select. The level on the MODE pin determines the decoding method to be used. When wired to GND, MODE selects 8B/10B decoding. When wired to V_{CC}, registered shifter contents bypass the decoder and are sent to $Q_{a–j}$ directly. When left floating (internal resistors hold the MODE pin at $V_{CC}/2$) the internal bit clock generator is disabled and INB becomes the bit rate test clock to be used for factory test. In typical applications, MODE is wired to V_{CC} or GND.

Table 2. CY7B933 HOTLink Receiver (continued)

Name	I/O	Description
$\overline{\text{BISTEN}}$	TTL In	Built-in self-test enable. When $\overline{\text{BISTEN}}$ is LOW the Receiver awaits a D0.0 (sent once per BIST loop) character and begins a continuous test sequence that tests the functionality of the Transmitter, the Receiver, and the link connecting them. In BIST mode the status of the test can be monitored with RDY and RVS outputs. In normal use BISTEN is held HIGH or wired to V_{CC}. BISTEN has the same timing as $Q_{0–7}$.
V_{CCN}		Power for output drivers.
V_{CCQ}		Power for internal circuitry.
GND		Ground.

CY7B923 HOTLink Transmitter Block Diagram Description

Input Register

The input register holds the data to be processed by the HOTLink transmitter and allows the input timing to be made consistent with standard FIFOs. The input register is clocked by CKW and loaded with information on the D_{0-7}, SC/$\overline{D}$, and SVS pins. Two enable inputs (ENA and $\overline{\text{ENN}}$) allow the user to choose when data is loaded in the register. Asserting Enable, active LOW (ENA) causes the inputs to be loaded in the register on the rising edge of CKW. If $\overline{\text{ENN}}$ (Enable Next, active LOW) is asserted when CKW rises, the data present on the inputs on the next rising edge of CKW are loaded into the Input register. If neither ENA nor $\overline{\text{ENN}}$ are asserted LOW on the rising edge of CKW, then a SYNC (K28.5) character is sent. These two inputs allow proper timing and function for compatibility with either asynchronous FIFOs or clocked FIFOs without external logic, as shown in Figure 6.

In BIST mode, the input register becomes the signature pattern generator by logically converting the parallel input register into a linear feedback shift register (LFSR). When enabled, this LFSR generates a 511-byte sequence that includes all data and special character codes, including the explicit violation symbols. This pattern provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the receiver.

Encoder

The encoder transforms the input data held by the input register into a form more suitable for transmission on a serial interface link. The code used is specified by ANSI X3.230 (Fibre Channel) and the IBM ESCON channel (see the table Valid Data Characters (SC/D = LOW) on page 21). The eight $D_{0–7}$ data inputs are converted to either a data symbol or a special character, depending upon the state of the SC/$\overline{D}$ input. If SC/$\overline{D}$ is HIGH, the data inputs represent a control code and are encoded using the special character code table. If SC/$\overline{D}$ is LOW, the data inputs are converted using the data code table. If a byte time passes with the inputs disabled, the encoder outputs a special character comma K28.5 (or SYNC) that maintains link synchronization. SVS input forces the transmission of a specified violation symbol to allow the user to check the error handling system logic in the controller or for proprietary applications.

The 8B/10B coding function of the encoder can be bypassed for systems that include an external coder or scrambler function as part of the controller. This bypass is controlled by setting the MODE select pin HIGH. When in bypass mode, D_{a-j} (note that the bit order is specified in the fibre channel 8B/10B code) become the ten inputs to the shifter, with D_a being the first bit to be shifted out.

Shifter

The shifter accepts parallel data from the encoder after each byte time and shifts it to the serial interface output buffers using a PLL multiplied bit clock that runs at 10 times the byte clock rate. Timing for the parallel transfer is controlled by the counter included in the clock generator and is not affected by signal levels or timing at the input pins.

OutA, OutB, OutC

The serial interface PECL output buffers (ECL100K referenced to +5 V) are the drivers for the serial media. They are all connected to the shifter and contain the same serial data. Two of the output pairs (OUTA± and OUTB±) are controllable by the FOTO input and can be disabled by the system controller to force a logical zero (that is, “light off”) at the outputs. The third output pair (OUTC±) is not affected by FOTO and supplies a continuous data stream suitable for loopback testing of the subsystem.

OUTA± and OUTB± responds to FOTO input changes within a few bit times. However, since FOTO is not synchronized with the transmitter data stream, the outputs will be forced off or turned on at arbitrary points in a transmitted byte. This function is intended to augment an external laser safety controller and as an aid for Receiver PLL testing.

In wire-based systems, control of the outputs may not be required, and FOTO can be strapped LOW. The three outputs are intended to add system and architectural flexibility by offering identical serial bit streams with separate interfaces for redundant connections or for multiple destinations. Unneeded outputs can be wired to VCC to disable and power down the unused output circuitry.

Clock Generator

The clock generator is an embedded PLL that takes a byte-rate reference clock (CKW) and multiplies it by 10 to create a bit rate clock for driving the serial shifter. The byte rate reference comes from CKW, the rising edge of which clocks data into the input register. This clock must be a crystal referenced pulse stream that has a frequency between the minimum and maximum specified for the HOTLink transmitter/receiver pair. Signals controlled by this block form the bit clock and the timing signals that control internal data transfers between the input register and the shifter.

The read pulse ($\overline{RP}$) is derived from the feedback counter used in the PLL multiplier. It is a byte-rate pulse stream with the proper phase and pulse widths to allow transfer of data from an asynchronous FIFO. Pulse width is independent of CKW duty cycle, since proper phase and duty cycle is maintained by the PLL. The $\overline{RP}$ pulse stream ensures correct data transfers between asynchronous FIFOs and the transmitter input latch with no external logic.

Test Logic

Test logic includes the initialization and control for the BIST generator, the multiplexer for test mode clock distribution, and control logic to properly select the data encoding. Test logic is discussed in detail in CY7B923 HOTLink Transmitter Operating Mode Description on page 11.

CY7B933 HOTLink Receiver Block Diagram Description

Serial Data Inputs

Two pairs of differential line receivers are the inputs for the serial data stream. INA± or INB± can be selected with the A/B input. INA± is selected with A/B HIGH and INB± is selected with A/B LOW. The threshold of A/B is compatible with the ECL 100K signals from PECL fiber optic interface modules. TTL logic elements can be used to select the A or B inputs by adding a resistor pull-up to the TTL driver connected to A/B. The differential threshold of INA± and INB± will accommodate wire interconnect with filtering losses or transmission line attenuation greater than 20 db ($V_{DIF} \geq 50$ mv) or can be directly connected to fiber optic interface modules (any ECL logic family, not limited to ECL 100K). The common mode tolerance will accommodate a wide range of signal termination voltages. The highest HIGH input that can be tolerated is $V_{IN} = V_{CC}$, and the lowest LOW input that can be interpreted correctly is V_{IN} = GND+2.0V.

PECL-TTL Translator

The function of the INB(INB+) input and the SI(INB–) input is defined by the connections on the SO output pin. If the PECL/TTL translator function is not required, the SO output is wired to VCC. A sensor circuit detects this connection and causes the inputs to become INB± (a differential line-receiver serial-data input). If the PECL/TTL translator function is required, the SO output is connected to its normal TTL load (typically one or more TTL inputs, but no pull-up resistor) and the INB+ input becomes single-ended ECL 100K, serial data input (INB) and the INB– input becomes single-ended, ECL 100K status input (SI).

This positive-referenced PECL-to-TTL translator is provided to eliminate external logic between an PECL fiber-optic interface module “carrier detect” output and the TTL input in the control logic. The input threshold is compatible with ECL 100K levels (+5-V referenced). It can also be used as part of the link status indication logic for wire connected systems.

Clock Synchronization

The clock synchronization function is performed by an embedded PLL that tracks the frequency of the incoming bit stream and aligns the phase of its internal bit rate clock to the serial data transitions. This block contains the logic to transfer the data from the shifter to the decode register once every byte. The counter that controls this transfer is initialized by the framer logic. CKR is a buffered output derived from the bit counter used to control the decode register and the output register transfers.

Clock output logic is designed so that when reframing causes the counter sequence to be interrupted, the period and pulse width of CKR is never less than normal. Reframing may stretch the period of CKR by up to 90%, and either CKR Pulse Width HIGH or Pulse Width LOW may be stretched, depending on when reframe occurs.

The REFCLK input provides a byte-rate reference frequency to improve PLL acquisition time and limit unlocked frequency excursions of the CKR when no data is present at the serial inputs. The frequency of REFCLK is required to be within ±0.1% of the frequency of the clock that drives the transmitter CKW pin.

Framer

Framer logic checks the incoming bit stream for the pattern that defines the byte boundaries. This combinatorial logic filter looks for the X3.230 symbol defined as a Special Character Comma (K28.5). When it is found, the free-running bit counter in the Clock Synchronization block is synchronously reset to its initial state, thus framing the data correctly on the correct byte boundaries.

Random errors that occur in the serial data can corrupt some data patterns into a bit pattern identical to a K28.5, and thus cause an erroneous data-framing error. The RF input prevents this by inhibiting reframing during times when normal message data is present. When RF is held LOW, the HOTLink receiver will deserialize the incoming data without trying to reframe the data to incoming patterns. When RF rises, $\overline{RDY}$ will be inhibited until a K28.5 has been detected, after which $\overline{RDY}$ will resume its normal function. While RF is HIGH, it is possible that an error could cause misframing, after which all data will be corrupted. Likewise, a K28.7 followed by D11.x, D20.x, or an SVS (C0.7) followed by D11.x will create alias K28.5 characters and cause erroneous framing. These sequences must be avoided while RF is HIGH.

If RF remains HIGH for greater than 2048 bytes, the framer converts to double-byte framing, requiring two K28.5 characters aligned on the same byte boundary within 5 bytes in order to reframe. Double-byte framing greatly reduces the possibility of erroneously reframing to an aliased K28.5 character.

Shifter

The shifter accepts serial inputs from the serial data inputs one bit at a time, as clocked by the clock synchronization logic. Data is transferred to the framer on each bit, and to the decode register once per byte.

Decode Register

The decode register accepts data from the shifter once per byte as determined by the logic in the clock synchronization block. It is presented to the decoder and held until it is transferred to the output latch.

Decoder

Parallel data is transformed from ANSI-specified X3.230 8B/10B codes back to 'raw data' in the decoder. This block uses the standard decoder patterns shown in Valid Data Characters (SC/D = LOW) on page 21 and Valid Special Character Codes and Sequences (SC/D = HIGH)[1, 2] on page 29. Data patterns are signaled by a LOW on the SC/D output and special character patterns are signaled by a HIGH on the SC/D output. Unused patterns or disparity errors are signaled as errors by a HIGH on the RVS output and by specific special character codes.

Output Register

The output register holds the recovered data (Q_{0-7}, SC/D, and RVS) and aligns it with the recovered byte clock (CKR). This synchronization insures proper timing to match a FIFO interface or other logic that requires glitch-free and specified output behavior. Outputs change synchronously with the rising edge of CKR.

In BIST mode, this register becomes the signature pattern generator and checker by logically converting itself into a linear feedback shift register (LFSR) pattern generator. When enabled, this LFSR generates a 511-byte sequence that includes all data and special character codes, including the explicit violation symbols. This pattern provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Transmitter. When synchronized, it checks each byte in the Decoder with each byte generated by the LFSR and shows errors at RVS. Patterns generated by the LFSR are compared after being buffered to the output pins and then fed back to the comparators, allowing test of the entire receive function.

In BIST mode, the LFSR is initialized by the first occurrence of the transmitter BIST loop start code D0.0 (D0.0 is sent only once per BIST loop). Once the BIST loop has been started, RVS will be HIGH for pattern mismatches between the received sequence and the internally generated sequence. Code rule violations or running disparity errors that occur as part of the BIST loop will not cause an error indication. RDY will pulse HIGH once per BIST loop and can be used to check test pattern progress. The receiver BIST generator can be reinitialized by leaving and re-entering BIST mode.

Test Logic

Test logic includes the initialization and control for the Built-In Self-Test (BIST) generator, the multiplexer for Test mode clock distribution, and control logic for the decoder. Test logic is discussed in more detail in the CY7B933 HOTLink Receiver Operating Mode Description.

HOTLink CY7B923 Transmitter and CY7B933 Receiver Operation

The CY7B923 Transmitter operating with the CY7B933 Receiver form a general purpose data communications subsystem capable of transporting user data at up to 33 Mbytes per second (40 Mbytes per second for –400 devices) over several types of serial interface media. Figure 10 on page 33 illustrates the flow of data through the HOTLink CY7B923 transmitter pipeline. Data is latched into the transmitter on the rising edge of CKW when enabled by ENA or ENN. RP is asserted LOW with a 60% LOW/40% HIGH duty cycle when ENA is LOW. RP may be used as a read strobe for accessing data stored in a FIFO. The parallel data flows through the encoder and is then shifted out of the OUTx± PECL drivers. The bit-rate clock is generated internally from a multiply-by-ten PLL clock generator. The latency through the transmitter is approximately $21t_B$ – 10 ns over the operating range. A more complete description is found in the section CY7B923 HOTLink Transmitter Operating Mode Description.

Figure 5 illustrates the data flow through the HOTLink CY7B933 receiver pipeline. Serial data is sampled by the receiver on the INx± inputs. The receiver PLL locks onto the serial bit stream and generates an internal bit rate clock. The bit stream is deserialized, decoded and then presented at the parallel output pins. A byte rate clock (bit clock ÷ 10) synchronous with the parallel data is presented at the CKR pin. The RDY pin will be asserted to LOW to indicate that data or control characters are present on the outputs. RDY will not be asserted LOW in a field of K28.5s except for any single K28.5 or the last one in a continuous series of K28.5's. The latency through the receiver is approximately $24t_B$ + 10 ns over the operating range. A more complete description of the receiver is in the section CY7B933 HOTLink Receiver Operating Mode Description.

The HOTLink receiver has a built-in byte framer that synchronizes the Receiver pipeline with incoming SYNC (K28.5) characters. Figure illustrates the HOTLink CY7B933 Receiver framing operation. The Framer is enabled when the RF pin is asserted HIGH. RF is latched into the receiver on the falling edge of CKR. The framer looks for K28.5 characters embedded in the serial data stream. When a K28.5 is found, the framer sets the parallel byte boundary for subsequent data to the K28.5 boundary. While the framer is enabled, the RDY pin indicates the status of the framing operation.

When the RF pin is asserted HIGH, RDY leaves it normal mode of operation and is asserted HIGH while the framer searches the data stream for a K28.5 character. After the framer has synchronized to a K28.5 character, the Receiver will assert the RDY pin LOW when the K28.5 character is present at the parallel output. The RDY pin will then resume its normal operation as dictated by the MODE and BISTEN pins.

The normal operation of the RDY pin in encoded mode is to signal when parallel data is present at the output pins by pulsing LOW with a 60% LOW/40% HIGH duty cycle. RDY does not pulse LOW in a field of K28.5 characters; however, RDY does pulse LOW for the last K28.5 character in the field or for any single K28.5. In unencoded mode, the normal operation of the RDY pin is to signal when any K28.5 is at the parallel output pins.

Figure 4. CY7B933 Receiver Data Pipeline in Encoded Mode

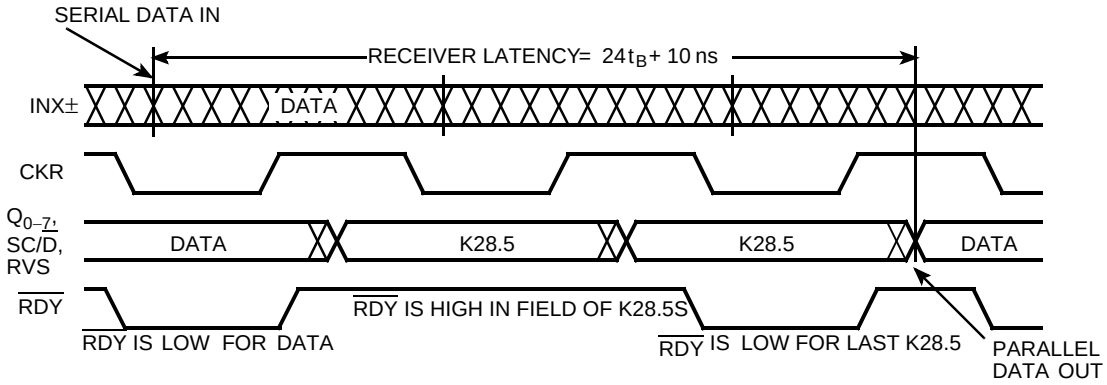
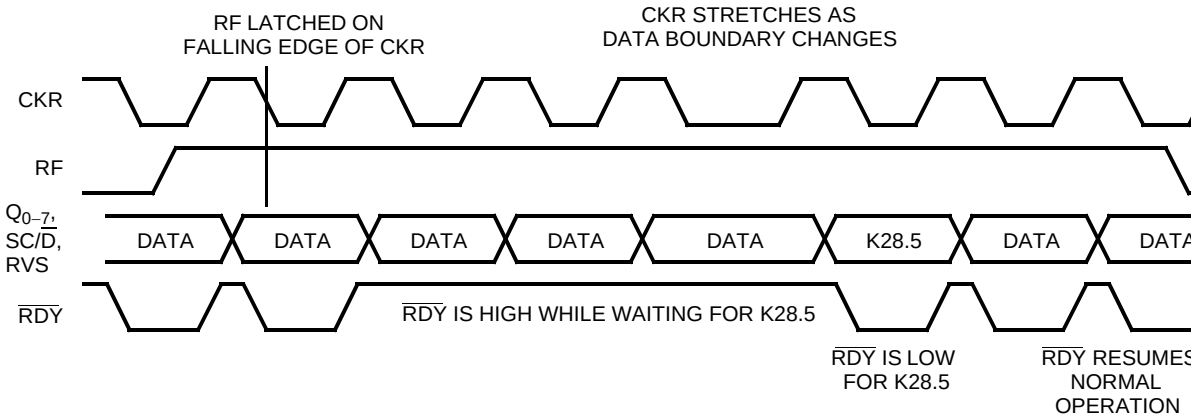


Figure 5. CY7B933 Framing Operation in Encoded Mode



The transmitter and receiver parallel interface timing and functionality can be made to match the timing and functionality of either an asynchronous FIFO or a clocked FIFO by appropriately connecting signals (see Figure 6 on page 12). Proper operation of the FIFO interface depends upon various FIFO-specific access and response specifications.

The HOTLink transmitter and receiver serial interface provides a seamless interface to various types of media. A minimal number of external components are needed to properly terminate transmission lines and provide PECL loads. For proper power supply decoupling, a single 0.01 µF for each device is all that is required to bypass the V_{CC} and GND pins. Figure 7 on page 14 illustrates a HOTLink transmitter and receiver interface to fiber-optic and copper media. More information on interfacing HOTLink to various media can be found in the *HOTLink Design Considerations* application note.

CY7B923 HOTLink Transmitter Operating Mode Description

In normal operation, the transmitter can operate in either of two modes. The encoded mode allows a user to send and receive eight-bit data and control information without first converting it to transmission characters. The bypass mode is used for systems in which the encoding and decoding is performed in an external protocol controller.

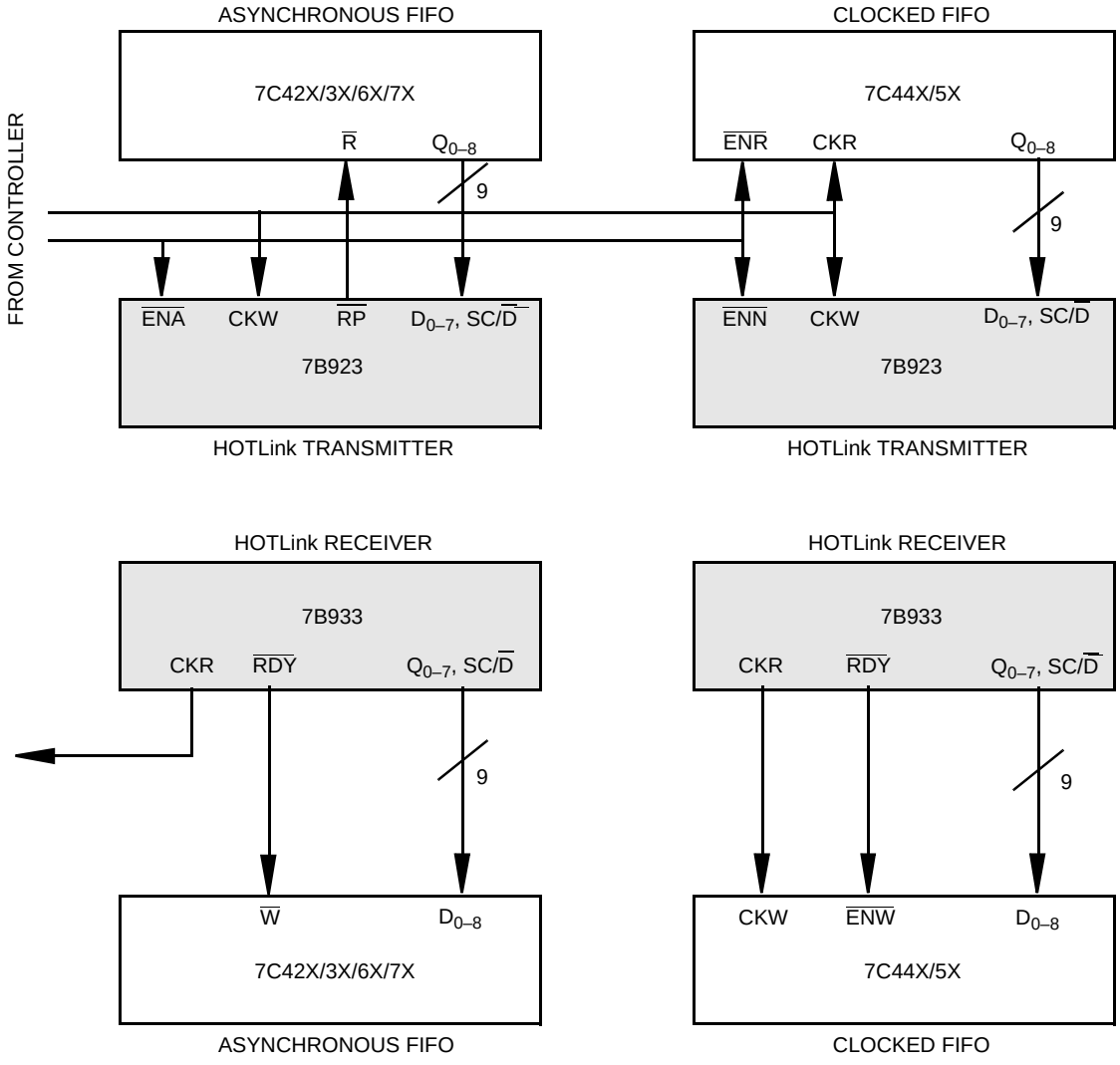
In either mode, data is loaded into the Input register of the Transmitter on the rising edge of CKW. The input timing and functional response of the Transmitter input can be made to match the timing and functionality of either an asynchronous FIFO or a clocked FIFO by an appropriate connection of input signals (see Figure 6 on page 12). Proper operation of the FIFO interface depends upon various FIFO-specific access and response specifications.

Encoded Mode Operation

In the encoded mode, the input data is interpreted as eight bits of data (D_0–D_7), a context control bit (SC/$\overline{D}$), and a system diagnostic input bit (SVS). If the context of the data is to be normal message data, the SC/$\overline{D}$ input should be LOW, and the data should be encoded using the valid data character set described in Valid Data Characters (SC/D = LOW) on page 21. If the context of the data is to be control or protocol information, the SC/$\overline{D}$ input is HIGH, and the data is encoded using the valid special character set described in Valid Special Character Codes and Sequences (SC/D = HIGH)[1, 2] on page 29. Special characters include all protocol characters necessary to encode packets for Fibre Channel, ESCON, proprietary systems, and diagnostic purposes.

The diagnostic characters and sequences available as special characters include those for Fibre Channel link testing, as well as codes to be used for testing system response to link errors and timing. A Violation symbol can be explicitly sent as part of a user data packet (i.e., send C0.7; D_{7-0} = 111 00000 and SC/$\overline{D}$ = 1), or it can be sent in response to an external system using the SVS input. This allows the system diagnostic logic to evaluate the errors in an unambiguous manner, and does not require any modification to the transmission interface to force transmission errors for testing purposes.

Figure 6. Seamless FIFO Interface



Bypass Mode Operation

In the bypass mode, the input data is interpreted as 10 bits ($D_{b–h}$), SC/$\overline{D}$ (D_a), and SVS (D_j) of pre-encoded transmission data to be serialized and sent over the link. This data can use any encoding method suitable to the designer. The only restrictions upon the data encoding method is that it contain suitable transition density for the receiver PLL data synchronizer (one per 10-bit byte), and that it be compatible with the transmission media.

Data loaded into the Input register on the rising edge of CKW is loaded into the shifter on the subsequent rising edges of CKW. It will then be shifted to the outputs one bit at a time using the internal clock generated by the clock generator. The first bit of the transmission character (D_a) appears at the output (OUTA±, OUTB±, and OUTC±) after the next CKW edge.

While in either the encoded mode or bypass mode, if a CKW edge arrives when the inputs are not enabled ($\overline{ENA}$ and $\overline{ENN}$ both HIGH), the encoder inserts a pad character K28.5 (for example, C5.0) to maintain proper link synchronization (in the bypass mode the proper sense of running disparity cannot be guaranteed for the first pad character, but is correct for all pad characters that follow). This automatic insertion of pad characters can be inhibited by insuring that the transmitter is always enabled (that is, $\overline{ENA}$ or $\overline{ENN}$ is hard-wired LOW).

PECL Output Functional and Connection Options

The three pairs of PECL outputs all contain the same information and are intended for use in systems with multiple connections. Each output pair may be connected to a different serial media, each of which may be a different length, link type, or interface technology. For systems that do not require all three output pairs, the unused pairs should be wired to V_{CC} to minimize the power dissipated by the output circuit, and to minimize unwanted noise generation. An internal voltage comparator detects when an output differential pair is wired to V_{CC}, causing the current source for that pair to be disabled. This results in a power savings of around 5 mA for each unused pair.

In systems that require the outputs to be shut off during some periods when link transmission is prohibited (for example, for laser safety functions), the FOTO input can be asserted. While it is possible to insure that the output state of the PECL drivers is LOW (that is, light is off) by sending all 0s in bypass mode, it is often inconvenient to insert this level of control into the data transmission channel, and it is impossible in encoded mode. FOTO is provided to simplify and augment this control function (typically found in laser-based transmission systems). FOTO will force OUTA+ and OUTB+ to go LOW, OUTA– and OUTB– to go HIGH, while allowing OUTC± to continue to function normally (OUTC is typically used as a diagnostic feedback and cannot be disabled). This separation of function allows various system configurations without undue load on the control function or data channel logic.

Transmitter Serial Data Characteristics

The CY7B923 HOTLink transmitter serial output conforms to the requirements of the Fibre Channel specification. The serial data output is controlled by an internal PLL that multiplies the frequency of CKW by 10 to maintain the proper bit clock frequency. The jitter characteristics (including both PLL and logic components) are as follows:

- Deterministic Jitter (D_j) < 35 ps (peak-peak). Typically measured while sending a continuous K28.5 (C5.0).
- Random Jitter (R_j) < 175 ps (peak-peak). Typically measured while sending a continuous K28.7 (C7.0).

Transmitter Test Mode Description

The CY7B923 transmitter offers two types of test mode operation, BIST mode and Test mode. In a normal system application, the BIST mode can be used to check the functionality of the transmitter, the receiver, and the link connecting them. This mode is available with minimal impact on user system logic, and can be used as part of the normal system diagnostics. Typical connections and timing are shown in Figure 8 on page 15.