



## 2K x 16 Dual-Port Static RAM

### Features

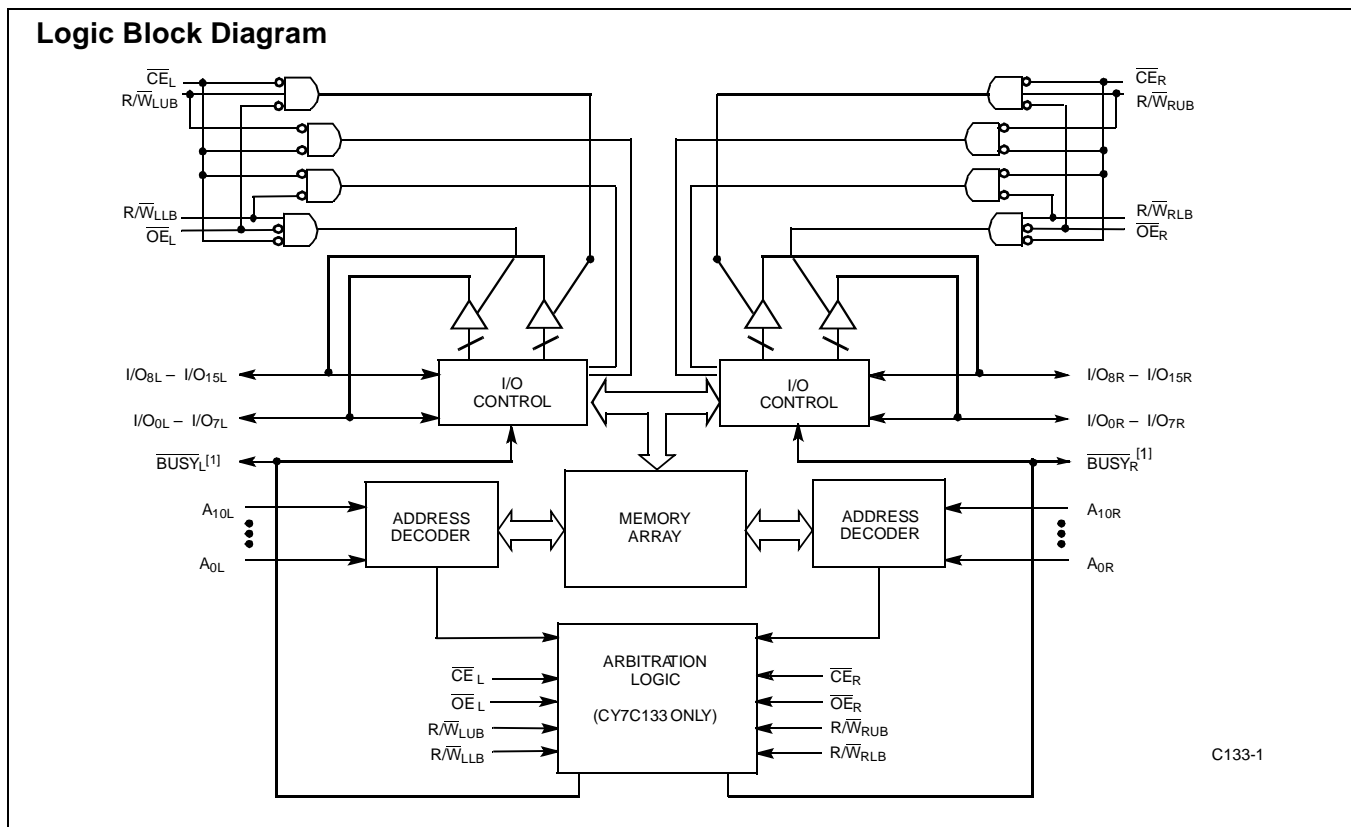
- True dual-ported memory cells which allow simultaneous reads of the same memory location
- 2K x 16 organization
- 0.65-micron CMOS for optimum speed/power
- High-speed access: 25/35/55 ns
- Low operating power:  $I_{CC} = 150 \text{ mA (typ.)}$
- Fully asynchronous operation
- Master CY7C133 expands data bus width to 32 bits or more using slave CY7C143
- BUSY input flag on CY7C133; BUSY output flag on CY7C143
- Available in 68-pin PLCC
- Pin-compatible and functionally equivalent to IDT7133 and IDT7143

### Functional Description

The CY7C133 and CY7C143 are high-speed CMOS 2K by 16 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C133 can be utilized as either a stand-alone 16-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C143 slave dual-port device in systems requiring 32-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

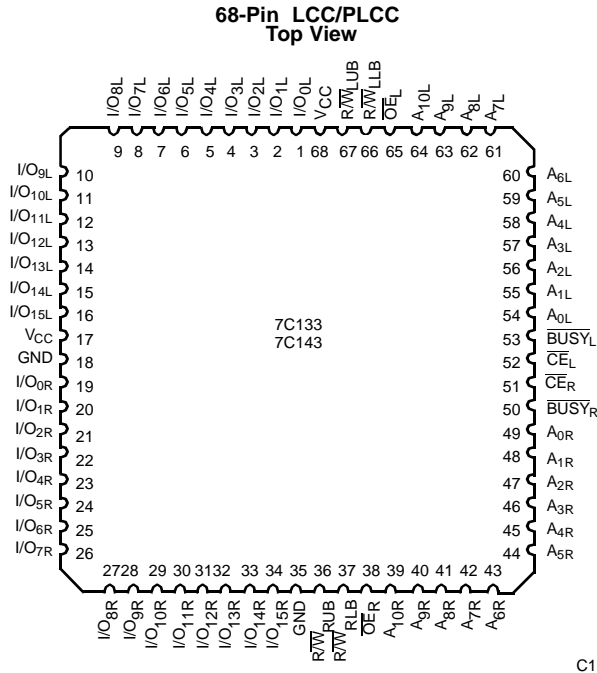
Each port has independent control pins; Chip Enable ( $\overline{CE}$ ), Write Enable ( $R/\overline{W}_{UB}$ ,  $R/\overline{W}_{LB}$ ), and Output Enable ( $\overline{OE}$ ). BUSY signals that the port is trying to access the same location currently being accessed by the other port. An automatic power-down feature is controlled independently on each port by the Chip Enable ( $\overline{CE}$ ) pin.

The CY7C133 and CY7C143 are available in 68-pin PLCC.



**Note:**

1. CY7C133 (Master):  $\overline{BUSY}$  is open drain output and requires pull-up resistor. CY7C143 (Slave):  $\overline{BUSY}$  is input.

**Pin Configuration**


C133-2

**Selection Guide**

|  | <b>7C133-25<br/>7C143-25</b> | <b>7C133-35<br/>7C143-35</b> | <b>7C133-55<br/>7C143-55</b> |
|--|------------------------------|------------------------------|------------------------------|
| Maximum Access Time (ns)                   | 25                           | 35                           | 55                           |
| Typical Operating Current $I_{CC}$ (mA)    | 170                          | 160                          | 150                          |
| Typical Standby Current for $I_{SB1}$ (mA) | 40                           | 30                           | 20                           |

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential  
(Pin 48 to Pin 24) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs  
in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

**Operating Range**

| <b>Range</b> | <b>Ambient<br/>Temperature</b> | <b>V<sub>CC</sub></b> |
|--------------|--------------------------------|-----------------------|
| Commercial   | 0°C to +70°C                   | 5V ± 10%              |
| Industrial   | -40°C to +85°C                 | 5V ± 10%              |

**Electrical Characteristics** Over the Operating Range

| Parameter        | Description                                   | Test Conditions  | 7C133-25<br>7C143-25 |      |      | Unit |    |
|------------------|---|--|----------------------|------|------|------|----|
|                  |   |  | Min.                 | Typ. | Max. |      |    |
| V <sub>OH</sub>  | Output HIGH Voltage                           | V <sub>CC</sub> = Min.,<br>I <sub>OH</sub> = -4.0 mA   | 2.4                  |      |      | V    |    |
| V <sub>OL</sub>  | Output LOW Voltage                            | I <sub>OL</sub> = 4.0 mA   |                      |      | 0.4  | V    |    |
|                  |   | I <sub>OL</sub> = 16.0 mA <sup>[2]</sup>   |                      |      | 0.5  |      |    |
| V <sub>IH</sub>  | Input HIGH Voltage                            |  | 2.2                  |      |      | V    |    |
| V <sub>IL</sub>  | Input LOW Voltage                             |  |                      |      | 0.8  | V    |    |
| I <sub>IX</sub>  | Input Leakage Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -5                   |      | +5   | μA   |    |
| I <sub>OZ</sub>  | Output Leakage Current                        | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -5                   |      | +5   | μA   |    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[3,4]</sup> | V <sub>CC</sub> = Max.,<br>V <sub>OUT</sub> = GND  |                      |      | -200 | mA   |    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current      | $\overline{CE} = V_{IL}$ ,<br>Outputs Open,<br>f = f <sub>MAX</sub> <sup>[5]</sup>   | Com'l                |      | 170  | 250  | mA |
|                  |   |  | Ind.                 |      | 170  | 290  |    |
| I <sub>SB1</sub> | Standby Current Both Ports, TTL Inputs        | $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ , f = f <sub>MAX</sub> <sup>[5]</sup>  | Com'l                |      | 40   | 60   | mA |
|                  |   |  | Ind.                 |      | 40   | 75   |    |
| I <sub>SB2</sub> | Standby Current One Port, TTL Inputs          | $\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ , Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[5]</sup>   | Com'l                |      | 100  | 140  | mA |
|                  |   |  | Ind.                 |      | 100  | 160  |    |
| I <sub>SB3</sub> | Standby Current Both Ports, CMOS Inputs       | Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0  | Com'l                |      | 3    | 15   | mA |
|                  |   |  | Ind.                 |      | 3    | 15   |    |
| I <sub>SB4</sub> | Standby Current One Port, CMOS Inputs         | One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[5]</sup> | Com'l                |      | 90   | 120  | mA |
|                  |   |  | Ind.                 |      | 90   | 140  |    |

**Notes:**

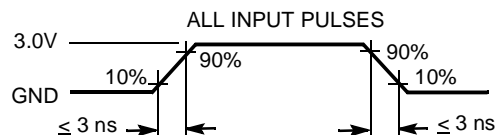
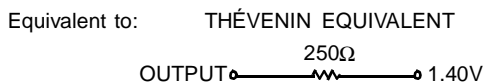
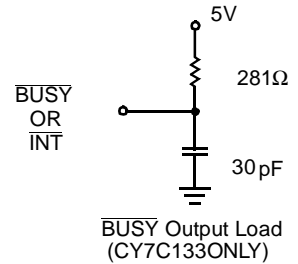
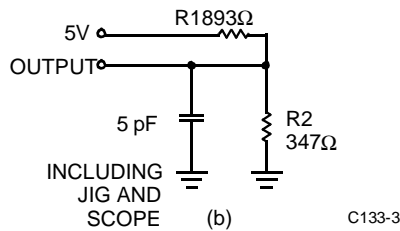
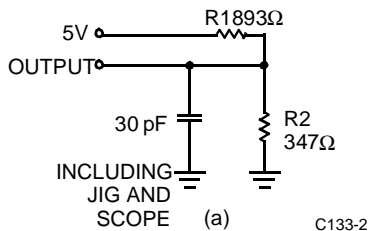
2.  $\overline{BUSY}$  pin only.
3. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.
5. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency of read cycle of 1/t<sub>RC</sub> and using AC Test Waveforms input levels of GND to 3V.

**Electrical Characteristics** Over the Operating Range (continued)

| Parameter        | Description                                   | Test Conditions  | 7C133-35<br>7C143-35 |      |      | 7C133-55<br>7C143-55 |      |      | Unit |    |
|------------------|---|--|----------------------|------|------|----------------------|------|------|------|----|
|                  |   |  | Min.                 | Typ. | Max. | Min.                 | Typ. | Max. |      |    |
| V <sub>OH</sub>  | Output HIGH Voltage                           | V <sub>CC</sub> = Min.,<br>I <sub>OH</sub> = -4.0 mA   | 2.4                  |      |      | 2.4                  |      |      | V    |    |
| V <sub>OL</sub>  | Output LOW Voltage                            | I <sub>OL</sub> = 4.0 mA   |                      |      | 0.4  |                      |      | 0.4  | V    |    |
|                  |   | I <sub>OL</sub> = 16.0 mA <sup>[2]</sup>   |                      |      | 0.5  |                      |      | 0.5  |      |    |
| V <sub>IH</sub>  | Input HIGH Voltage                            |  | 2.2                  |      |      | 2.2                  |      |      | V    |    |
| V <sub>IL</sub>  | Input LOW Voltage                             |  |                      |      | 0.8  |                      |      | 0.8  | V    |    |
| I <sub>Ix</sub>  | Input Leakage Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -5                   |      | +5   | -5                   |      | +5   | μA   |    |
| I <sub>OZ</sub>  | Output Leakage Current                        | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -5                   |      | +5   | -5                   |      | +5   | μA   |    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[3,4]</sup> | V <sub>CC</sub> = Max.,<br>V <sub>OUT</sub> = GND  |                      |      | -200 |                      |      | -200 | mA   |    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current      | $\overline{CE} = V_{IL}$ ,<br>Outputs Open,<br>f = f <sub>MAX</sub> <sup>[5]</sup>   | Com'l                |      | 160  | 230                  |      | 150  | 220  | mA |
|                  |   |  | Ind.                 |      | 160  | 260                  |      | 150  | 250  |    |
| I <sub>SB1</sub> | Standby Current Both Ports, TTL Inputs        | $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ , f = f <sub>MAX</sub> <sup>[5]</sup>  | Com'l                |      | 30   | 50                   |      | 20   | 40   | mA |
|                  |   |  | Ind.                 |      | 30   | 65                   |      | 20   | 55   |    |
| I <sub>SB2</sub> | Standby Current One Port, TTL Inputs          | $\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ , Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[5]</sup>   | Com'l                |      | 85   | 125                  |      | 75   | 110  | mA |
|                  |   |  | Ind.                 |      | 85   | 140                  |      | 75   | 125  |    |
| I <sub>SB3</sub> | Standby Current Both Ports, CMOS Inputs       | Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0  | Com'l                |      | 3    | 15                   |      | 3    | 15   | mA |
|                  |   |  | Ind.                 |      | 3    | 15                   |      | 3    | 15   |    |
| I <sub>SB4</sub> | Standby Current One Port, CMOS Inputs         | One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[5]</sup> | Com'l                |      | 80   | 105                  |      | 70   | 90   | mA |
|                  |   |  | Ind.                 |      | 80   | 120                  |      | 70   | 105  |    |

**Capacitance<sup>[4]</sup>**

| Parameter        | Description        | Test Conditions  | Max. | Unit |
|------------------|--------------------|--|------|------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 10   | pF   |
| C <sub>OUT</sub> | Output Capacitance |  | 10   | pF   |

**AC Test Loads and Waveforms**


C133-4

**Switching Characteristics** Over the Operating Range<sup>[6]</sup>

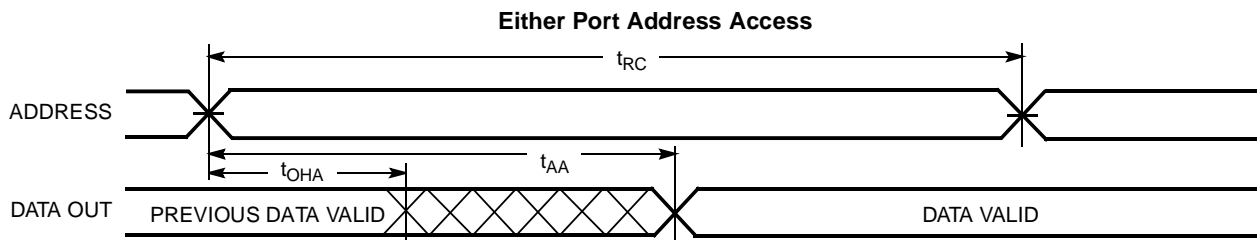
| Parameter                         | Description  | 7C133-25<br>7C143-25 |      | 7C133-35<br>7C143-35 |      | 7C133-55<br>7C143-55 |      | Unit |
|-----------------------------------|--|----------------------|------|----------------------|------|----------------------|------|------|
|                                   |  | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |      |
| <b>READ CYCLE</b>                 |  |                      |      |                      |      |                      |      |      |
| t <sub>RC</sub>                   | Read Cycle Time                                      | 25                   |      | 35                   |      | 55                   |      | ns   |
| t <sub>AA</sub>                   | Address to Data Valid <sup>[7]</sup>                 |                      | 25   |                      | 35   |                      | 55   | ns   |
| t <sub>OHA</sub>                  | Data Hold from Address Change                        | 0                    |      | 0                    |      | 0                    |      | ns   |
| t <sub>ACE</sub>                  | $\overline{CE}$ LOW to Data Valid <sup>[7]</sup>     |                      | 25   |                      | 35   |                      | 55   | ns   |
| t <sub>DOE</sub>                  | $\overline{OE}$ LOW to Data Valid <sup>[7]</sup>     |                      | 20   |                      | 25   |                      | 30   | ns   |
| t <sub>LZOE</sub>                 | $\overline{OE}$ LOW to Low Z <sup>[8, 9, 10]</sup>   | 3                    |      | 3                    |      | 3                    |      | ns   |
| t <sub>HZOE</sub>                 | $\overline{OE}$ HIGH to High Z <sup>[8, 9, 10]</sup> |                      | 15   |                      | 20   |                      | 25   | ns   |
| t <sub>LZCE</sub>                 | $\overline{CE}$ LOW to Low Z <sup>[8, 9, 10]</sup>   | 3                    |      | 5                    |      | 5                    |      | ns   |
| t <sub>HZCE</sub>                 | $\overline{CE}$ HIGH to High Z <sup>[8, 9, 10]</sup> |                      | 15   |                      | 20   |                      | 20   | ns   |
| t <sub>PU</sub>                   | $\overline{CE}$ LOW to Power-Up <sup>[10]</sup>      | 0                    |      | 0                    |      | 0                    |      | ns   |
| t <sub>PD</sub>                   | $\overline{CE}$ HIGH to Power-Down <sup>[10]</sup>   |                      | 25   |                      | 25   |                      | 25   | ns   |
| <b>WRITE CYCLE<sup>[11]</sup></b> |  |                      |      |                      |      |                      |      |      |
| t <sub>WC</sub>                   | Write Cycle Time                                     | 25                   |      | 35                   |      | 55                   |      | ns   |
| t <sub>SCE</sub>                  | $\overline{CE}$ LOW to Write End                     | 20                   |      | 25                   |      | 40                   |      | ns   |
| t <sub>AW</sub>                   | Address Set-Up to Write End                          | 20                   |      | 25                   |      | 40                   |      | ns   |
| t <sub>HA</sub>                   | Address Hold from Write End                          | 2                    |      | 2                    |      | 2                    |      | ns   |
| t <sub>SA</sub>                   | Address Set-Up to Write Start                        | 0                    |      | 0                    |      | 0                    |      | ns   |
| t <sub>PWE</sub>                  | R $\overline{W}$ Pulse Width                         | 20                   |      | 25                   |      | 35                   |      | ns   |
| t <sub>SD</sub>                   | Data Set-Up to Write End                             | 15                   |      | 20                   |      | 20                   |      | ns   |
| t <sub>HD</sub>                   | Data Hold from Write End                             | 0                    |      | 0                    |      | 0                    |      | ns   |
| t <sub>HZWE</sub>                 | R $\overline{W}$ LOW to High Z <sup>[9, 10]</sup>    |                      | 15   |                      | 20   |                      | 20   | ns   |
| t <sub>LZWE</sub>                 | R $\overline{W}$ HIGH to Low Z <sup>[9, 10]</sup>    | 0                    |      | 0                    |      | 0                    |      | ns   |

**Notes:**

6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
7. AC Test Conditions use V<sub>OH</sub> = 1.6V and V<sub>OL</sub> = 1.4V.
8. At any given temperature and voltage condition for any given device, t<sub>LZCE</sub> is less than t<sub>HZCE</sub> and t<sub>LZOE</sub> is less than t<sub>HZOE</sub>.
9. t<sub>LZCE</sub>, t<sub>LZWE</sub>, t<sub>HZOE</sub>, t<sub>LZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
10. This parameter is guaranteed but not tested.
11. The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and R $\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

**Switching Characteristics** Over the Operating Range<sup>[6]</sup> (continued)

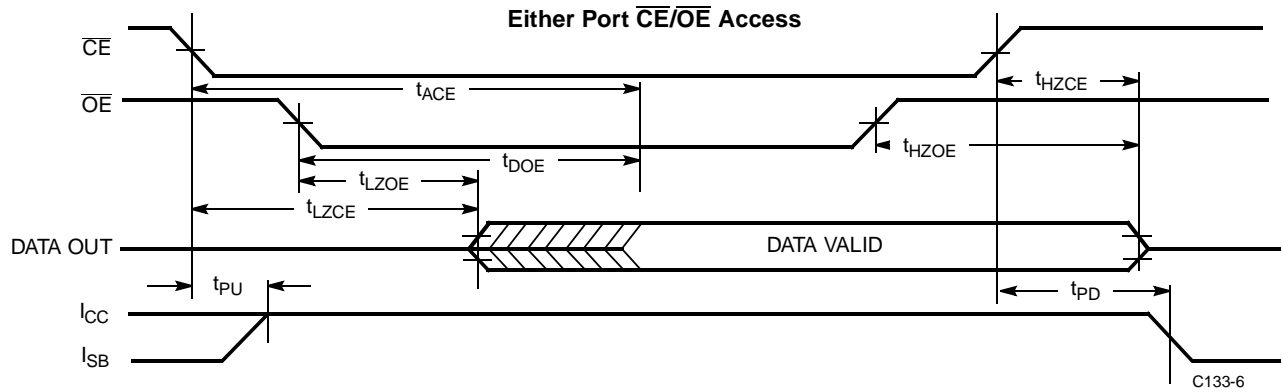
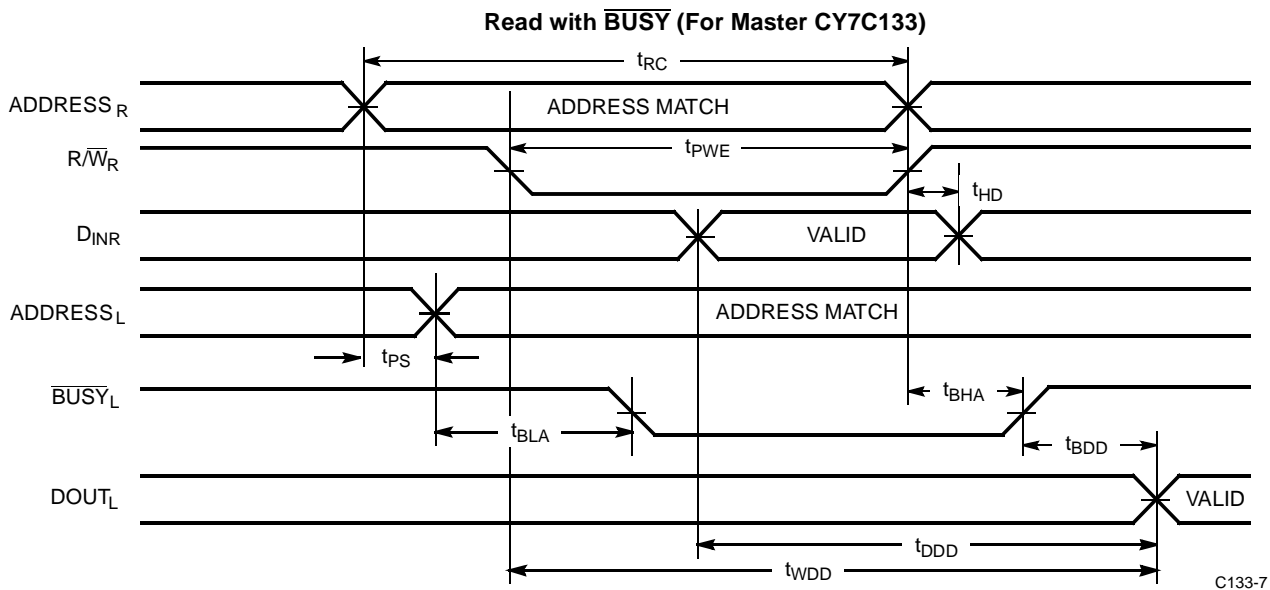
| Parameter   | Description  | 7C133-25<br>7C143-25 |         | 7C133-35<br>7C143-35 |         | 7C133-55<br>7C143-55 |         | Unit |
|---|--|----------------------|---------|----------------------|---------|----------------------|---------|------|
|   |  | Min.                 | Max.    | Min.                 | Max.    | Min.                 | Max.    |      |
| <b>BUSY/INTERRUPT TIMING (For Master CY7C133)</b> |  |                      |         |                      |         |                      |         |      |
| $t_{BLA}$   | $\overline{BUSY}$ Low from Address Match             |                      | 25      |                      | 35      |                      | 50      | ns   |
| $t_{BHA}$   | $\overline{BUSY}$ High from Address Mismatch         |                      | 20      |                      | 30      |                      | 40      | ns   |
| $t_{BLC}$   | $\overline{BUSY}$ Low from $\overline{CE}$ LOW       |                      | 20      |                      | 25      |                      | 35      | ns   |
| $t_{BHC}$   | $\overline{BUSY}$ High from $\overline{CE}$ HIGH     |                      | 20      |                      | 20      |                      | 30      | ns   |
| $t_{WDD}$   | Write Pulse to Data Delay <sup>[12]</sup>            |                      | 50      |                      | 60      |                      | 80      | ns   |
| $t_{DDD}$   | Write Data Valid to Read Data Valid <sup>[12]</sup>  |                      | 35      |                      | 45      |                      | 55      | ns   |
| $t_{BDD}$   | $\overline{BUSY}$ High to Valid Data <sup>[13]</sup> |                      | Note 13 |                      | Note 13 |                      | Note 13 | ns   |
| $t_{PS}$  | Arbitration Priority Set Up Time <sup>[14]</sup>     | 5                    |         | 5                    |         | 5                    |         | ns   |
| <b>BUSY TIMING (For Slave CY7C143)</b>            |  |                      |         |                      |         |                      |         |      |
| $t_{WB}$  | Write to $\overline{BUSY}$ <sup>[15]</sup>           | 0                    |         | 0                    |         | 0                    |         | ns   |
| $t_{WH}$  | Write Hold After $\overline{BUSY}$ <sup>[16]</sup>   | 20                   |         | 25                   |         | 30                   |         | ns   |
| $t_{WDD}$   | Write Pulse to Data Delay <sup>[17]</sup>            |                      | 50      |                      | 60      |                      | 80      | ns   |
| $t_{DDD}$   | Write Data Valid to Read Data Valid <sup>[17]</sup>  |                      | 35      |                      | 45      |                      | 55      | ns   |

**Switching Waveforms**
**Read Cycle No.1** <sup>[18, 19]</sup>


C133-5

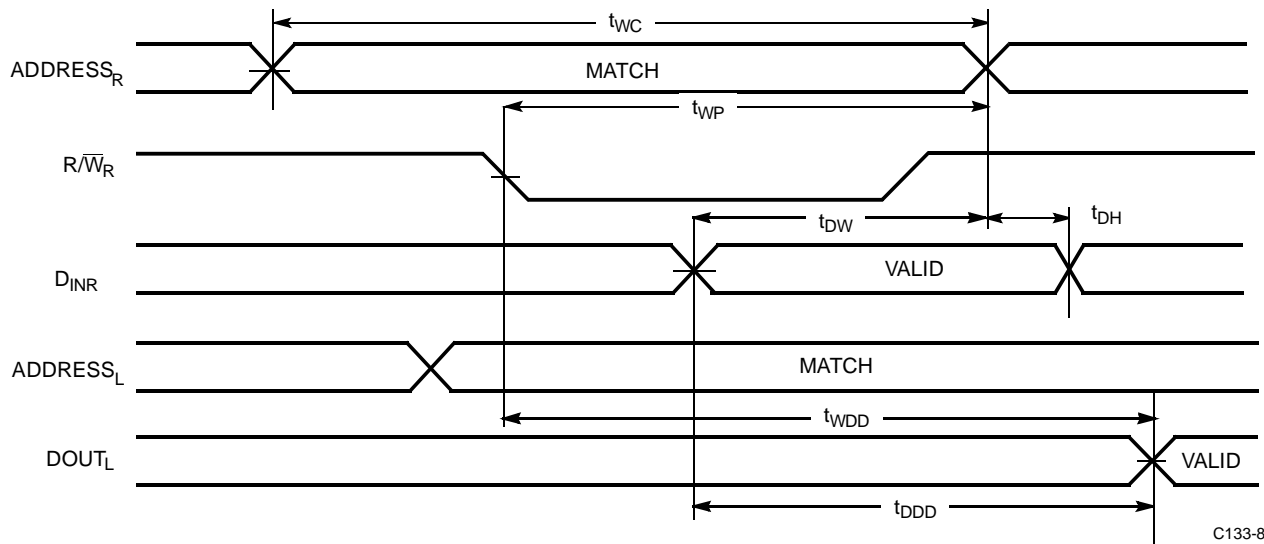
**Notes:**

12. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveform of "Read with  $\overline{BUSY}$ , Master: CY7C133."
13.  $t_{BDD}$  is a calculated parameter and is greater of  $0, t_{WDD} - t_{WP}$  (actual) or  $t_{DDD} - t_{DW}$  (actual).
14. To ensure that the earlier of the two ports wins.
15. To ensure that write cycle is inhibited during contention.
16. To ensure that a write cycle is completed after contention.
17. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveform of "Read with Port-to-port Delay."
18. R/W is HIGH for read cycle.
19. Device is continuously selected,  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .

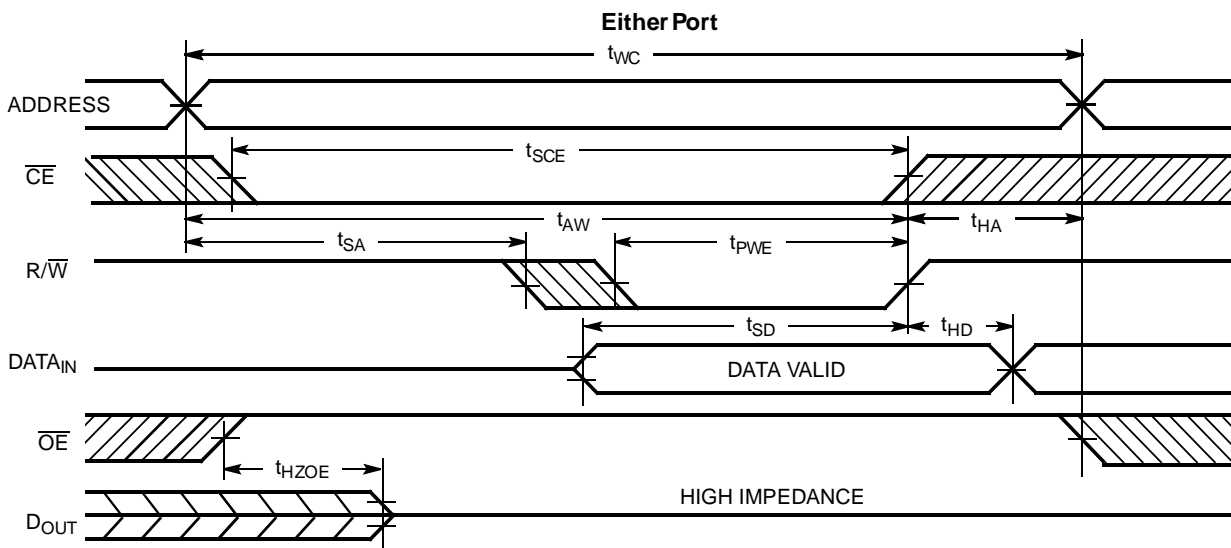
**Switching Waveforms (continued)**
**Read Cycle No. 2** <sup>[18, 20]</sup>

**Read Cycle No. 3** <sup>[19]</sup>

**Note:**

20. Address valid prior to or coincidence with  $\overline{CE}$  transition LOW.

**Switching Waveforms** (continued)

**Timing Waveform of Read with Port-to-port Delay No. 4 (For Slave CY7C143)** [21, 22, 23]


C133-8

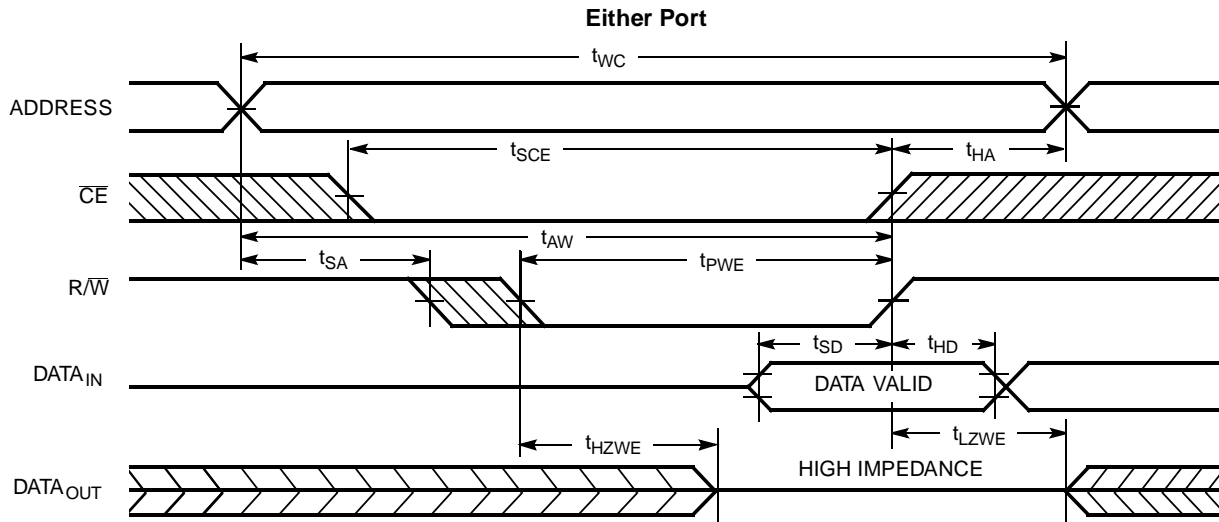
**Write Cycle No. 1 (OE Three-States Data I/Os - Either Port)** [14, 24]


C133-9

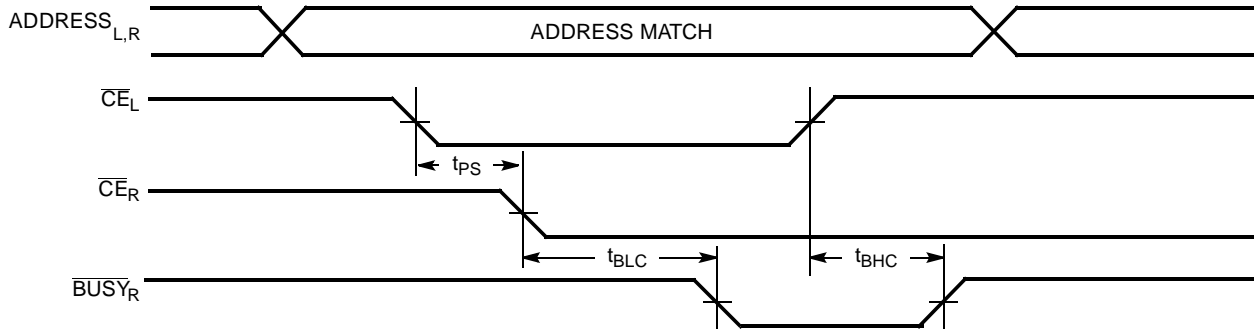
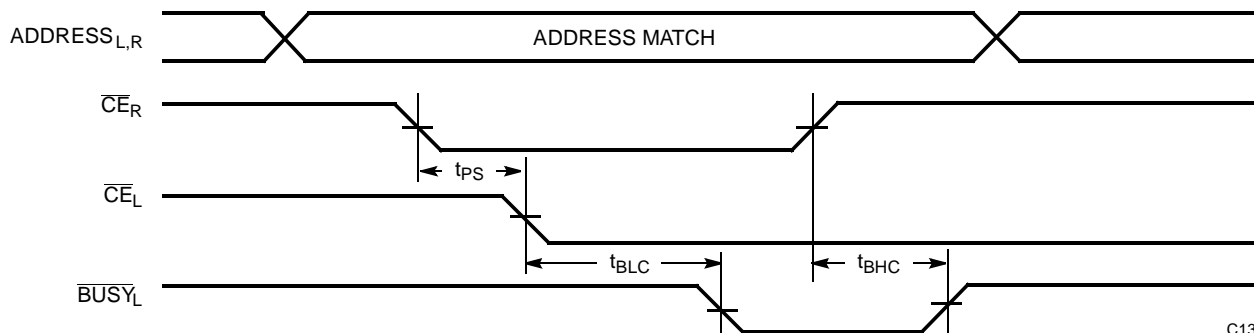
**Notes:**

21. Assume  $\overline{\text{BUSY}}$  input at  $V_{IH}$  for the writing port and at  $V_{IL}$  for the reading port.
22. Write cycle parameters should be adhered to in order to ensure proper writing.
23. Device is continuously enabled for both ports.
24. If  $\overline{\text{OE}}$  is LOW during a  $\text{R}/\overline{\text{W}}$  controlled write cycle, the write pulse width must be the larger of  $t_{\text{PWE}}$  or  $t_{\text{HZWE}} + t_{\text{SD}}$  to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required  $t_{\text{SD}}$ .



**Switching Waveforms (continued)**
**Write Cycle No. 2 (R/W Three-States Data I/Os—Either Port)** <sup>[20, 25]</sup>


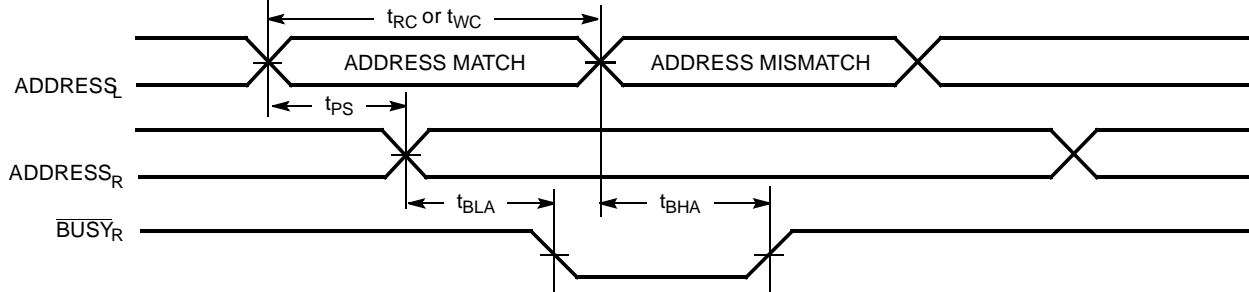
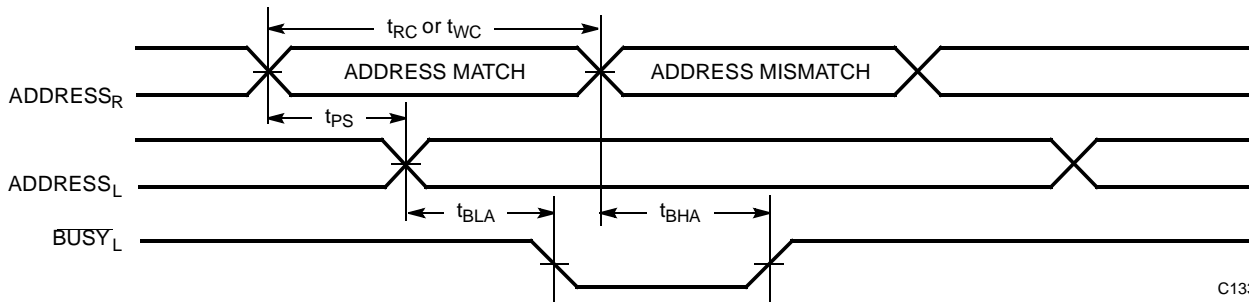
C133-10

**Busy Timing Diagram No. 1 ( $\overline{CE}$  Arbitration)**
 **$\overline{CE}_L$  Valid First:**

 **$\overline{CE}_R$  Valid First:**


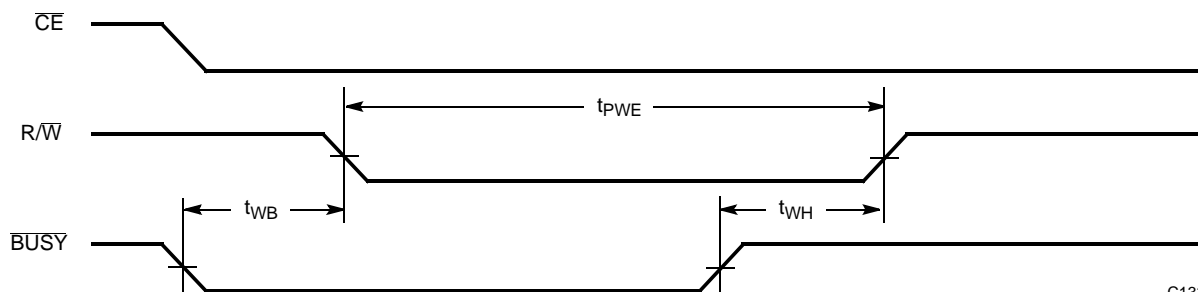
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**Note:**

 25. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high-impedance state.

**Switching Waveforms (continued)**
**Busy Timing Diagram No. 2 (Address Arbitration)**
**Left Address Valid First:**

**Right Address Valid First:**


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**Busy Timing Diagram No. 3**
**Write with  $\overline{\text{BUSY}}$  (For Slave CY7C143)**


C133-13

## Architecture

The CY7C133 (master) and CY7C143 (slave) consist of an array of 2K words of 16 bits each of dual-port RAM cells, I/O and address lines, and control signals ( $\overline{CE}$ ,  $\overline{OE}$ ,  $R/\overline{W}$ ). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a  $\overline{BUSY}$  pin is provided on each port. The CY7C133 and CY7C143 have an automatic power-down feature controlled by  $\overline{CE}$ . Each port is provided with its own output enable control ( $\overline{OE}$ ), which allows data to be read from the device.

## Functional Description

### Write Operation

Data must be set up for a duration of  $t_{SD}$  before the rising edge of  $R/\overline{W}$  in order to guarantee a valid write. A write operation is controlled by either the  $R/\overline{W}$  pin (see Write Cycle No. 1 waveform) or the  $\overline{CE}$  pin (see Write Cycle No. 2 waveform). Two  $R/\overline{W}$  pins ( $R/\overline{W}_{UB}$  and  $R/\overline{W}_{LB}$ ) are used to separate the upper and lower bytes of IO. Required inputs for non-contention operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flow-through delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port  $t_{DD}$  after the data is presented on the other port.

### Read Operation

When reading the device, the user must assert both the  $\overline{OE}$  and  $\overline{CE}$  pins. Data will be available  $t_{ACE}$  after  $\overline{CE}$  or  $t_{DOE}$  after  $\overline{OE}$  is asserted.

### Busy

The CY7C133 (master) provides on-chip arbitration to resolve simultaneous memory location access (contention). Table 2 shows a summary of conditions where  $\overline{BUSY}$  is asserted. If both ports'  $\overline{CE}$ s are asserted and an address match occurs within  $t_{PS}$  of each other, the busy logic will determine which port has access. If  $t_{PS}$  is violated, one port will definitely gain permission to the location, but which one is not predictable.  $\overline{BUSY}$  will be asserted  $t_{BLA}$  after an address match or  $t_{BLC}$  after  $\overline{CE}$  is taken LOW. The results of all eight arbitration possibilities are summarized in Table 3.  $\overline{BUSY}$  is an open drain output and requires a pull-up resistor.

One master and as many slaves as necessary may be connected in parallel to expand the data bus width in 16 bit increments. The  $\overline{BUSY}$  output of the master is connected to the  $\overline{BUSY}$

input of the slave. Writing to slave devices must be delayed until after the  $\overline{BUSY}$  input has settled ( $t_{BLC}$  or  $t_{BLA}$ ). Otherwise, the slave chip may begin a write cycle during a contention situation.

### Flow-Through Operation

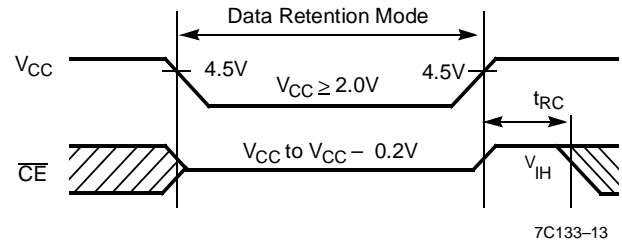
The CY7C133/143 has a flow-through architecture that facilitates repeating (actually extending) an operation when a  $\overline{BUSY}$  is received by a losing port. The  $\overline{BUSY}$  signal should be interpreted as a NOT READY. If a  $\overline{BUSY}$  to a port is active, the port should wait for  $\overline{BUSY}$  to go inactive, and then extend the operation it was performing for another cycle. The timing diagram titled, "Timing waveform with port to port delay" illustrates the case where the right port is writing to an address and the left port reads the same address. The data that the right port has just written flows through to the left, and is valid either  $t_{DD}$  after the falling edge of the write strobe of the left port, or  $t_{DD}$  after the data being written becomes stable.

### Data Retention Mode

The CY7C133/143 is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip enable ( $\overline{CE}$ ) must be held HIGH during data retention, within  $V_{CC}$  to  $V_{CC} - 0.2V$ .
2.  $\overline{CE}$  must be kept between  $V_{CC} - 0.2V$  and 70% of  $V_{CC}$  during the power-up and power-down transitions.
3. The RAM can begin operation  $>t_{RC}$  after  $V_{CC}$  reaches the minimum operating voltage (4.5 volts).

### Timing



7C133-13

| Parameter   | Test Conditions <sup>[26]</sup> | Max. | Unit |
|-------------|---------------------------------|------|------|
| $I_{CCDR1}$ | @ $V_{CCDR} = 2V$               | 1.5  | mA   |

Note:

26.  $\overline{CE} = V_{CC}$ ,  $V_{in} = GND$  to  $V_{CC}$ ,  $T_A = 25^\circ C$ . This parameter is guaranteed but not tested.

**Table 1. Non-Contending Read/Write Control**

| Control           |                   |    |    | I/O                                |                                     | Operation                         |
|-------------------|-------------------|----|----|------------------------------------|-------------------------------------|-----------------------------------|
| R/W <sub>LB</sub> | R/W <sub>UB</sub> | CE | OE | I/O <sub>0</sub> -I/O <sub>8</sub> | I/O <sub>9</sub> -I/O <sub>17</sub> |                                   |
| X                 | X                 | H  | X  | High Z                             | High Z                              | Deselected: Power-Down            |
| L                 | L                 | L  | X  | Data In                            | Data In                             | Write to Both Bytes               |
| L                 | H                 | L  | L  | Data In                            | Data Out                            | Write Lower Byte, Read Upper Byte |
| H                 | L                 | L  | L  | Data Out                           | Data In                             | Read Lower Byte, Write Upper Byte |
| L                 | H                 | L  | H  | Data In                            | High Z                              | Write to Lower Byte               |
| H                 | L                 | L  | H  | High Z                             | Data In                             | Write to Upper Byte               |
| H                 | H                 | L  | L  | Data Out                           | Data Out                            | Read to Both Bytes                |
| H                 | H                 | L  | H  | High Z                             | High Z                              | High Impedance Outputs            |

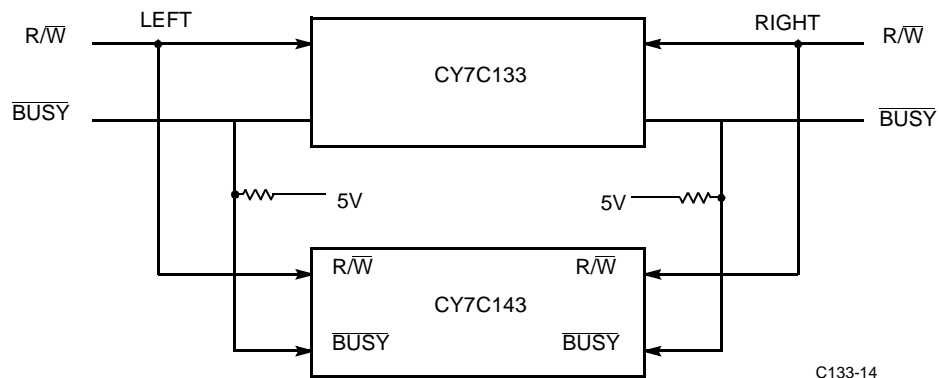
**Table 2. Address BUSY Arbitration**

| Inputs          |                 |  | Outputs           |                   | Function                      |
|-----------------|-----------------|--|-------------------|-------------------|-------------------------------|
| CE <sub>L</sub> | CE <sub>R</sub> | Address <sub>L</sub><br>Address <sub>R</sub> | BUSY <sub>L</sub> | BUSY <sub>R</sub> |                               |
| X               | X               | No Match                                     | H                 | H                 | Normal                        |
| H               | X               | Match  | H                 | H                 | Normal                        |
| X               | H               | Match  | H                 | H                 | Normal                        |
| L               | L               | Match  | Note 27           | Note 27           | Write Inhibit <sup>[28]</sup> |

**Notes:**

27. The loser of the port arbitration will receive BUSY = "L" (BUSY<sub>L</sub> or BUSY<sub>R</sub> = "L"). BUSY<sub>L</sub> and BUSY<sub>R</sub> cannot both be LOW simultaneously.

28. Writes are inhibited to the left port when BUSY<sub>L</sub> is LOW. Writes are inhibited to the right port when BUSY<sub>R</sub> is LOW.

**32-Bit Master/Slave Dual-Port Memory Systems**


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**Table 3. Arbitration Results**

| Case | Port  |       | Winning Port | Result                                      |
|------|-------|-------|--------------|---|
|      | Left  | Right |              |   |
| 1    | Read  | Read  | L            | Both ports read                             |
| 2    | Read  | Read  | R            | Both ports read                             |
| 3    | Read  | Write | L            | L port reads OK R port write inhibited      |
| 4    | Read  | Write | R            | R port writes OK L port data may be invalid |
| 5    | Write | Read  | L            | L port writes OK R port data may be invalid |
| 6    | Write | Read  | R            | R port reads OK L port write inhibited      |
| 7    | Write | Write | L            | L port writes OK R port write inhibited     |
| 8    | Write | Write | R            | R port writes OK L port write inhibited     |

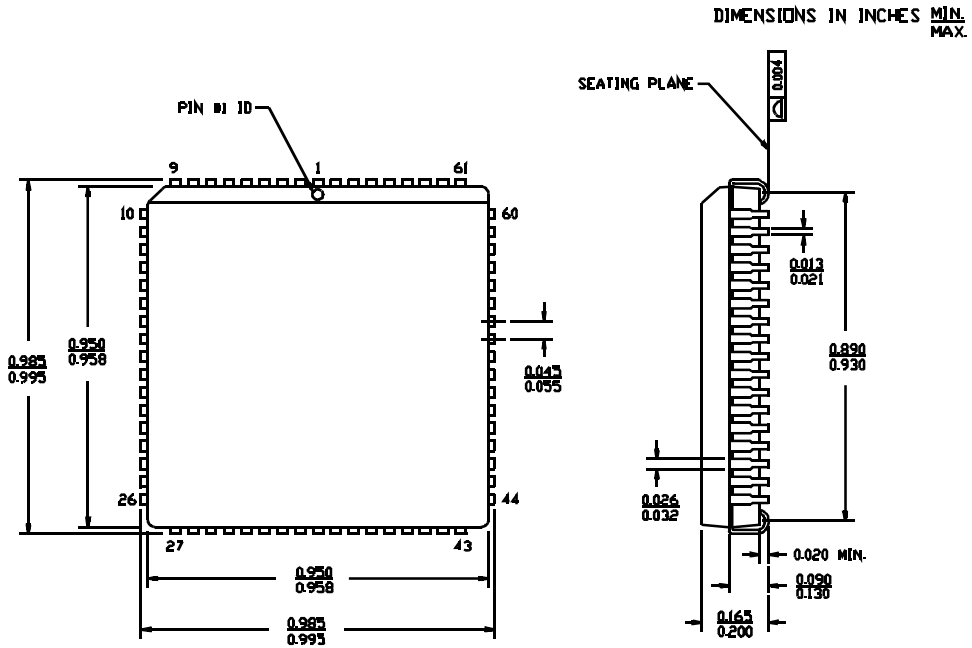
**Ordering Information**
**2K x16 Master Dual-Port SRAM**

| Speed (ns) | Ordering Code | Package Name | Package Type                        | Operating Range |
|------------|---------------|--------------|-------------------------------------|-----------------|
| 25         | CY7C133-25JC  | J81          | 68-Lead Plastic Leaded Chip Carrier | Commercial      |
|            | CY7C133-25JI  | J81          | 68-Lead Plastic Leaded Chip Carrier | Industrial      |
| 35         | CY7C133-35JC  | J81          | 68-Lead Plastic Leaded Chip Carrier | Commercial      |
|            | CY7C133-35JI  | J81          | 68-Lead Plastic Leaded Chip Carrier | Industrial      |
| 55         | CY7C133-55JC  | J81          | 68-Lead Plastic Leaded Chip Carrier | Commercial      |
|            | CY7C133-55JI  | J81          | 68-Lead Plastic Leaded Chip Carrier | Industrial      |

**2K x16 Slave Dual-Port SRAM**

| Speed (ns) | Ordering Code | Package Name | Package Type                        | Operating Range |
|------------|---------------|--------------|-------------------------------------|-----------------|
| 25         | CY7C143-25JC  | J81          | 68-Lead Plastic Leaded Chip Carrier | Commercial      |
|            | CY7C143-25JI  | J81          | 68-Lead Plastic Leaded Chip Carrier | Industrial      |
| 35         | CY7C143-35JC  | J81          | 68-Lead Plastic Leaded Chip Carrier | Commercial      |
|            | CY7C143-35JI  | J81          | 68-Lead Plastic Leaded Chip Carrier | Industrial      |
| 55         | CY7C143-55JC  | J81          | 68-Lead Plastic Leaded Chip Carrier | Commercial      |
|            | CY7C143-55JI  | J81          | 68-Lead Plastic Leaded Chip Carrier | Industrial      |

Document #: 38-00414-B

**Package Diagram**
**68-Lead Plastic Leaded Chip Carrier J81**


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