



## 16-Bit, Ultra-Low Power, Voltage-Output Digital-to-Analog Converter

### FEATURES

- **16-Bit Resolution**
- **2.7 V to 5.5 V Single-Supply Operation**
- **Very Low Power: 15  $\mu$ W for 3 V Power**
- **High Accuracy, INL: 1 LSB**
- **Low Noise: 18n V/ $\sqrt{\text{Hz}}$**
- **Fast Settling: 1.0  $\mu$ S**
- **Fast SPI™ Interface, up to 50 MHz**
- **Reset to Mid-Code**
- **Schmitt-Trigger Inputs for Direct Optocoupler Interface**

### APPLICATIONS

- **Portable Equipment**
- **Automatic Test Equipment**
- **Industrial Process Control**
- **Data Acquisition Systems**
- **Optical Networking**

### DESCRIPTION

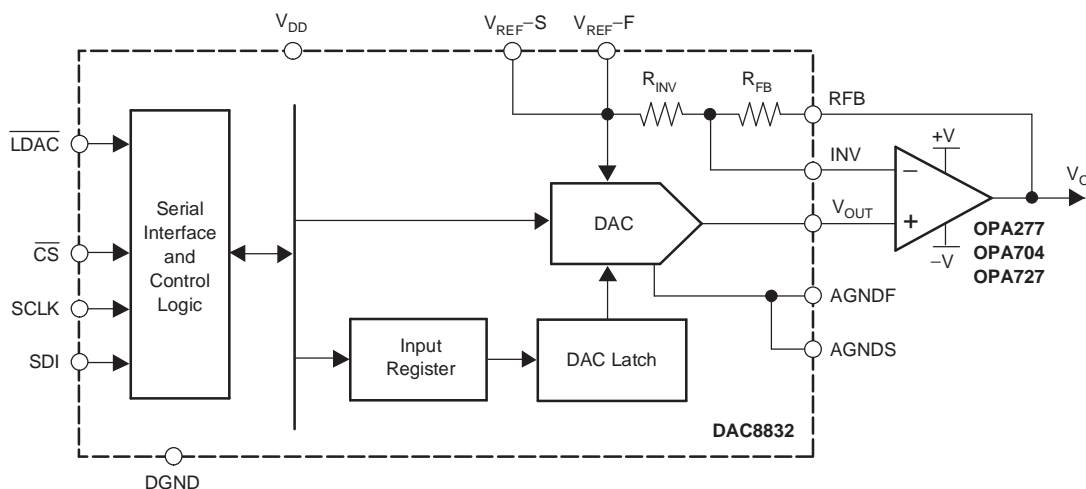
The DAC8832 is a single, 16-bit, serial-input, voltage-output digital-to-analog converter (DAC) operating from a single 3 V to 5 V power supply. The DAC8832 provides excellent linearity (1 LSB INL), low glitch, low noise, and fast settling (1.0  $\mu$ S to 1/2 LSB of full-scale output) over the specified temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . The output is unbuffered, which reduces the power consumption and the error introduced by the buffer.

This device features a standard high-speed (clock up to 50MHz), 3 V or 5 V SPI serial interface to communicate with a DSP or microprocessor.

The DAC8832 provides unipolar or bipolar output ( $\pm V_{\text{REF}}$ ) when working with an external buffer, and is reset to mid-code after power-up. For optimum performance, a set of Kelvin connections to the external reference and the analog ground input are provided.

The DAC8832 is available in a QFN-14 package, and is pin-to-pin compatible with the DAC8831IRGY, which is reset to zero code after power-up.

**Functional Block Diagram**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	POWER-ON RESET VALUE	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8832IRGY	±4	±1	Mid Code	–40°C to +85°C	8832I	QFN-14	RGY	DAC8832IRGYT	Tape and Reel, 250
								DAC8832IRGYR	Tape and Reel, 1000
DAC8832IBRGY	±2	±1	Mid Code	–40°C to +85°C	8832I	QFN-14	RGY	DAC8832IBRGYT	Tape and Reel, 250
								DAC8832IBRGYR	Tape and Reel, 1000
DAC8832ICRGY	±1	±1	Mid Code	–40°C to +85°C	8832I	QFN-14	RGY	DAC8832ICRGYT	Tape and Reel, 250
								DAC8832ICRGYR	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	DAC8832	UNIT
$V_{DD}$ to AGND	–0.3 to +7	V
Digital input voltage to DGND	–0.3 to $+V_{DD} + 0.3$	V
$V_{OUT}$ to AGND	–0.3 to $+V_{DD} + 0.3$	V
AGND, AGNDF, AGNDS to DGND	–0.3 to +0.3	V
Operating temperature range	–40 to +85	°C
Storage temperature range	–65 to +150	°C
Junction temperature range ( $T_J$ max)	+150	°C
Power dissipation	$(T_J \text{ max} - T_A) / \theta_{JA}$	W
Thermal impedance, $\theta_{JA}$	54.9	°C/W

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

All specifications at  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{DD} = +3\text{ V}$  or  $V_{DD} = +5\text{ V}$ ,  $V_{REF} = +2.5\text{ V}$  unless otherwise noted.

PARAMETER		CONDITIONS	DAC8832			UNIT
			MIN	TYP	MAX	
<b>STATIC PERFORMANCE</b>						
Resolution			16			bits
Linearity error	DAC8832ICRGY			±0.5	±1	LSB
	DAC8832IBRGY			±0.5	±2	
	DAC8832IRGY			±0.5	±4	
Differential linearity error		All grades		±0.5	±1	LSB
Gain error	$T_A = +25^\circ\text{C}$			±1	±5	LSB
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				±7	
Gain drift				±0.1		ppm/°C
Zero code error	$T_A = +25^\circ\text{C}$			±0.25	±1	LSB
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				±2	
Zero code drift				±0.05		ppm/°C
<b>OUTPUT CHARACTERISTICS</b>						
Voltage output <sup>(1)</sup>	Unipolar operation		0		$+V_{REF}$	V
	Bipolar operation		$-V_{REF}$		$+V_{REF}$	V
Output impedance				6.25		kΩ
Settling time		To 1/2 LSB of FS, $C_L = 10\text{ pF}$		1		μs
Slew rate <sup>(2)</sup>		$C_L = 10\text{ pF}$		25		V/μs
Digital-to-analog glitch		1 LSB change around major carry		35		nV-s
Digital feedthrough <sup>(3)</sup>				0.2		nV-s
Output noise		$T_A = +25^\circ\text{C}$		18		nV/√Hz
Power-supply rejection		$V_{DD}$ varies ±10%			±1	LSB
Bipolar resistor matching	$R_{FB} / R_{INV}$			1		Ω/Ω
	Ratio error			±0.0015	±0.0076	%
Bipolar zero error	$T_A = +25^\circ\text{C}$			±0.25	±5	LSB
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				±7	
Bipolar zero drift				±0.2		ppm/°C

(1) See the [Bipolar Output Operation](#) section for details.

(2) Slew rate is measured from 10% to 90% of transition when the output changes from 0 to full-scale.

(3) Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change;  $\overline{CS}$  is held high, while SCLK and DIN signals are toggled.

**ELECTRICAL CHARACTERISTICS (continued)**

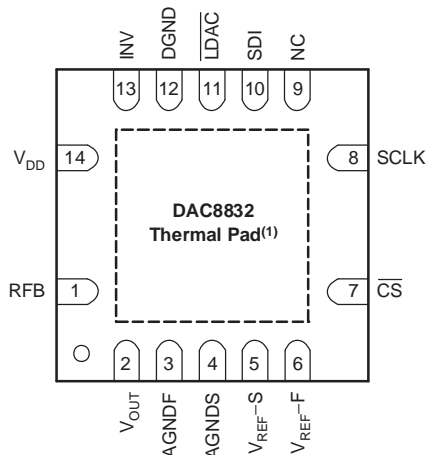
All specifications at  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{DD} = +3$  V or  $V_{DD} = +5$  V,  $V_{REF} = +2.5$  V unless otherwise noted.

PARAMETER	CONDITIONS	DAC8832			UNIT
		MIN	TYP	MAX	
<b>REFERENCE INPUT</b>					
Reference input voltage range		1.25		$V_{DD}$	V
Reference input impedance <sup>(4)</sup>	Unipolar mode	9			k $\Omega$
	Bipolar mode	7.5			
Reference –3 dB bandwidth, BW	Code = FFFFh		1.3		MHz
Reference feedthrough	Code = 0000h, $V_{REF} = 1$ V <sub>PP</sub> at 100 kHz		1		mV
Signal-to-noise ratio, SNR			92		dB
Reference input capacitance	Code = 0000h		75		pF
	Code = FFFFh		120		
<b>DIGITAL INPUTS</b>					
$V_{IL}$ Input low voltage	$V_{DD} = 2.7$ V			0.6	V
	$V_{DD} = 5$ V			0.8	
$V_{IH}$ Input high voltage	$V_{DD} = 2.7$ V	2.1			V
	$V_{DD} = 5$ V	2.4			
Input current				$\pm 1$	$\mu$ A
Input capacitance				10	pF
Hysteresis voltage			0.4		V
<b>POWER SUPPLY</b>					
$V_{DD}$ Power-supply voltage		2.7		5.5	V
$I_{DD}$ Power-supply current	$V_{DD} = 3$ V		5	20	$\mu$ A
	$V_{DD} = 5$ V		5	20	
Power	$V_{DD} = 3$ V		15	60	$\mu$ W
	$V_{DD} = 5$ V		25	100	
<b>TEMPERATURE RANGE</b>					
Specified performance		–40		+85	$^{\circ}$ C

(4) Reference input resistance is code-dependent, minimum at 8555h.

**PIN CONFIGURATION (NOT TO SCALE)**

**RGY PACKAGE  
QFN-14  
(TOP VIEW)**



NOTE: (1) Exposed thermal pad must be connected to analog ground.

**TERMINAL FUNCTIONS**

TERMINAL		DESCRIPTION
NO.	NAME	
1	RFB	Feedback resistor. Connect to the output of external operational amplifier in bipolar mode.
2	V <sub>OUT</sub>	Analog output of DAC
3	AGNDF	Analog ground (Force)
4	AGNDS	Analog ground (Sense)
5	V <sub>REF-S</sub>	Voltage reference input (Sense). Connect to external voltage reference
6	V <sub>REF-F</sub>	Voltage reference input (Force). Connect to external voltage reference
7	$\overline{CS}$	Chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low.
8	SCLK	Serial clock input.
9	NC	No internal connection
10	SDI	Serial data input. Data are latched into input register on the rising edge of SCLK.
11	$\overline{LDAC}$	Load DAC control input. Active low. When $\overline{LDAC}$ is Low, the DAC latch is simultaneously updated with the content of the input register.
12	DGND	Digital ground
13	INV	Junction point of internal scaling resistors. Connect to external operational amplifier inverting input in bipolar mode.
14	V <sub>DD</sub>	Analog power supply, +3 V to +5 V.

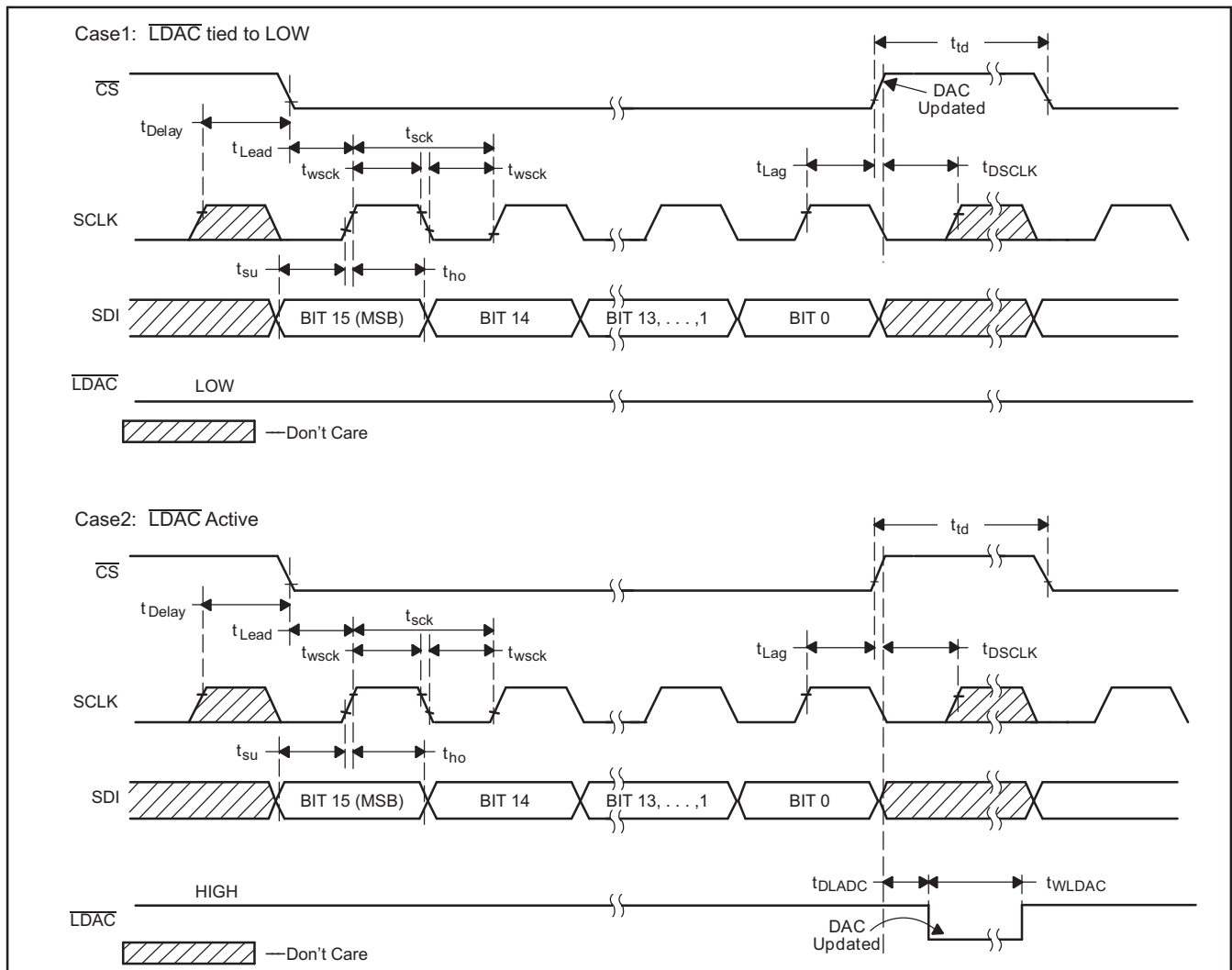


Figure 1. DAC8832 Timing Diagram

**TIMING CHARACTERISTICS:  $V_{DD} = +5 V^{(1)(2)}$** 

 At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
$t_{\text{sck}}$	SCLK period	20		ns
$t_{\text{wsck}}$	SCLK high or low time	10		ns
$t_{\text{Delay}}$	Delay from SCLK high to $\overline{\text{CS}}$ low	10		ns
$t_{\text{Lead}}$	$\overline{\text{CS}}$ enable lead time	10		ns
$t_{\text{Lag}}$	$\overline{\text{CS}}$ enable lag time	10		ns
$t_{\text{DSCLK}}$	Delay from $\overline{\text{CS}}$ high to SCLK high	10		ns
$t_{\text{td}}$	$\overline{\text{CS}}$ high between active period	30		ns
$t_{\text{su}}$	Data setup time (input)	10		ns
$t_{\text{ho}}$	Data hold time (input)	0		ns
$t_{\text{WLDAC}}$	$\overline{\text{LDAC}}$ width	30		ns
$t_{\text{DLDAC}}$	Delay from $\overline{\text{CS}}$ high to $\overline{\text{LDAC}}$ low	30		ns
	$V_{DD}$ high to $\overline{\text{CS}}$ low (power-up delay)	10		$\mu\text{s}$

(1) Assured by design. Not production tested.

(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

**TIMING CHARACTERISTICS:  $V_{DD} = +3 V^{(1)(2)}$** 

 At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise noted.

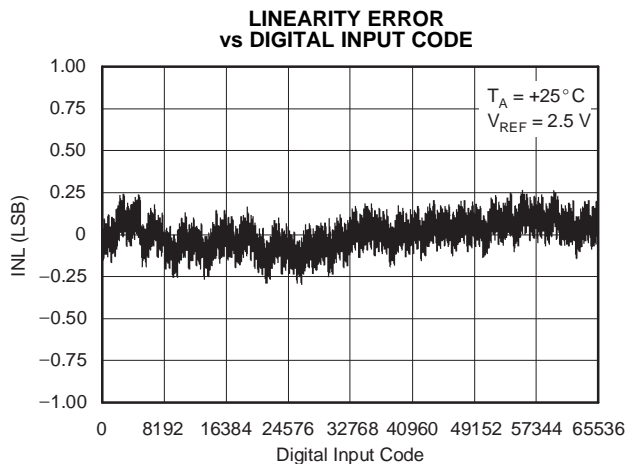
PARAMETER		MIN	MAX	UNIT
$t_{\text{sck}}$	SCLK period	20		ns
$t_{\text{wsck}}$	SCLK high or low time	10		ns
$t_{\text{Delay}}$	Delay from SCLK high to $\overline{\text{CS}}$ low	10		ns
$t_{\text{Lead}}$	$\overline{\text{CS}}$ enable lead time	10		ns
$t_{\text{Lag}}$	$\overline{\text{CS}}$ enable lag time	10		ns
$t_{\text{DSCLK}}$	Delay from $\overline{\text{CS}}$ high to SCLK high	10		ns
$t_{\text{td}}$	$\overline{\text{CS}}$ high between active period	30		ns
$t_{\text{su}}$	Data setup time (input)	10		ns
$t_{\text{ho}}$	Data hold time (input)	0		ns
$t_{\text{WLDAC}}$	$\overline{\text{LDAC}}$ width	30		ns
$t_{\text{DLDAC}}$	Delay from $\overline{\text{CS}}$ high to $\overline{\text{LDAC}}$ low	30		ns
	$V_{DD}$ high to $\overline{\text{CS}}$ low (power-up delay)	10		$\mu\text{s}$

(1) Assured by design. Not production tested.

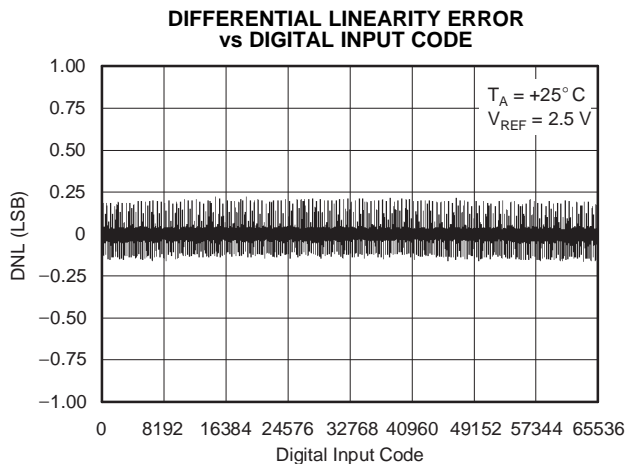
(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$**

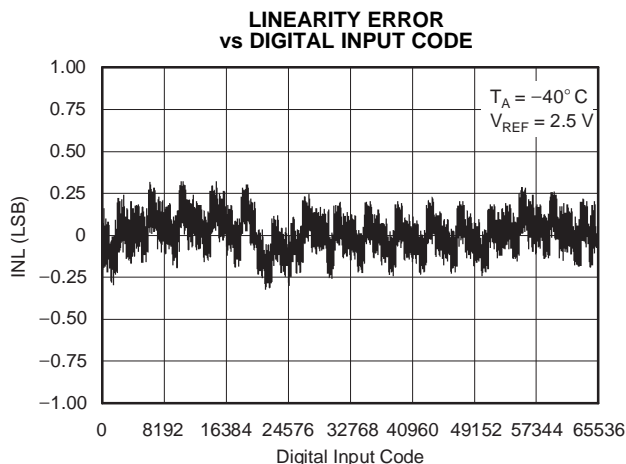
At  $T_A = +25^\circ\text{C}$ ,  $V_{REF} = +2.5\text{ V}$  unless otherwise noted.



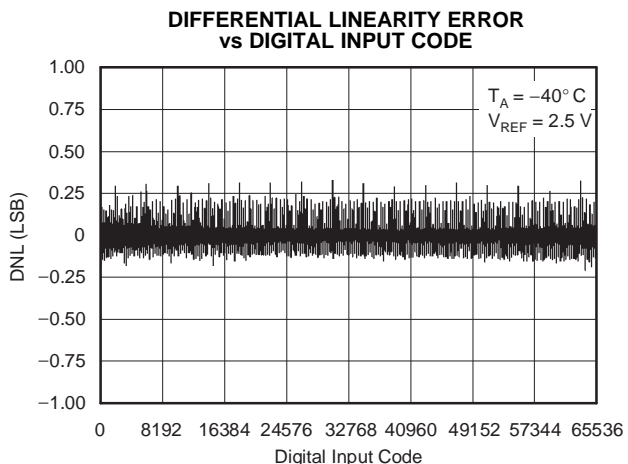
**Figure 2.**



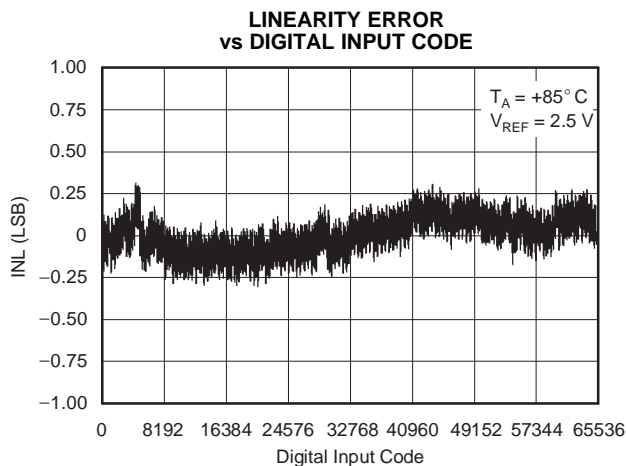
**Figure 3.**



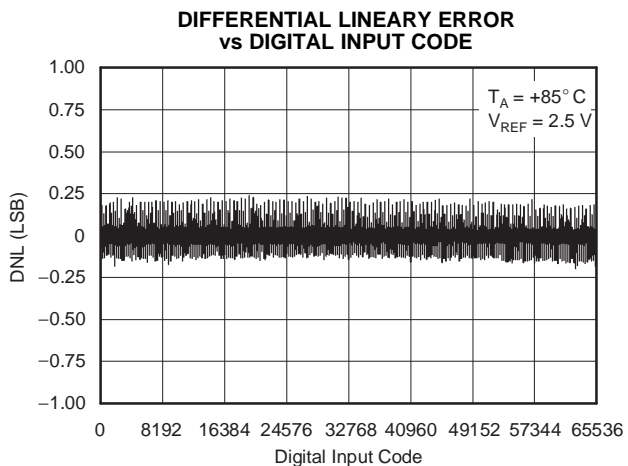
**Figure 4.**



**Figure 5.**



**Figure 6.**

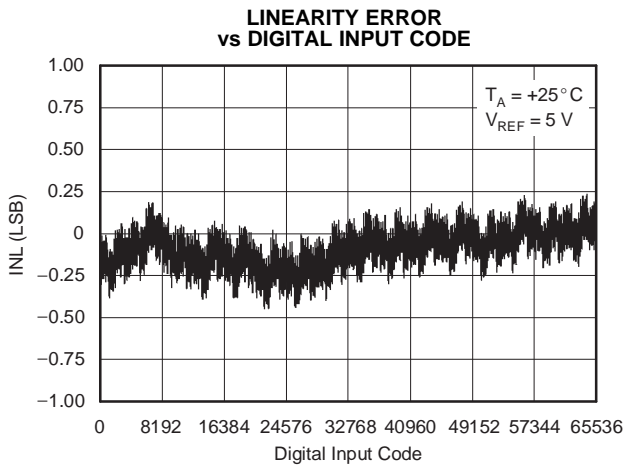


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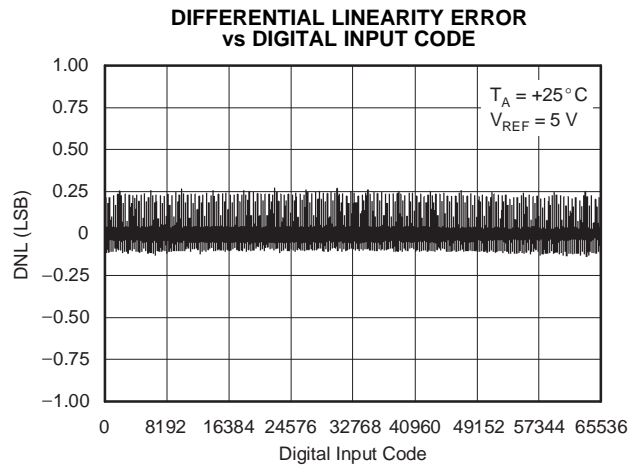


**TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$  (continued)**

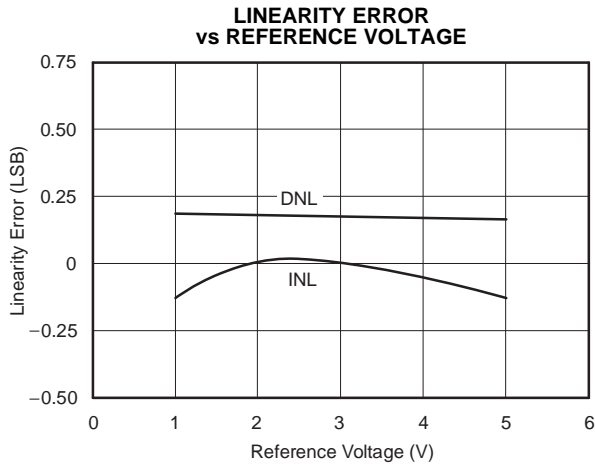
At  $T_A = +25^\circ\text{C}$ ,  $V_{REF} = +2.5\text{ V}$  unless otherwise noted.



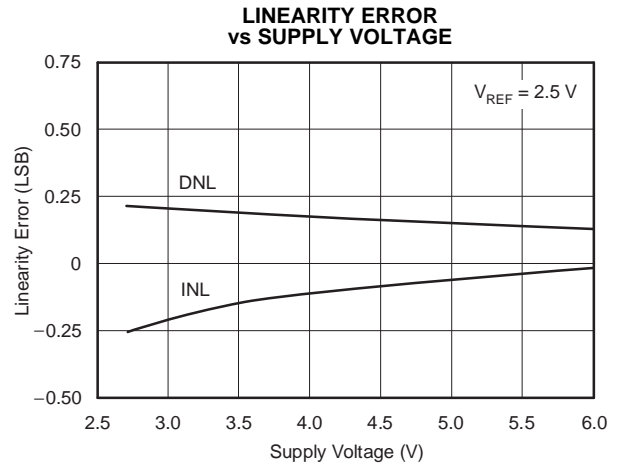
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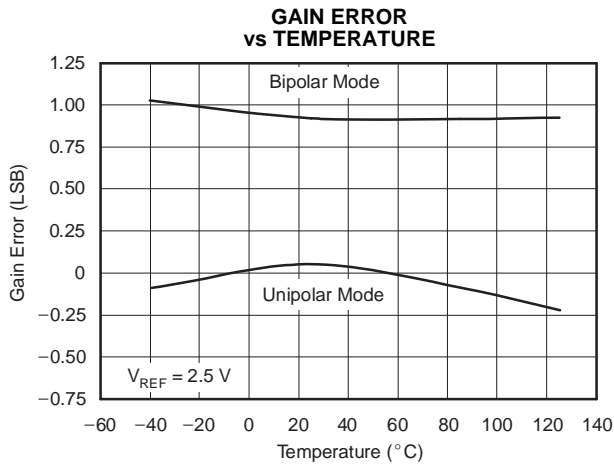
**Figure 9.**



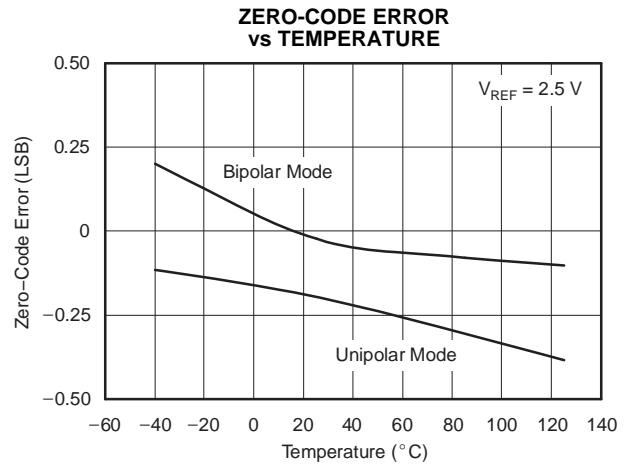
**Figure 10.**



**Figure 11.**



**Figure 12.**



**Figure 13.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_{REF} = +2.5\text{ V}$  unless otherwise noted.

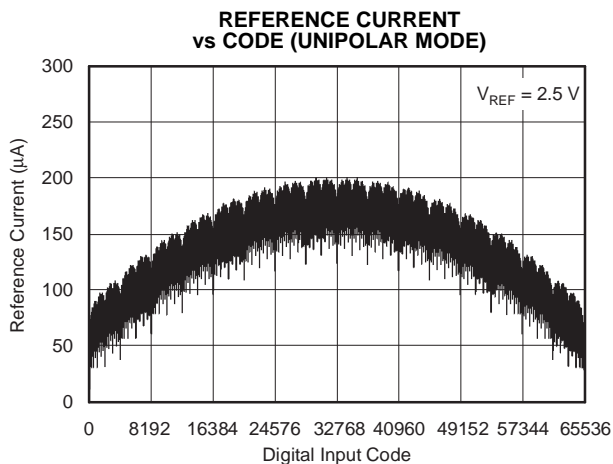


Figure 14.

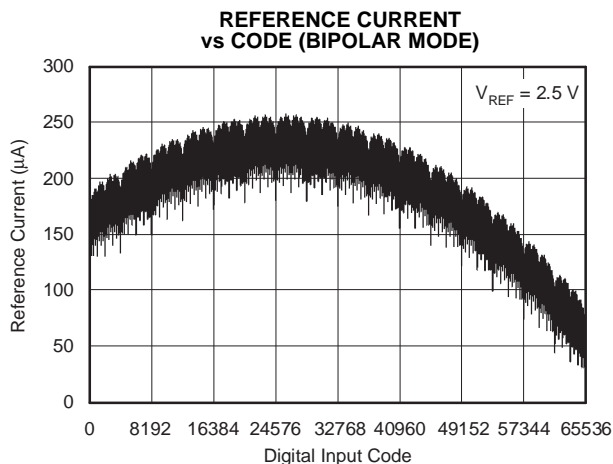


Figure 15.

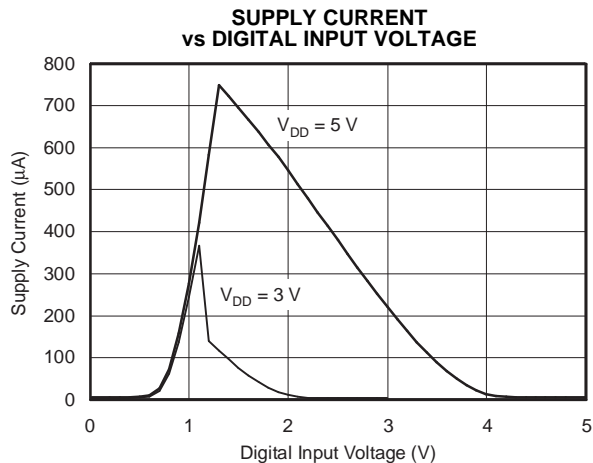


Figure 16.

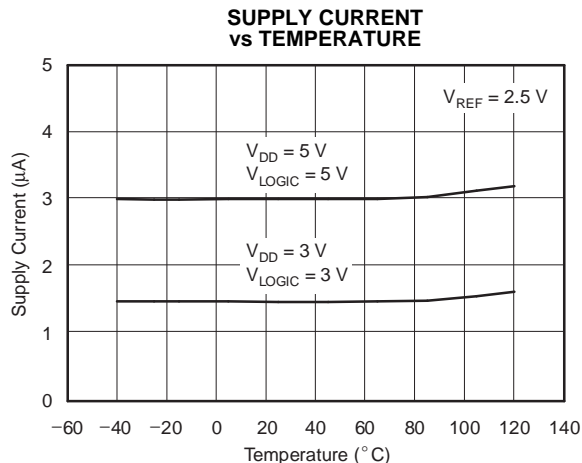


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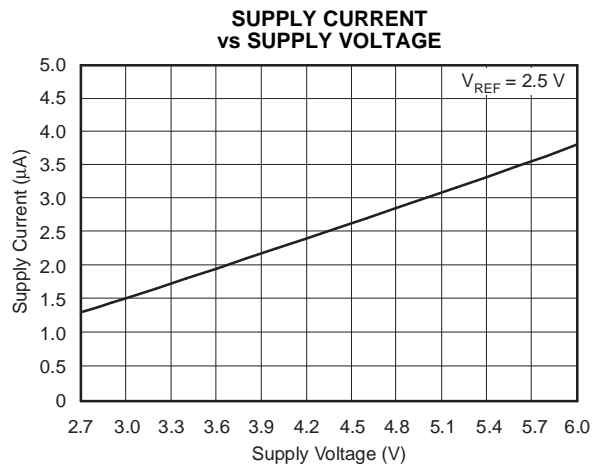


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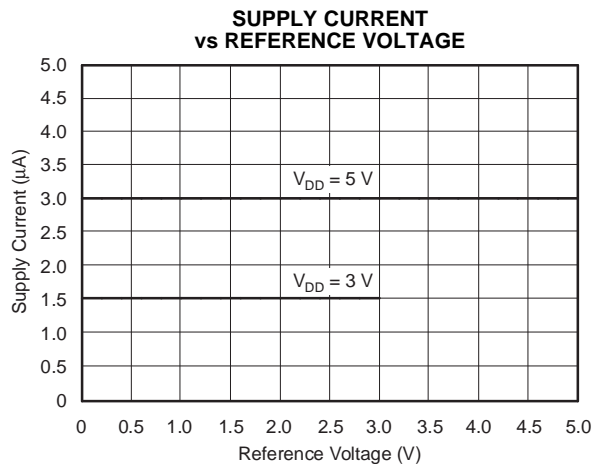
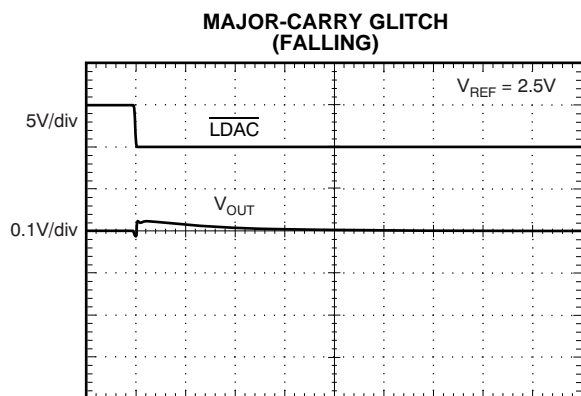


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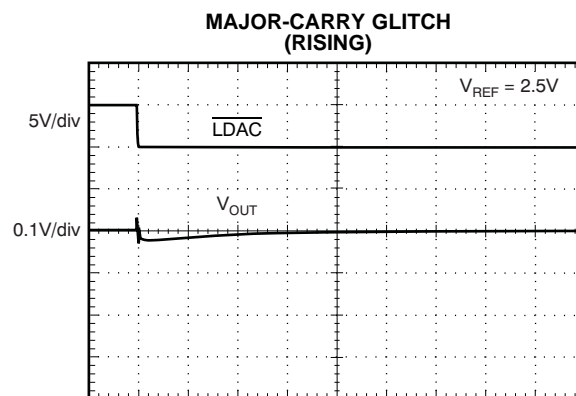
**TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_{REF} = +2.5\text{ V}$  unless otherwise noted.



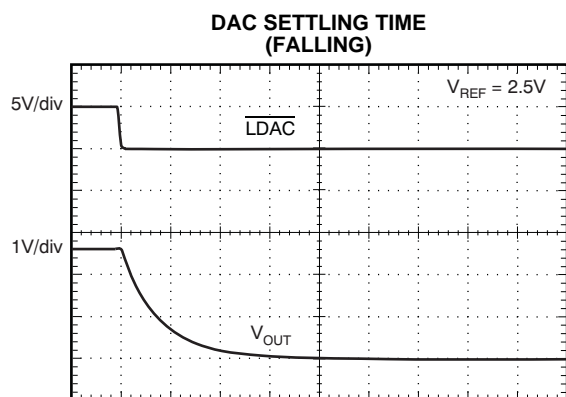
Time (0.5 $\mu\text{s}$ /div)

**Figure 20.**



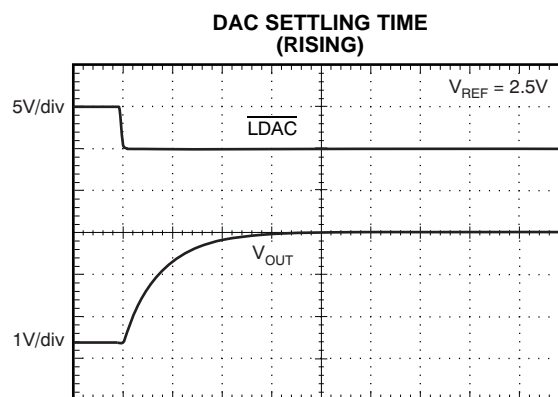
Time (0.5 $\mu\text{s}$ /div)

**Figure 21.**



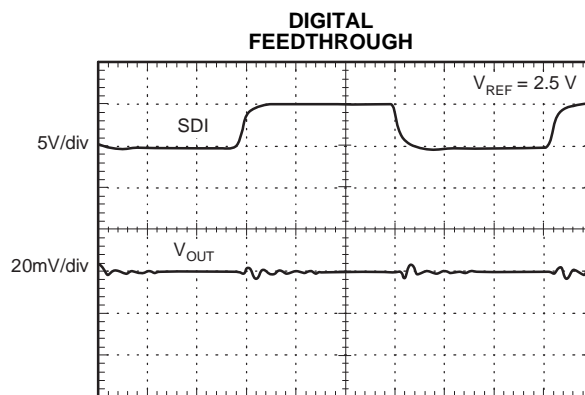
Time (0.2 $\mu\text{s}$ /div)

**Figure 22.**



Time (0.2 $\mu\text{s}$ /div)

**Figure 23.**

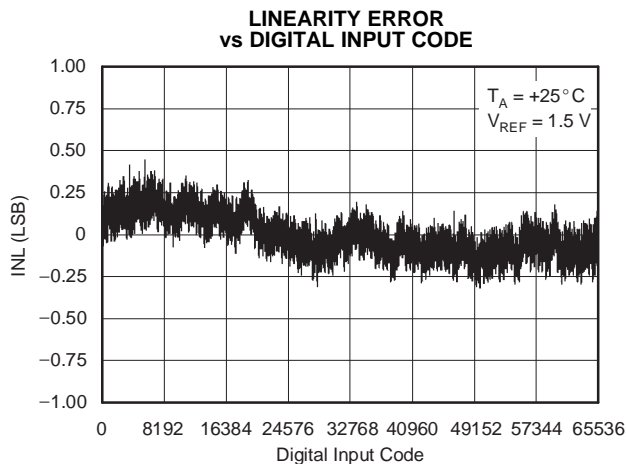


Time (50ns/div)

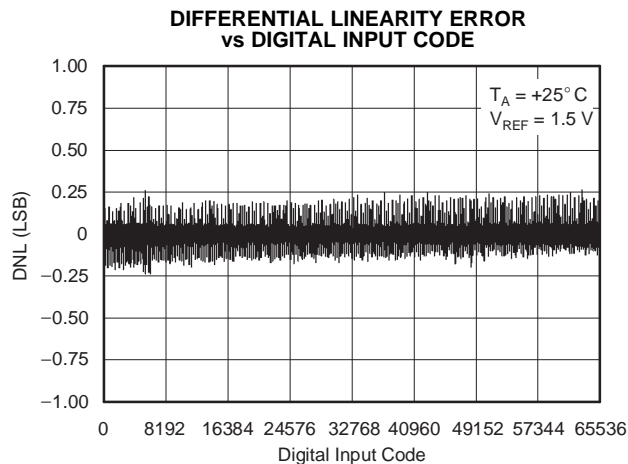
**Figure 24.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = +3\text{ V}$**

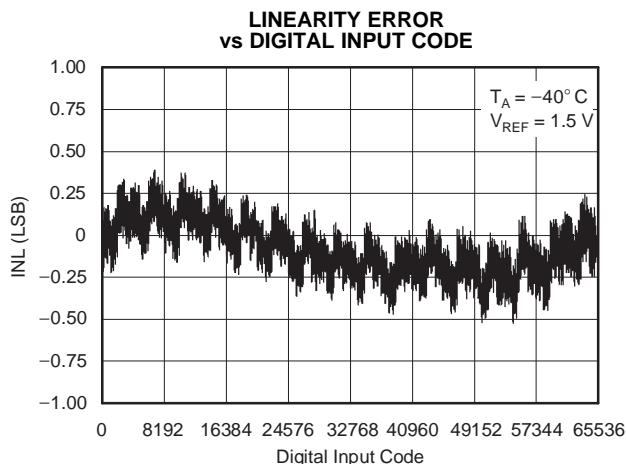
At  $T_A = +25^\circ\text{C}$ ,  $V_{REF} = +2.5\text{ V}$  unless otherwise noted.



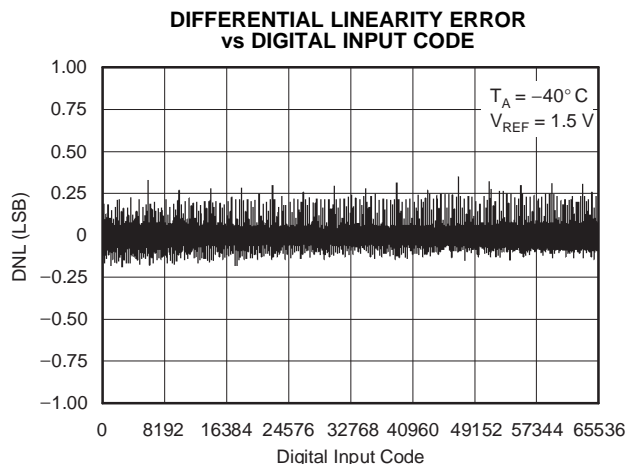
**Figure 25.**



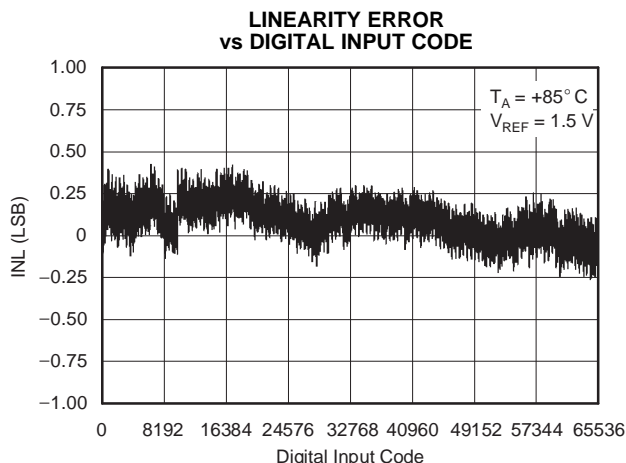
**Figure 26.**



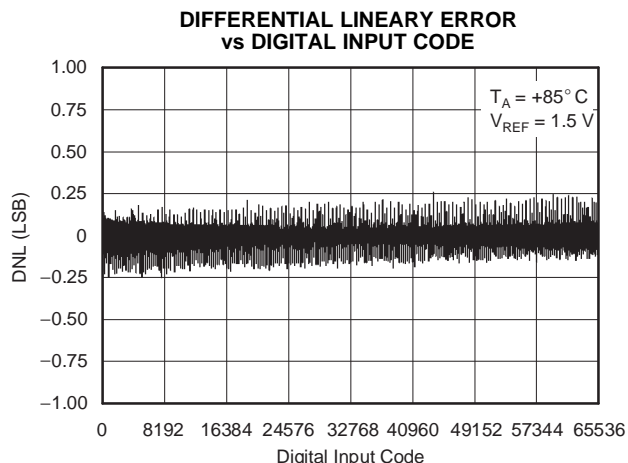
**Figure 27.**



**Figure 28.**



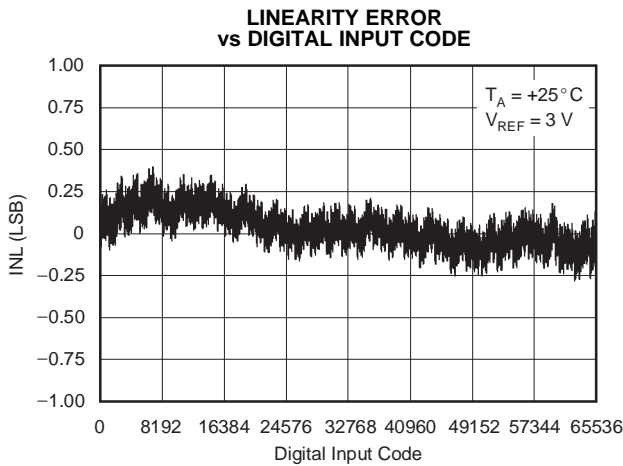
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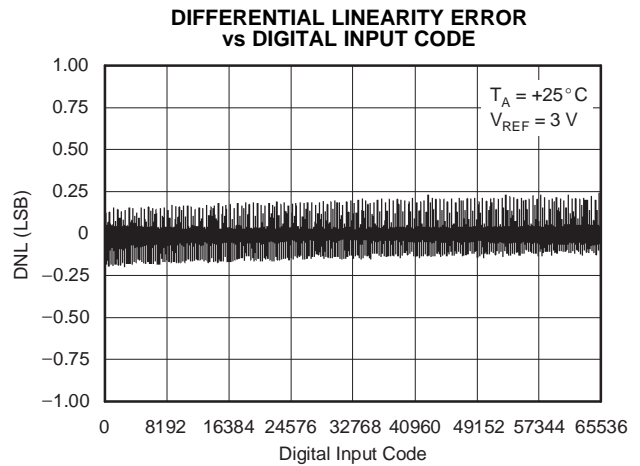
**Figure 30.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = +3\text{ V}$  (continued)**

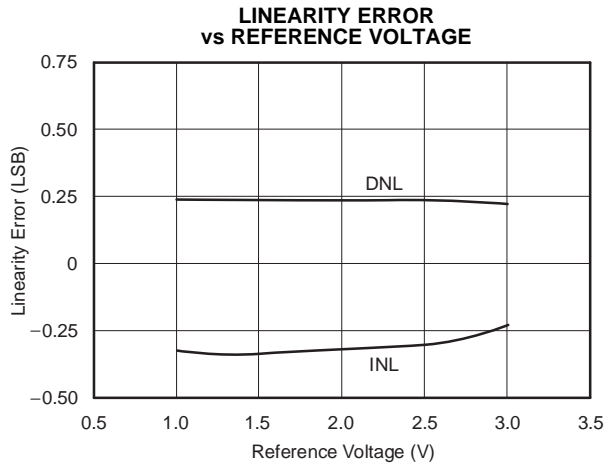
At  $T_A = +25^\circ\text{C}$ ,  $V_{REF} = +2.5\text{ V}$  unless otherwise noted.



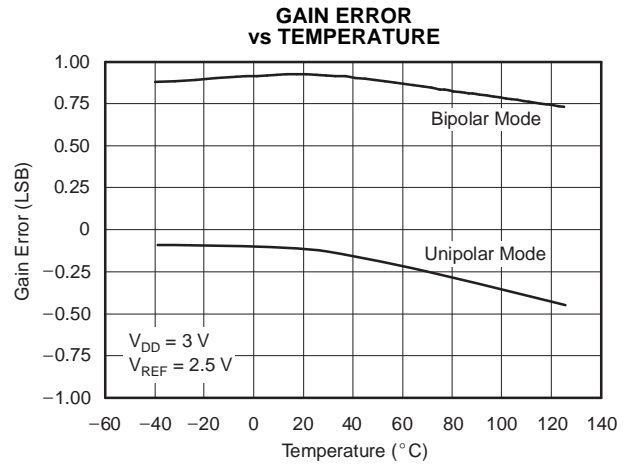
**Figure 31.**



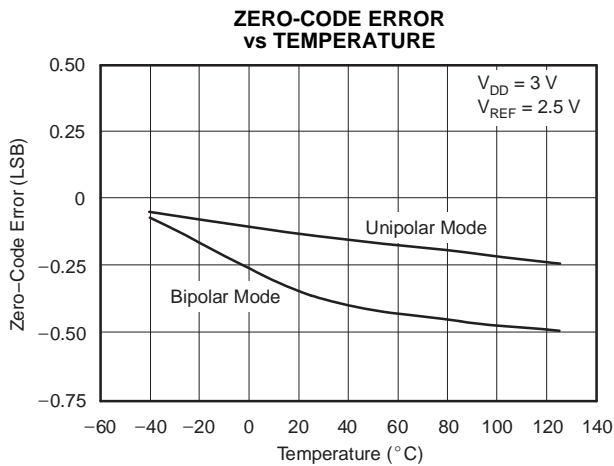
**Figure 32.**



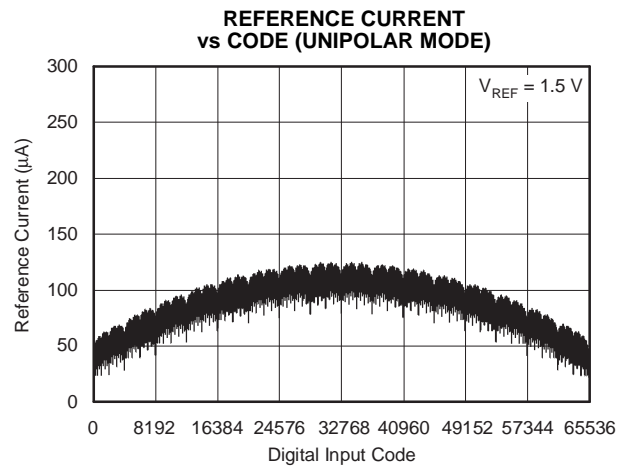
**Figure 33.**



**Figure 34.**



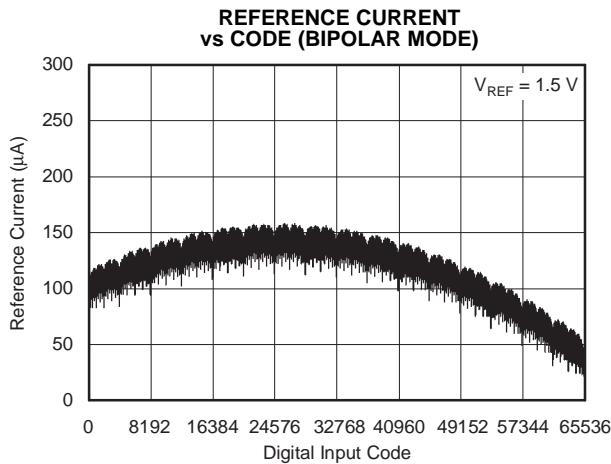
**Figure 35.**



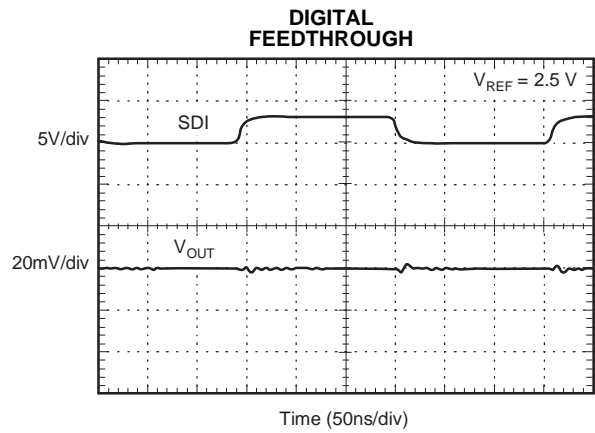
**Figure 36.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = +3\text{ V}$  (continued)**

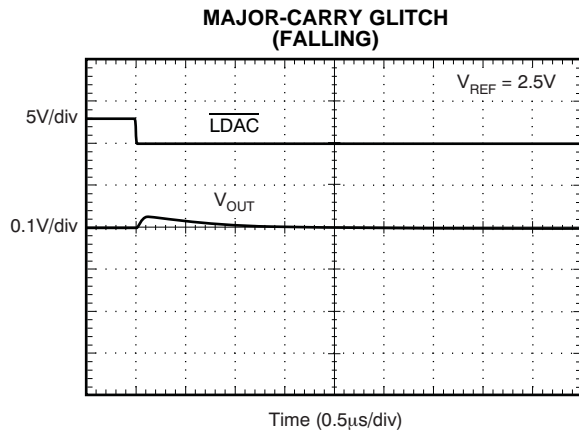
At  $T_A = +25^\circ\text{C}$ ,  $V_{REF} = +2.5\text{ V}$  unless otherwise noted.



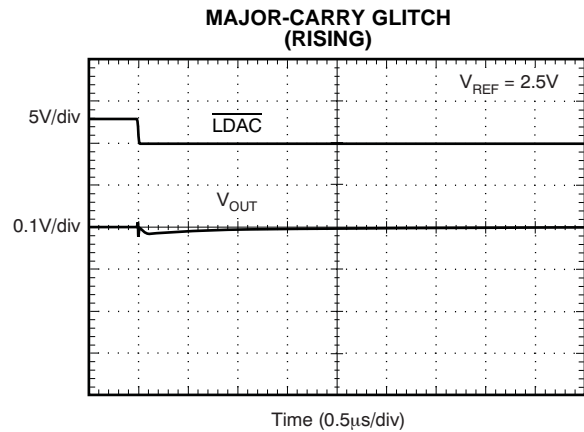
**Figure 37.**



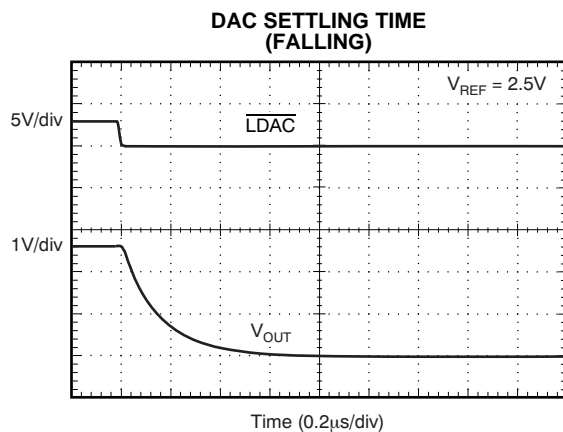
**Figure 38.**



**Figure 39.**



**Figure 40.**



**Figure 41.**



**Figure 42.**

## THEORY OF OPERATION

### GENERAL DESCRIPTION

The DAC8832 is a single, 16-bit, serial-input, voltage-output DAC. It operates from a single supply ranging from 2.7 V to 5 V, and typically consumes 5  $\mu$ A. Data are written to this device in a 16-bit word format, via an SPI serial interface. To ensure a known power-up state, the DAC8832 is designed with a power-on reset function. The DAC8832 is reset to mid-scale code. In unipolar mode, the DAC8832 is reset to  $1/2 \times V_{REF}$ , and in bipolar mode, is reset to 0 V. Kelvin sense connections for the reference and analog ground are also included.

### DIGITAL-TO-ANALOG SECTIONS

The DAC architecture consists of two matched DAC sections and is segmented. A simplified circuit diagram is shown in Figure 43. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or  $V_{REF}$ . The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

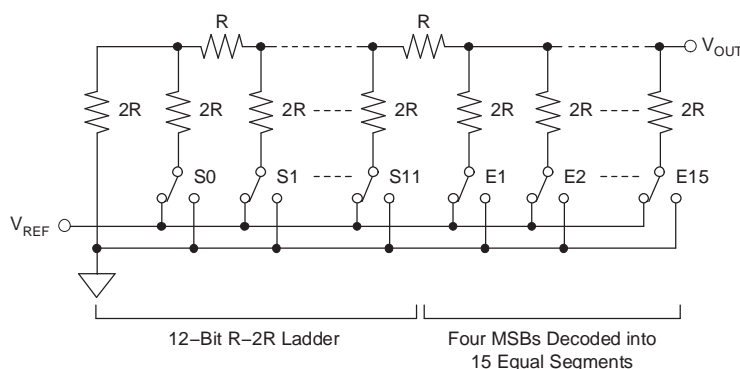


Figure 43. DAC Architecture

### OUTPUT RANGE

The output of the DAC is:

$$V_{OUT} = (V_{REF} \times Code) / 65536$$

Where *Code* is the decimal data word loaded to the DAC latch.

## POWER-ON RESET

The DAC8832 has a power-on reset function to ensure the output is at a known state upon power-up. Upon power-up, the DAC latch and input register contain mid-scale code until new data are loaded from the input serial shift register. Therefore, after power-up, the output from pin  $V_{OUT}$  is  $0.5 \times V_{REF}$  in unipolar mode, and 0 V in bipolar mode.

However, the serial register is not cleared on power-up, so its contents are undefined. When loading data initially to the device, 16 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 16 bits are loaded, the last 16 are kept; if less than 16 are loaded, bits will remain from the previous word. If the device must be interfaced with data shorter than 16 bits, the data should be padded with 0s at the LSBs.

## SERIAL INTERFACE

The digital interface is standard 3-wire connection compatible with SPI, QSPI™, Microwire™, and TI DSP interfaces, which can operate at speeds up to 50 M-bits/sec. The data transfer is framed by  $\overline{CS}$ , the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When  $\overline{CS}$  is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin  $\overline{CS}$  low. Immediately following the high-to-low transition of  $\overline{CS}$ , the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of  $\overline{CS}$  transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word,  $\overline{CS}$  must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of  $\overline{CS}$ , the last 16 bits are transferred to the input register on the rising edge of  $\overline{CS}$ . However, if  $\overline{CS}$  is not kept low during the entire 16 SCLK cycles, the data are corrupted. In this case, reload the DAC with a new 16-bit word.

The DAC8832 has an  $\overline{LDAC}$  pin allowing the DAC latch to be updated asynchronously by bringing  $\overline{LDAC}$  low after  $\overline{CS}$  goes high. In this case,  $\overline{LDAC}$  must be maintained high while  $\overline{CS}$  is low. If  $\overline{LDAC}$  is tied permanently low, the DAC latch is updated immediately after the input register is loaded (caused by the low-to-high transition of  $\overline{CS}$ ).



## APPLICATION INFORMATION

### UNIPOLAR OUTPUT OPERATION

The DAC8832 is capable of driving unbuffered loads of 60 kΩ. Unbuffered operation results in low supply current (typically 5 μA) and a low offset error. The DAC8832 can be configured to output both unipolar and bipolar voltages. Figure 44 shows a typical unipolar output voltage circuit. The code table for this mode of operation is shown in Table 1.

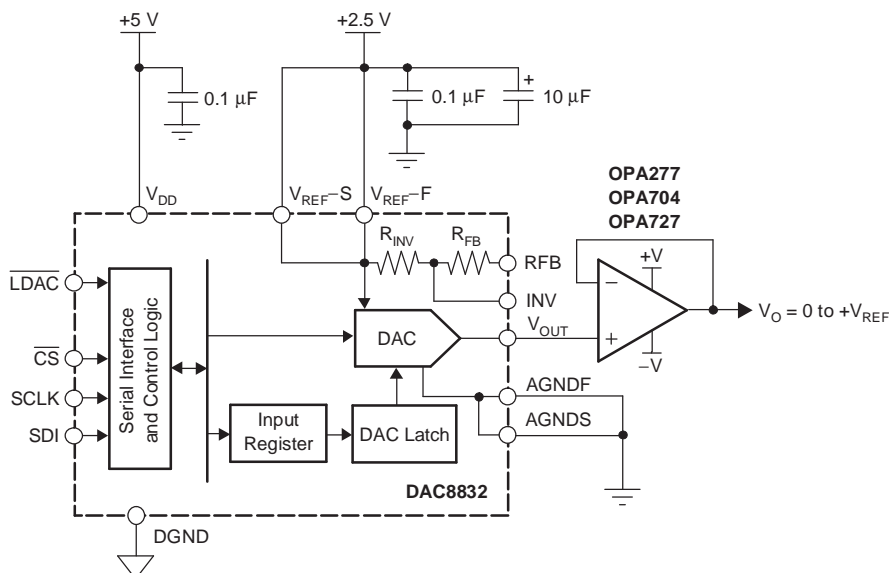


Figure 44. Unipolar Output Mode

Table 1. Unipolar Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111 1111 1111	$V_{REF} \times (65,535/65,536)$
1000	0000 0000 0000	$V_{REF} \times (32,768/65,536) = 1/2 V_{REF}$
0000	0000 0000 0001	$V_{REF} \times (1/65,536)$
0000	0000 0000 0000	0 V

Assuming a perfect reference, the worst-case output voltage may be calculated in the following equation:

**Unipolar Mode Worst-Case Output:**

$$V_{OUT\_UNI} = \frac{D}{2^{16}} \times (V_{REF} + V_{GE}) + V_{ZSE} + INL$$

Where:

$V_{OUT\_UNI}$  = Unipolar mode worst-case output

D = Code loaded to DAC

$V_{REF}$  = Reference voltage applied to part

$V_{GE}$  = Gain error in volts

$V_{ZSE}$  = Zero scale error in volts

INL = Integral nonlinearity in volts

### BIPOLAR OUTPUT OPERATION

With the aid of an external operational amplifier, the DAC8832 may be configured to provide a bipolar voltage output. A typical circuit of such an operation is shown in Figure 45. The matched bipolar offset resistors  $R_{FB}$  and  $R_{INV}$  are connected to an external operational amplifier to achieve this bipolar output swing; typically,  $R_{FB} = R_{INV} = 28\text{ k}\Omega$ .

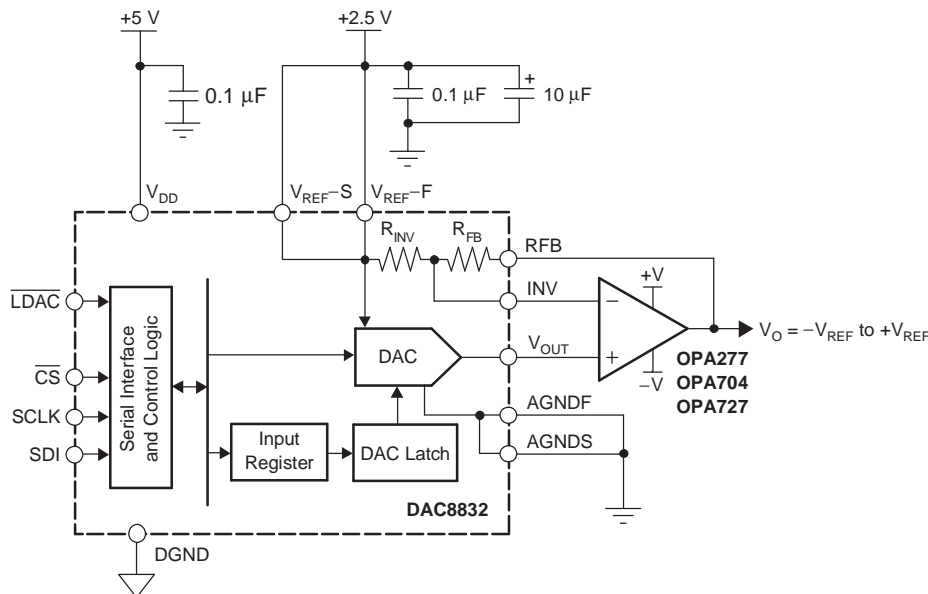


Figure 45. Bipolar Output Mode

Table 2 shows the transfer function for this output operating mode. The DAC8832 also provides a set of Kelvin connections to the analog ground and external reference inputs.

Table 2. Bipolar Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111 1111 1111 1111		$+V_{REF} \times (32,767/32,768)$
1000 0000 0000 0001		$+V_{REF} \times (1/32,768)$
1000 0000 0000 0000		0 V
0111 1111 1111 1111		$-V_{REF} \times (1/32,768)$
0000 0000 0000 0000		$-V_{REF} \times (32,768/32,768) = -V_{REF}$

Assuming a perfect reference, the worst-case output voltage may be calculated from the following equation:

**Bipolar Mode Worst-Case Output:**

$$V_{OUT\_BIP} = \frac{\left[ (V_{OUT\_UNI} + V_{OS}) (2 + RD) - V_{REF}(1 + RD) \right]}{1 + \left( \frac{2 + RD}{A} \right)}$$

Where:

- $V_{OS}$  = External operational amplifier input offset voltage
- $RD = R_{FB}$  and  $R_{IN}$  resistor matching error
- $A$  = Operational amplifier open-loop gain

## OUTPUT AMPLIFIER SELECTION

For bipolar mode, a precision amplifier should be used, supplied from a dual power supply. This provides the  $\pm V_{REF}$  output.

In a single-supply application, selection of a suitable operational amplifier may be more difficult because the output swing of the amplifier does not usually include the negative rail; in this case, AGND. This output swing can result in some degradation of the specified performance unless the application does not use codes near 0.

The selected operational amplifier needs to have low-offset voltage (the DAC LSB is 38  $\mu$ V with a 2.5 V reference), eliminating the need for output offset trims. Input bias current should also be low because the bias current multiplied by the DAC output impedance (approximately 6.25 k $\Omega$ ) adds to the zero-code error.

Rail-to-rail input and output performance are required. For fast settling, the slew rate of the operational amplifier should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but in order to minimize gain errors the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3 dB amplifier bandwidth results in a shorter effective settling time of the combined DAC and amplifier.

## REFERENCE AND GROUND

Since the input impedance is code-dependent, the reference pin should be driven from a low impedance source. The DAC8832 operates with a voltage reference ranging from 1.25 V to  $V_{DD}$ . References below 1.25 V result in reduced accuracy.

The DAC full-scale output voltage is determined by the reference. [Table 1](#) and [Table 2](#) outline the analog output voltage for particular digital codes.

For optimum performance, Kelvin sense connections are provided. If the application does not require separate force and sense lines, they should be tied together close to the package to minimize voltage drops between the package leads and the internal die.

## POWER SUPPLY AND REFERENCE BYPASSING

For accurate high-resolution performance, it is recommended that the reference and supply pins be bypassed with a 10  $\mu$ F tantalum capacitor in parallel with a 0.1  $\mu$ F ceramic capacitor.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
DAC8832IBRGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IBRGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IBRGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IBRGYTG4	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832ICRGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832ICRGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832ICRGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832ICRGYTG4	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IRGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IRGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IRGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IRGYTG4	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

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<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

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DAC8832IRGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IRGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IRGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
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**TBD:** The Pb-Free/Green conversion plan has not been defined.

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PLASTIC QUAD FLATPACK NO-LEAD



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