National Semiconductor

ADVANCE INFORMATION

DS34LV86T
3V Enhanced CMOS Quad Differential Line Receiver

General Description

The DS34LV86T is a high speed quad differential CMOS receiver that meets the requirements of both TIA/EIA-422-B and CCITT V.11. The CMOS DS34LV86T features low I_{CC} of X mA which makes it ideal for battery powered and power conscious applications.

The TRI-STATE® enables, EN, allow the device to be disabled when not in use to minimize power consumption. The dual enable scheme allows for flexibility in turning receivers on and off.

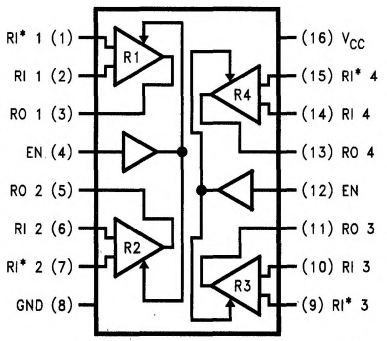
The receiver output (RO) is guaranteed to be High when the inputs are left open. The receiver can detect signals as low as ±200 mV over the common mode range of ±7V. The receiver outputs (RO) are compatible with TTL and CMOS levels.

Features

- Low power CMOS design
- Meets TIA/EIA-422-B (RS-422) and CCITT V.11 recommendation
- Receiver OPEN input failsafe feature
- Guaranteed AC parameter:
  - — Maximum receiver skew TBD
  - — Transition time TBD
- Pin compatible with DS34C86T
- Available in SOIC packaging

Connection Diagram

Dual-In-Line Package
DS34LV86T



TL/F/12644–1

Order Number DS34LV86TM or DS34LV86TN
See NS Package Number M16A or N16E

Truth Table

Enables		Inputs	Outputs
EN	**$\overline{EN}$**	**RI–RI***	**RO**
L	H	X	Z
H	L	$V_{ID} \geq V_{TH\ (Max)}$	H
H	H	$V_{ID} \leq V_{TH\ (Min)}$	L
L	L	Open	H

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)