Standard Read/Write Identification IC

Description

The e5550 is a contactless R/W-**ID**entification **IC** (IDIC®)* for general-purpose applications in the 125 kHz range. A single coil, connected to the chip, serves as the IC's power supply and bidirectional communication interface. Coil and chip together form a transponder.

The on-chip 264 bit EEPROM (8 blocks 33 bits each) can be read and written blockwise from a Base station. The blocks can be protected against overwriting. One block is reserved for setting the operation modes of the IC. Another block can contain a password to prevent unauthorized writing.

Reading occurs by damping the coil by an internal load. There are different bitrates and encoding schemes possible. Writing occurs by interrupting the RF field in a special way.

Features

- Low power, low voltage CMOS IDIC®
- Contactless power supply
- Contactless read/ write data transmission
- **R**adio **F**requency (RF): 100 to 150 kHz
- 264 bit EEPROM memory in 8 blocks of 33 bits
- 224 bits in 7 blocks of 32 bits are free for user data
- Block write protection
- Extensive protection against contactless malprogramming of the EEPROM
- Typical < 50 ms to write and verify a block
- Other options set by EEPROM:
  Bitrate [bit/s]: RF/8, RF/16, RF/32, RF/40
  RF/50, RF/64, RF/100, RF/128
  Modulation: BIN, FSK, PSK, Manchester, Biphase
  Other: Answer-On-Request (AOR), Terminator mode, Password mode

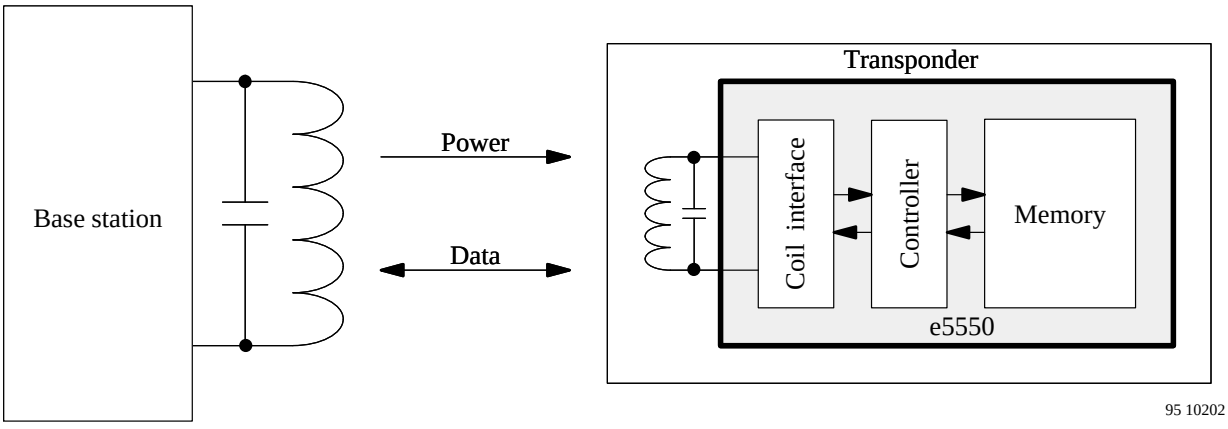


Figure 1. Transponder system example using e5550

* IDIC® stands for IDentification Integrated Circuit and is a trademark of TEMIC

Ordering Information

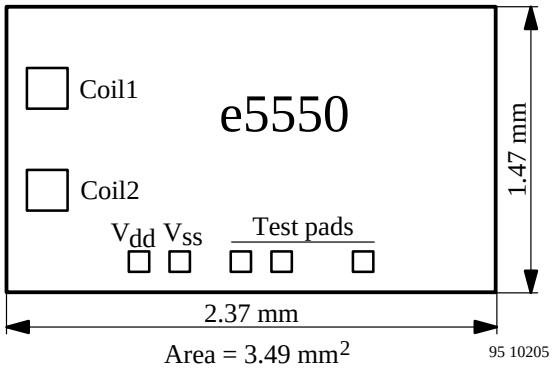
Extended Type Number	Package	Remarks
e5550F-DOW e5550F-S8	DOW SO8	All kind of modulation; RF/8, RF/16, RF/32, RF/40, RF/50, RF/64, RF/100 and RF/128 *) Default programmed: Manchester Modulation, RF/32, MAXBLK = 2

*) see page 4

Pads

Name	Pad Window	Function
Coil1	136 × 136 µm^2	1st coil pad
Coil2	136 × 136 µm^2	2nd coil pad
V_{dd}	78 × 78 µm^2	Positive supply voltage
V_{ss}	78 × 78 µm^2	Negative supply voltage (gnd)
Test1	78 × 78 µm^2	Test pad
Test2	78 × 78 µm^2	Test pad
Test3	78 × 78 µm^2	Test pad

Chip Dimensions



Note: For e5550F–SO8 pin 1 of the SO8–package is connected to Coil2 and pin 8 to Coil1. Pins 2 to 7 have to be open. They are not specified for applications.

e5550 Building Blocks

Analog Front End (AFE)

The AFE includes all circuits which are directly connected to the coil. It generates the IC's power supply and handles the bidirectional data communication with the reader unit. It consists of the following blocks:

- Rectifier to generate a dc supply voltage from the ac coil voltage
- Clock extractor
- Switchable load between Coil1/ Coil2 for data transmission from the IC to the reader unit (read)
- Field gap detector for data transmission from the reader unit into the IC (write)

Controller

The main controller has following functions:

- Load mode register with mode data from EEPROM block 0 after power-on and also during reading
- Control memory access (read, write)
- Handle write data transmission and the write error modes
- The first two bits of the write data stream are the OP-code. There are two valid OP-codes (standard and stop) which are decoded by the controller.
- In password mode, the 32 bits received after the OP-code are compared with the stored password in block 7.

Bitrate Generator

The bitrate generator can deliver the following bitrates:
rf/8 – rf/16 – rf/32 – rf/40 – rf/50 – rf/64 – rf/100 – rf/128

Write Decoder

Decode the detected gaps during writing. Check if write data stream is valid.

Test Logic

Test circuitry allows rapid programming and verification of the IC during test.

HV Generator

Voltage pump which generates ~18 V for programming of the EEPROM.

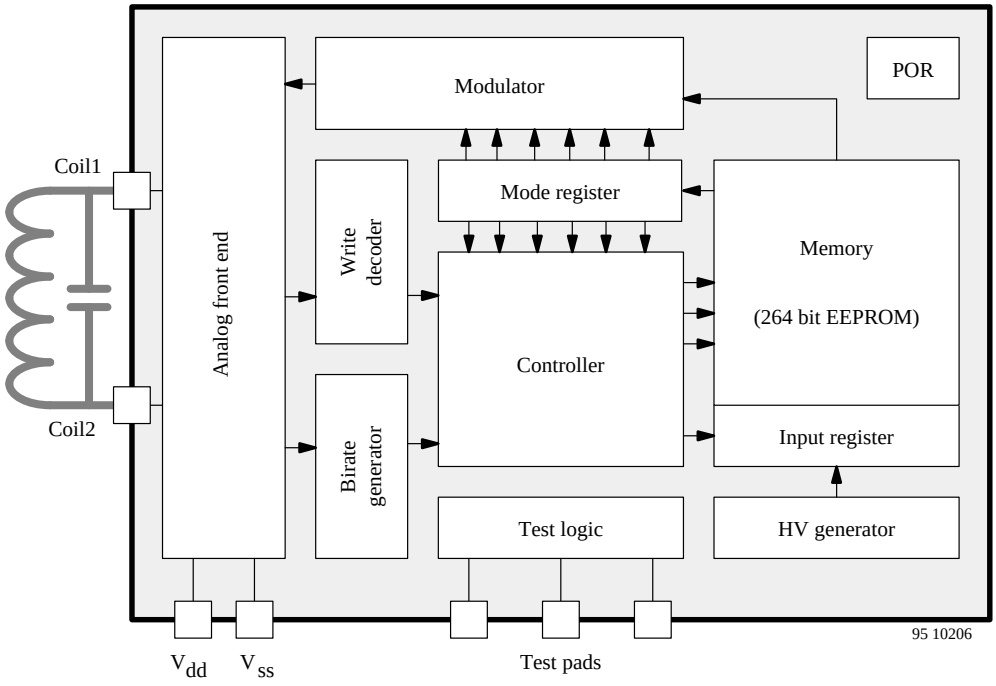


Figure 2. Block diagram e5550

Power-On Reset (POR)

The power-on reset is a delay reset which is triggered when supply voltage is applied.

Mode Register

The mode register stores the mode data from EEPROM block 0. It is continually refreshed at the start of every block. This increases the reliability of the device (if the originally loaded mode information is false, it will be corrected by subsequent refresh cycles).

Modulator

The modulator consists of several data encoders in two stages, which may be freely combined to obtain the desired modulation. The basic types of modulation are:

- PSK: phase shift: 1) every change; 2) every ‘1’; 3) every rising edge (carrier: fc/2, fc/4 or fc/8)
- FSK: 1) f1 = rf/8 f2 = rf/5; 2) f1 = rf/8, f2 = rf/10
- Manchester: rising edge = H; falling edge = L
- Biphase: every bit creates a change, a data ‘H’ creates an additional mid-bit change

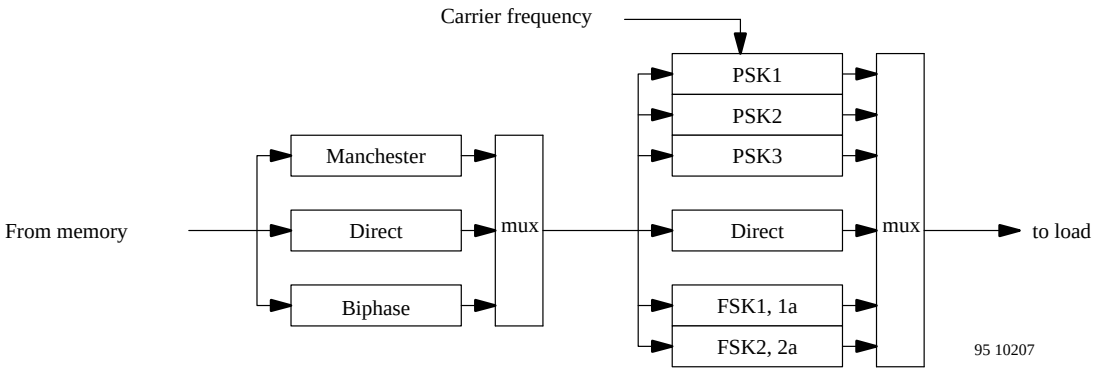


Figure 3. Modulator block diagram

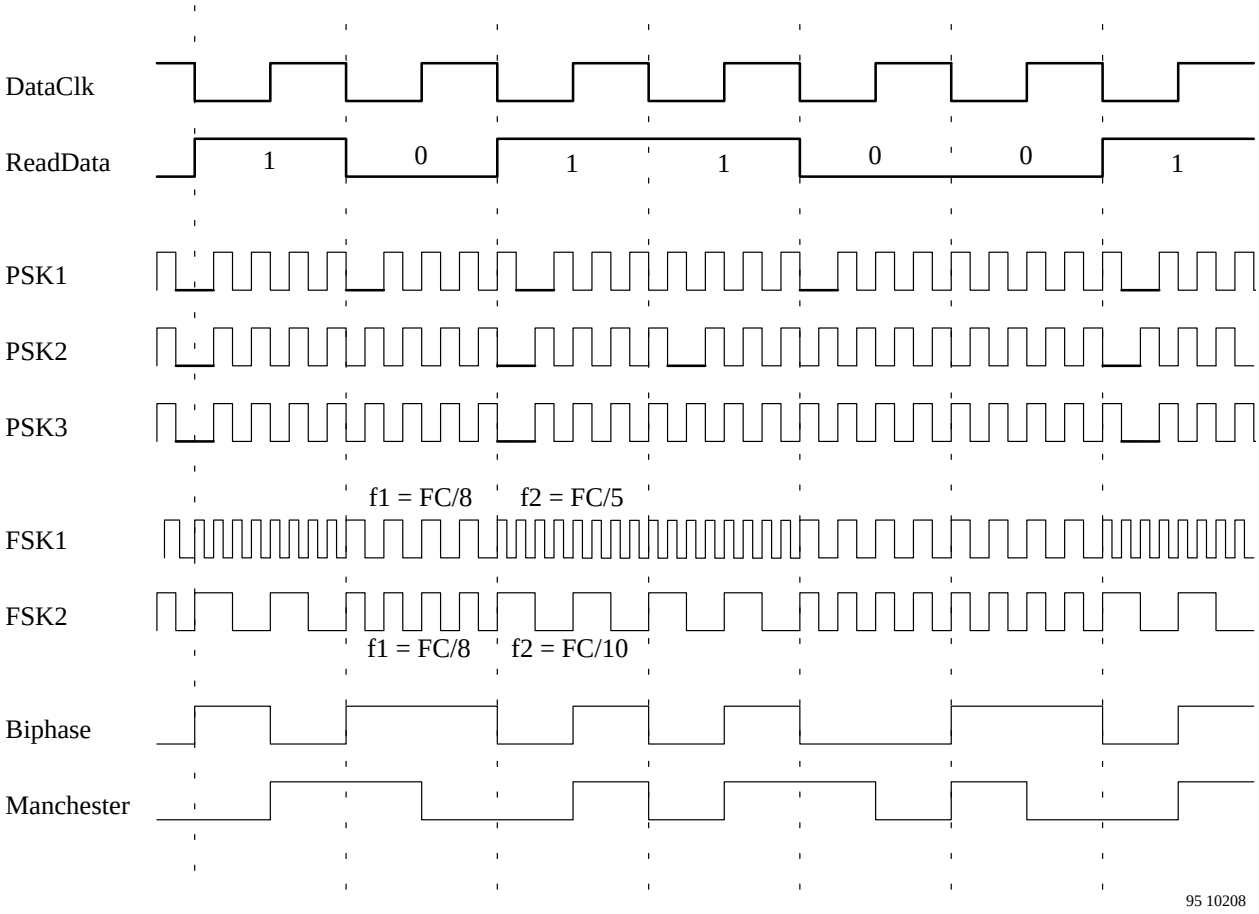


Figure 4. Types of modulation

Note: The following modulation type combinations will not work:

- Stage1 Manchester or Biphase, stage2 psk2, at any psk carrier frequency (because the first stage output frequency is higher than the second stage strobe frequency)
- Stage1 Manchester or Biphase and stage2 psk with bitrate = rf/8 and psk carrier frequency = rf/8 (for the same reason as above)
- Any stage1 option with any psk for bitrates rf/50 or rf/100 if the psk carrier frequency is not an integer multiple of the bitrate (e.g., br = rf/50, pskcf = rf/4, because 50/4 = 12.5). This is because the psk carrier frequency must maintain constant phase with respect to the bit clock.

Memory

The memory of the e5550 is a 264 bit EEPROM, which is arranged in 8 blocks of 33 bits each. All 33 bits of a block, including the lock bit, are programmed simultaneously. The programming voltage is generated on-chip.

Block 0 contains the mode data, which are not normally transmitted (see figure 6).

Block 1 to 6 are freely programmable. Block 7 may be used as a password. If password protection is not required, it may be used for user data.

Bit 0 of every block is the lock bit for that block. Once locked, the block (including the lockbit itself) cannot be field-reprogrammed.

Data from the memory is transmitted serially, starting with block 1, bit 1, up to block ‘MAXBLK’, bit 32. ‘MAXBLK’ is a mode parameter set by the user to a value between 0 and 7 (if maxblk=0, only block 0 will be transmitted).

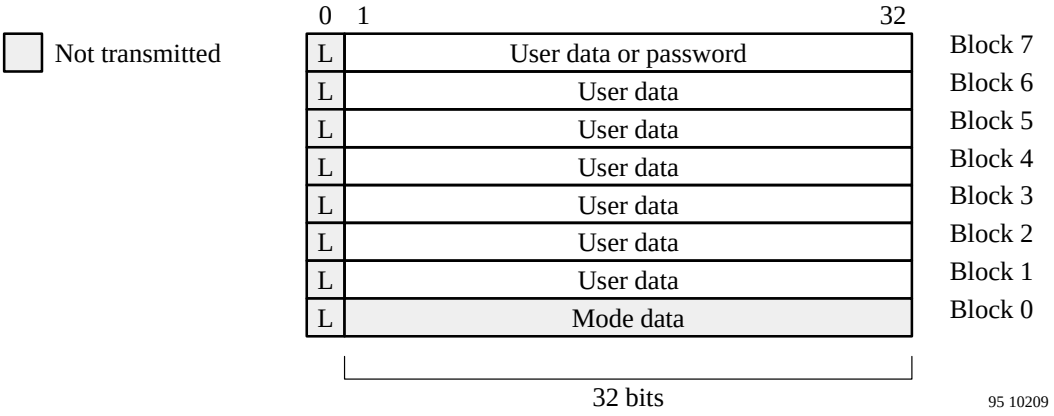


Figure 5. Memory map

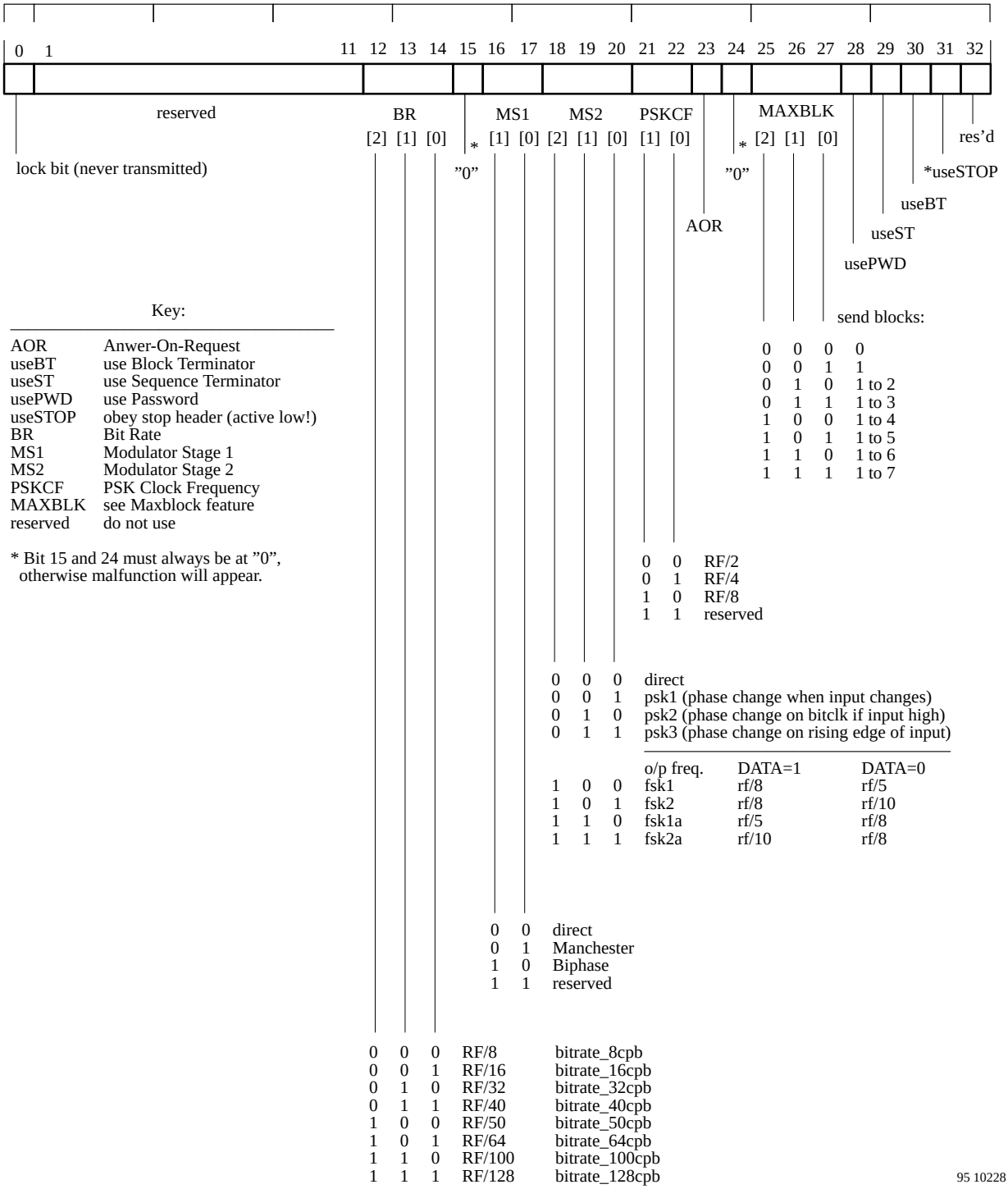


Figure 6. Memory map of block 0

Operating the e5550

General

The basic functions of the e5550 are: **supply** IC from the coil, **read** data from the EEPROM to the reader, **write** data into the IC and **program** these data into the EEPROM. Several **errors** can be detected to protect the memory from being written with the wrong data (see figure 20).

Supply

The e5550 is supplied via a tuned LC circuit which is connected to the Coil1 and Coil2 pads. The incoming RF (actually a magnetic field) induces a current into the coil which powers the chip. The on-chip rectifier generates the dc supply voltage (V_{dd}, V_{ss} pads). Overvoltage protection prevents the IC from damage due to high-field strengths. (Depending on the coil, the open-circuit voltage across the LC circuit can reach more than 100 V). The first occurrence of RF triggers a power-on reset pulse, ensuring a defined start-up state.

Read

Reading is the default mode after power-on reset. It is done by switching a load between the coil pads on and off. This changes the current through the IC coil, which can be detected from the reader unit.

Start-Up

The many different modes of the e5550 are activated after the first readout of block 0. The modulation is off while block 0 is read. After this set-up time of 256 field clock periods, modulation with the selected mode starts.

Read Datastream

The first block transmitted is block 1. When the last block is reached, reading restarts with block 1. Block 0, which contains mode data, is normally never transmitted. However, the mode register is continuously refreshed with the contents of EEPROM block 0.

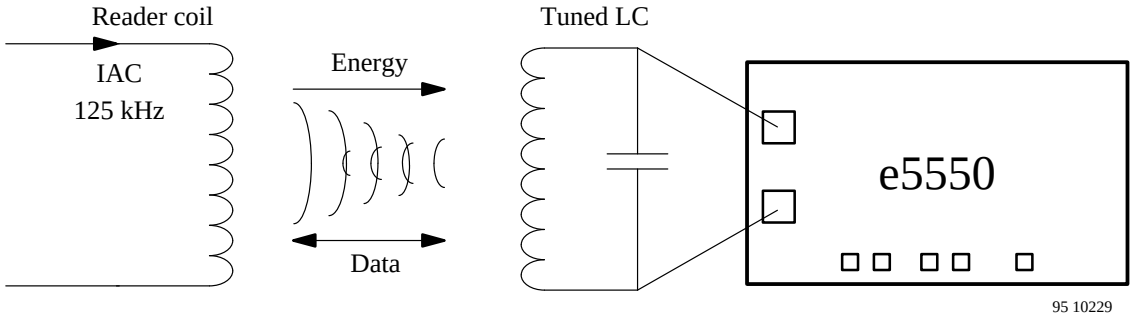


Figure 7. Application circuit

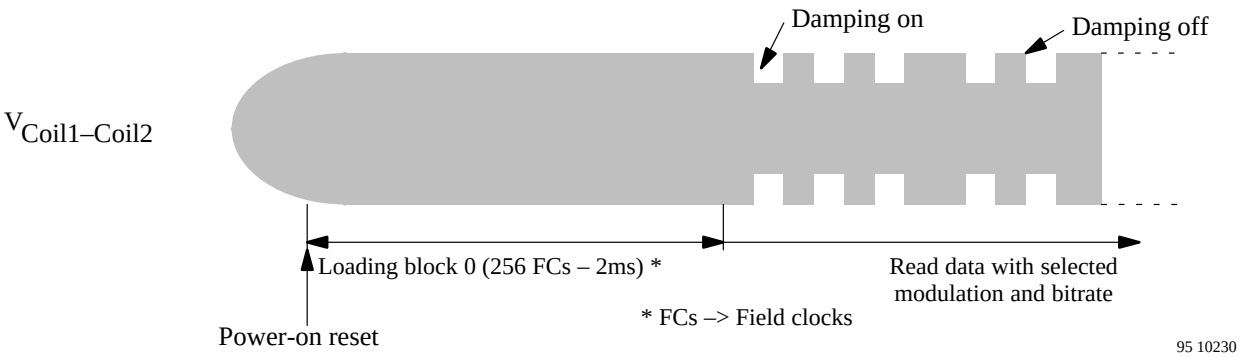


Figure 8. Voltage at Coil1/Coil2 after power-on

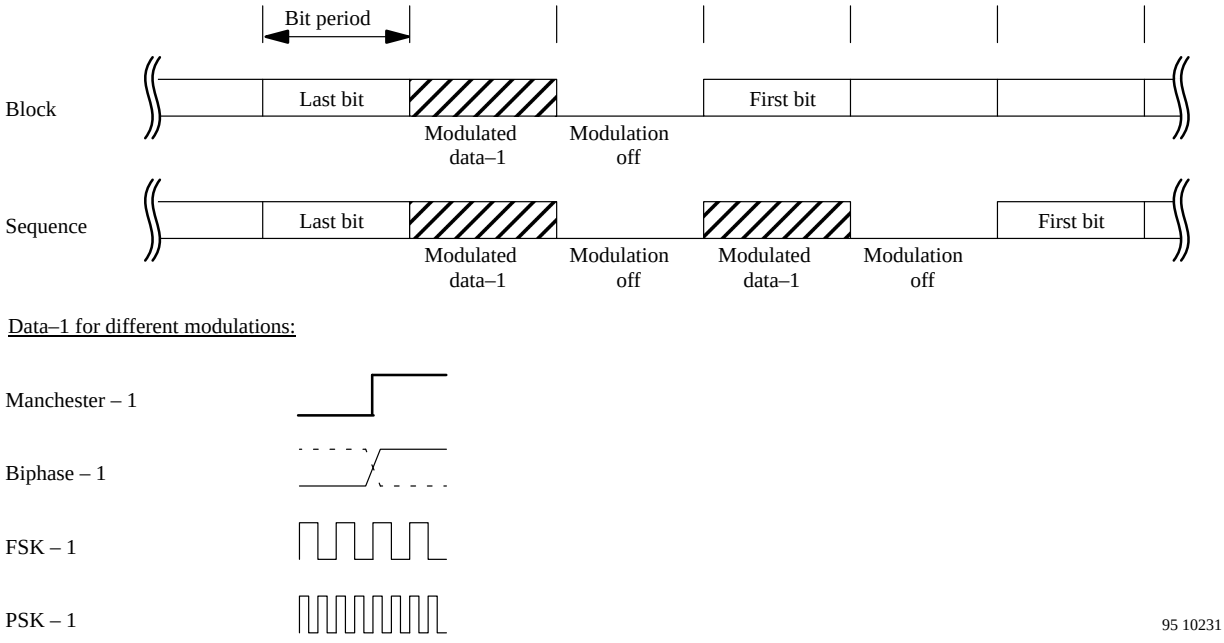


Figure 9. Terminators

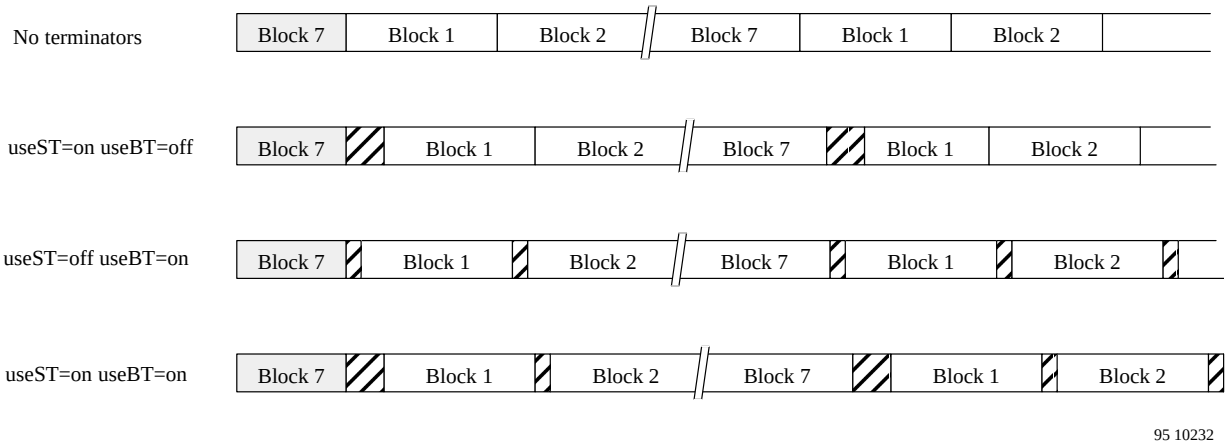


Figure 10. Read data streams and terminators

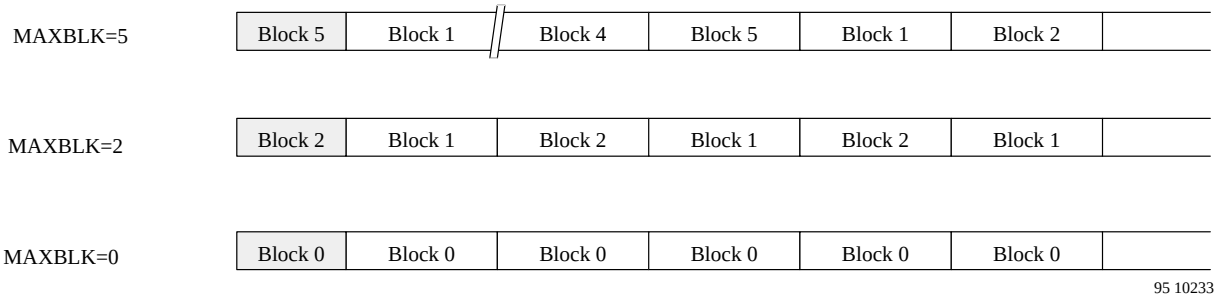


Figure 11. MAXBLK examples

Terminators

The terminators are (optionally selectable) special damping patterns, which may be used to synchronize the reader. There are two types available; a block terminator which precedes every block, and a sequence terminator which always follows the last block.

The sequence terminator consists of two consecutive block terminators. The terminators may be individually enabled with the mode bits useST (sequence terminator enable) or useBT (block terminator enable).

Note: It is not possible to include a sequence terminator in a transmission where MAXBLK = 0.

Direct Access

Direct access is a feature for reading out an individual block by sending the write OP-code, the lock-bit and the 3-bit address. This does not work in password-mode.

Modulation and Bitrate

There are two modulators in the e5550 (see figure 3) whose mode can be selected using the appropriate bits in block 0 (MS1[1:0] and MS[2:0]). Also the bitrate can be selected using BR[2:0] in block 0. These options are described in detail in figure 6.

Maxblock Feature

If it is not necessary to read all six user data blocks; the MAXBLK field in block 0 can be used to limit the number of blocks read. For example, if MAXBLK = 4, the e5550 repeatedly reads and transmits only blocks 1 to 4. If MAXBLK is set to ‘0’, block 0 (which is normally hidden) is read.

Answer-On-Request (AOR) Mode

When the AOR bit is set, the IC does **not** start modulation after reading block 0. It waits for a valid signal from the reader before modulation is enabled. This is used for applications where ‘tag is here’ information is supplied by some additional means (e.g., turning the key which contains a tag). Therefore, in AOR mode, it is not possible to read the tag by simply applying an RF field. The activation pattern (request), which re-enables modulation, is a standard OP-code followed by a valid password. If the usePWD bit is not set, any 32 valid bits will do in place of the password. The IC will remain active until the power is cycled, or a stop OP-code is sent if use STOP is active (low).

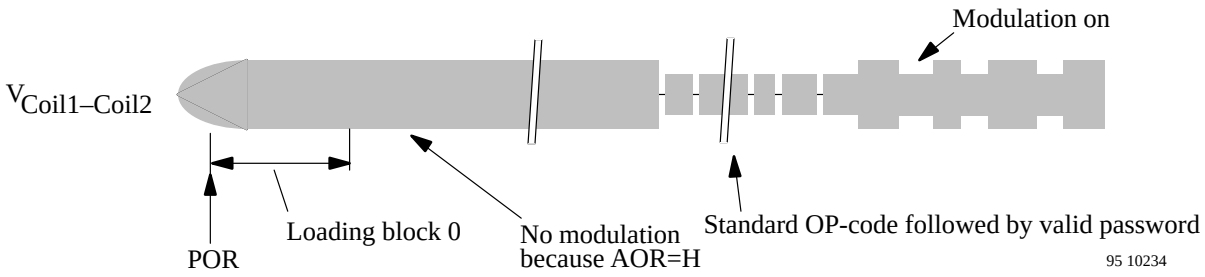


Figure 12. Answer-on-request mode

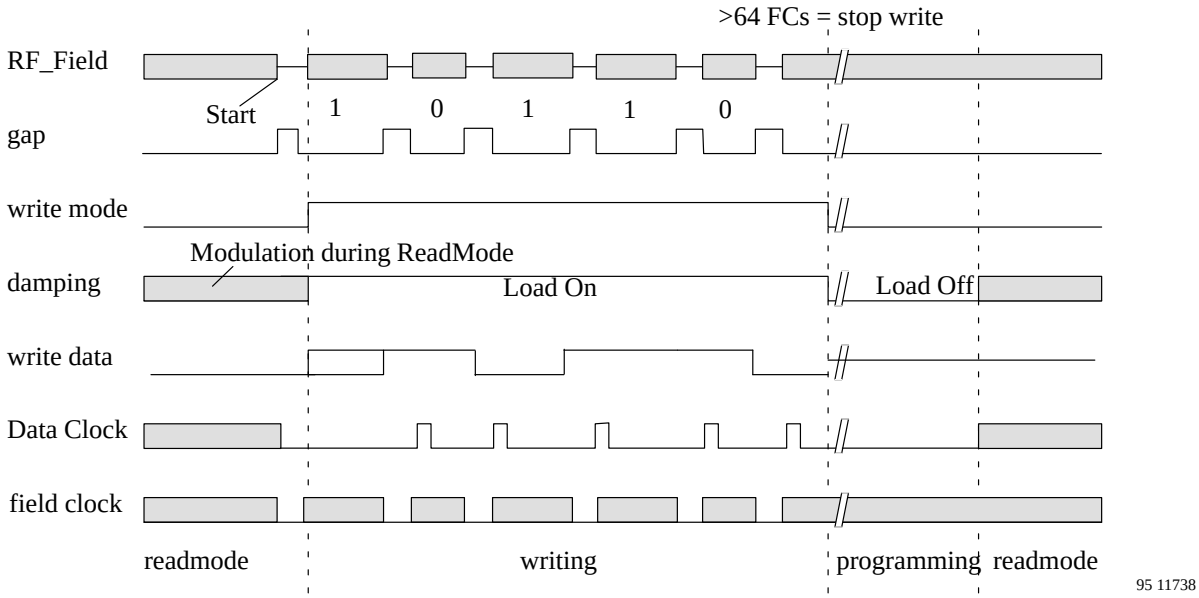


Figure 13. Signals during writing

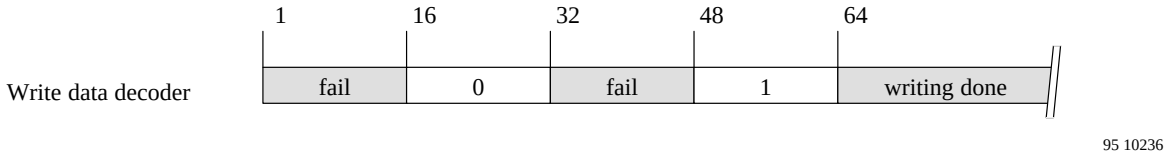


Figure 14. Write data decoding schemes

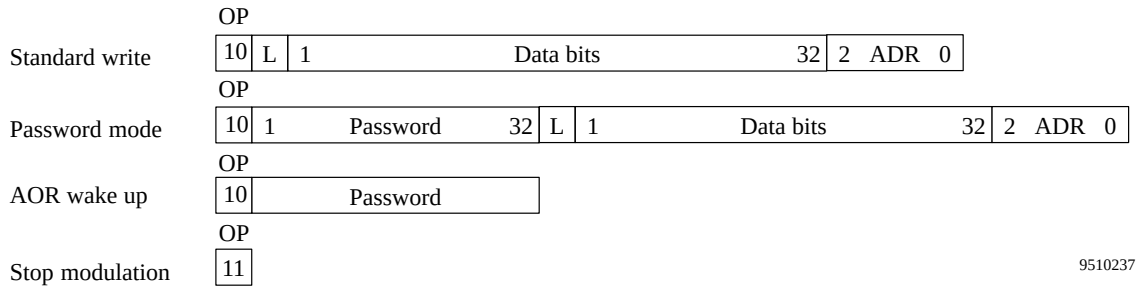


Figure 15. Legal write data sequences

Write

Writing data into the IC occurs via the TEMIC write method. It is based on interrupting the RF field with short gaps. The time between two gaps encodes the ‘0/1’ information to be transmitted.

Start Gap

The first gap is the start gap which triggers write mode. In write mode, the damping is permanently enabled which eases gap detection. The start gap may need to be longer than subsequent gaps in order to be detected reliably.

A start gap will be detected at any time after block 0 has been read (field-on plus approximately 2 ms).

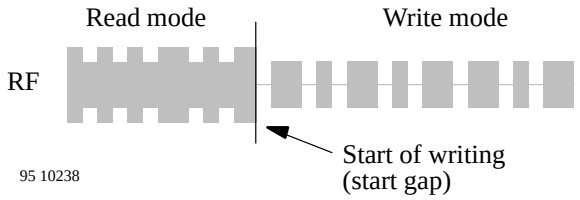


Figure 16. Start of writing

Decoder

The duration of the gaps is usually 50 to 150 µs. The time between two gaps is nominally 24 field clocks for a '0' and 56 field clocks for a '1'. When there is no gap for more than 64 field clocks after previous gap, the IDIC exits write mode; it starts with programming if the correct number of valid bits were received.

If there is a gap fail – i.e., one or more of the gaps was not a valid '0' or '1' – the IC does not program, but enters read mode beginning with block 1.

Writing Data into the e5550

The e5550 expects always to receive a OP-code first. This OP-code may be followed by different information:

- Standard writing needs only the OP-code, the lock bit, the 32 data bits and the block address.
- Writing with usePWD set requires a valid password between OP-code and address/data bits.
- In AOR mode with use PWD, OP-code and a valid password are necessary to enable modulation.
- A special OP-code is used to silence the e5550 (disable damping until power is cycled).

Note: The data bits are read in the same order as written.

OP-Codes

There are two valid OP-codes. If the OP-code is invalid, the e5550 starts read mode beginning with block 1 after the last gap.

The standard OP-code ('10') precedes all write operations. The stop OP-code ('11') is used to stop the IC until a power-on reset occurs. This feature can be used to have a steady RF field where single transponders are collected one by one. Each IC is read and than disabled, so that it does not interfere with the next IC.

Note: The stop OP-code should contain only the two OP-code bits to disable the IC. Any additional data sent will not be ignored, and the IC will not stop modulation.

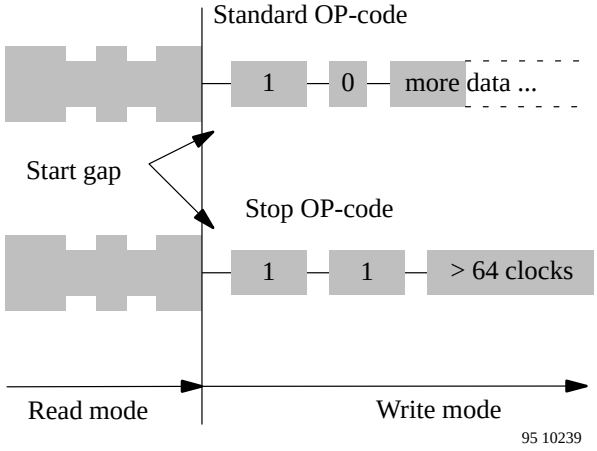


Figure 17. OP-codes

Password

When password mode is on (usePWD = 1), the first 32 bits after the OP-Code are regarded as the password. They are compared bit-by-bit with the contents of block 7, starting at bit 1. If the comparison fails, the IC will not program the memory, but restart in read mode at block 1 once writing has completed.

Notes:

- If usePWD is not set, but the IC receives a write datastream containing any 32 bits in place of a password, the IC will enter programming mode.
- The first 4 bits of the password have to be ”0”.
- In password mode, MAXBLK should be set to a value below 7 to prevent the password from being transmitted by the e5550.
- Every transmission of 2 OP-code bits plus 32 bits password plus 3 bits address plus 33 bits data (= 70 bits) needs about 35 ms. Testing all 2^{32} possible combinations (about 4.3 billion) takes about 40,000 h, or over four years. This is a sufficient password protection for a general-purpose IDIC.

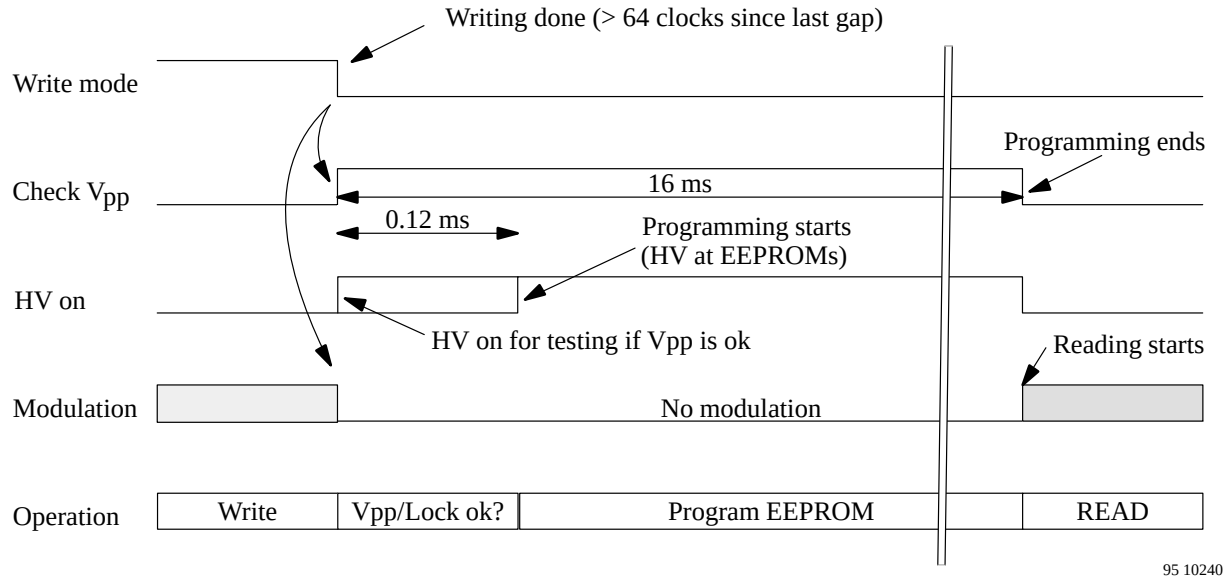


Figure 18. Programming

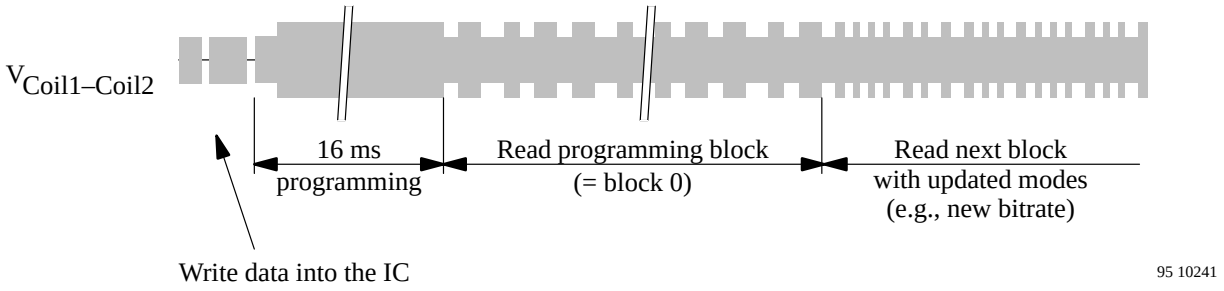


Figure 19. Coil voltage after programming of Block 0

Programming

When all necessary information has been written to the e5550, programming may proceed. There is a 32-clock delay between the end of writing and the start of programming. During this time, Vpp – the EEPROM programming voltage – is measured and the lock bit for the block to be programmed is examined. Further, Vpp is continually monitored throughout the programming cycle. If at any time Vpp is too low, the chip enters read mode immediately.

The programming time is 16 ms.

After programming is done, the e5550 enters read mode, starting with the block just programmed. If either block or sequence terminators are enabled, the block is preceded by a block terminator. If the mode register (block 0) has been reprogrammed, the new mode will be activated **after** the just-programmed block has been transmitted using the **old** mode.

Error Handling

Several error conditions can be detected to ensure that only valid bits are programmed into the EEPROM. There are two error types, which lead to two different actions.

Errors during writing

There are four detectable errors which could occur during writing data into the e5550:

- Wrong number of field clocks between two gaps
- The OP-Code is neither the standard OP-Code nor the stop OP-Code
- Password mode is active but the password does not match the contents of block 7
- The number of bits received is incorrect;
  valid bit counts are
  - Standard write 38 bits (usePWD not set)
  - Password write 70 bits (usePWD set)
  - AOR request 34 bits
  - Stop command 2 bits

If any of these four conditions are detected, the IC starts read mode immediately after leaving write mode. Reading starts with block 1.

Errors During Programming

If writing was successful, the following errors could prevent programming:

- The lock bit of the addressed block is set
- V_{PP} is too low

In these cases, programming stops immediately. The IC reverts to read mode, starting with the currently addressed block.

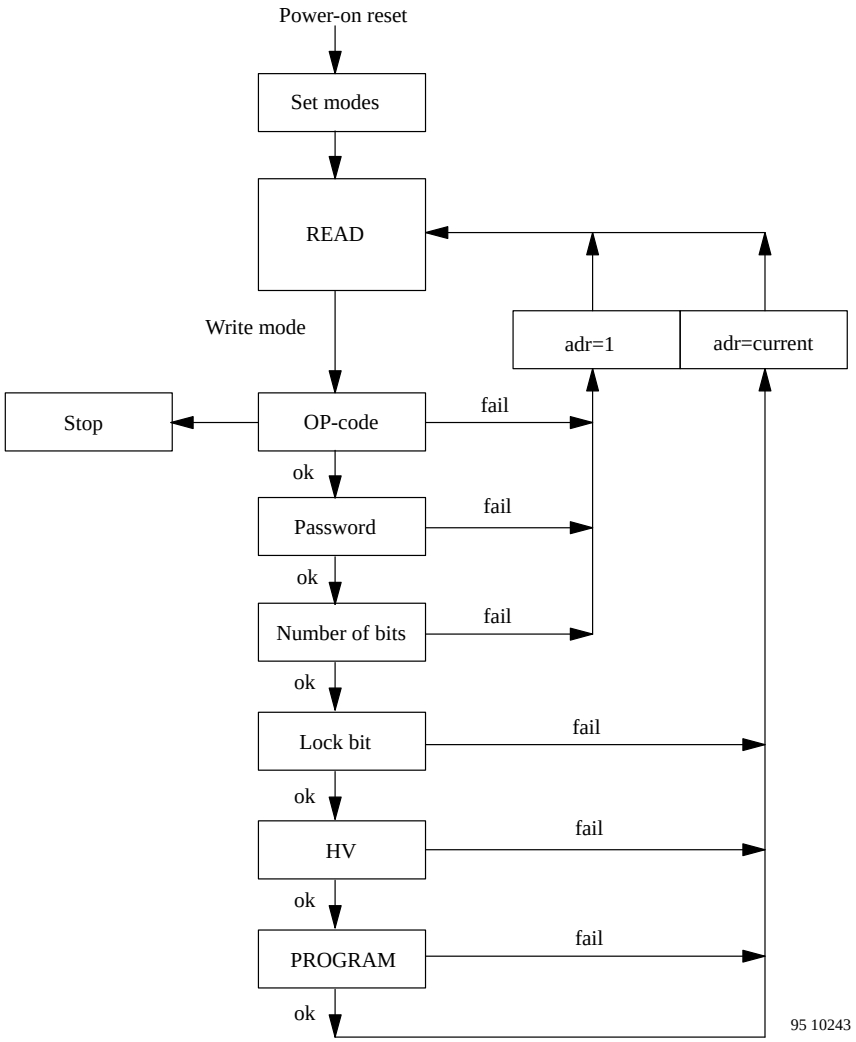


Figure 20. Functional diagram of the e5550

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Maximum DC current into COIL1/COIL2	I_{coil}	10	mA
Maximum AC current into COIL1/COIL2 f = 125 kHz	$i_{coil\ pp}$	20	mA
Power dissipation (dice) 1)	P_{tot}	100	mW
Electro-static discharge maximum to MIL-Standard 883 C method 3015	V_{max}	1000	V
Operating ambient temperature range	T_{amb}	–20 to +70	°C
Storage temperature range 2)	T_{stg}	–40 to +125	°C
Maximum assembly temperature for less than 5 min 3)	T_{sld}	+150	°C

Notes: 1) Free-air condition, time of application: 1 s
2) Data retention reduced
3) Assembly temperature of 150°C for less than 5 minutes does not affect the data retention.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

Operating Characteristics

T_{amb} = 25°C; f_{RF} = 125 kHz, reference terminal is V_{SS}

Parameters	Comments	Symbol	Min.	Typ.	Max.	Unit
RF frequency range		f_{RF}	100	125	150	kHz
Supply current	Read and write over the full temperature range	I_{DD}		5	7.5	µA
	Programming over the full temperature range	I_{DD}		100	200	µA
Clamp voltage	10 mA current into Coil1/2	V_{cl}	9.5		11.5	V
Programming voltage	From on-chip HV-Generator	V_{pp}	16		20	V
Programming time		t_P		18		ms
Startup time		$t_{startup}$			4	ms
Data retention	1)	$t_{retention}$	10			Years
Programming cycles	1)	n_{cycle}	100 000			
Supply voltage	Read and write	V_{DD}			1.6	V
Supply voltage	Read-mode, T = – 30°C	V_{DD}			2.0	V
Coil voltage	Read and write	$V_{coil\ pp}$			6.0	V
Coil voltage	Programming, RF field not damped	$V_{coil\ pp}$			7.0	V
Damping resistor		R_D		300		Ω

Note
1) Since EEPROM performance may be influenced by assembly and packaging, we can confirm the parameters for dow (= die-on-wafer) and ICs assembled in standard package.

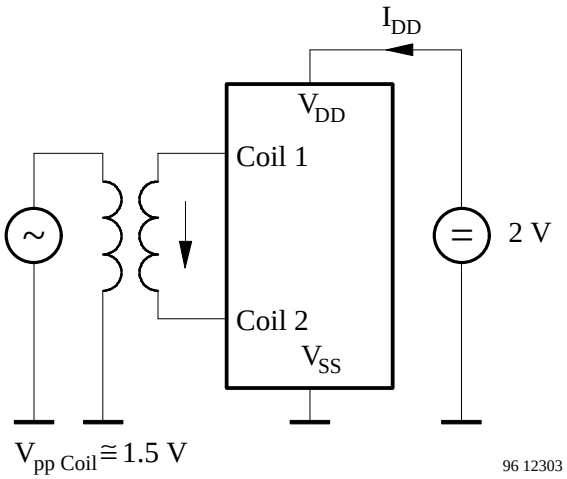


Figure 21. Measurement setup for I_{DD}

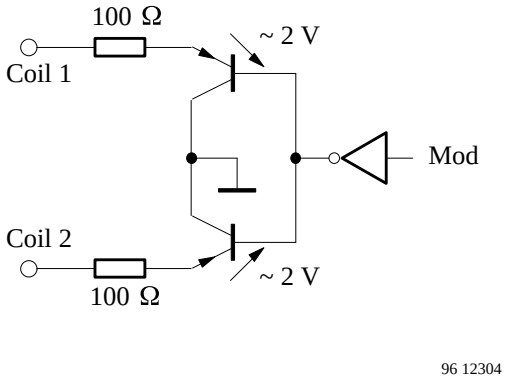


Figure 22. Simplified damping circuit

Application Example

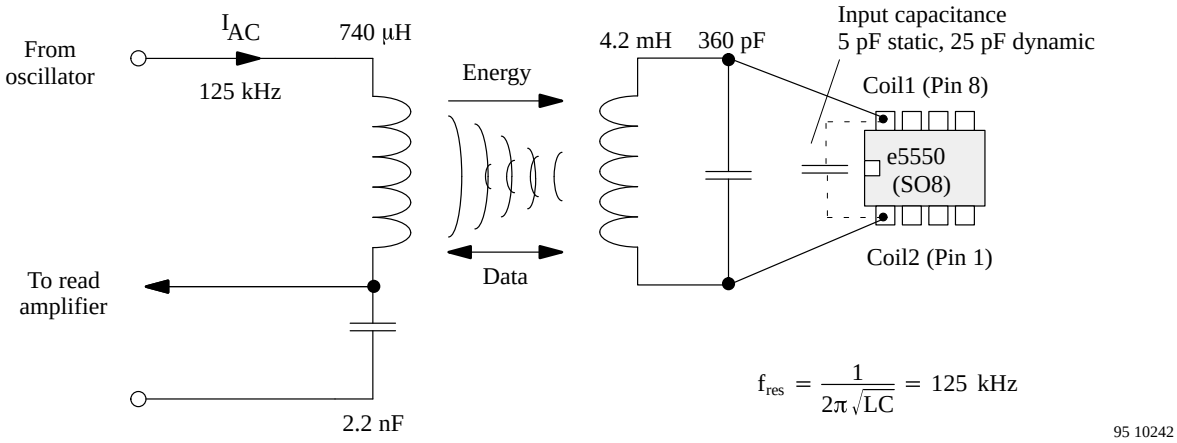


Figure 23. Typical application circuit

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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