261

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7661C
100V Full Bridge Driver

Features
- 100V High Side Voltage
- Programmable Delay
- Direct Coupled
- No Start Up Ambiguity
- Rail to Rail Output
- 1 MHz Operation
- 1.0 Amp Peak Current
- Improved Response Times
- Matched Rise and Fall Times
- Low Supply Current
- Low Output Impedance
- Low Input Capacitance

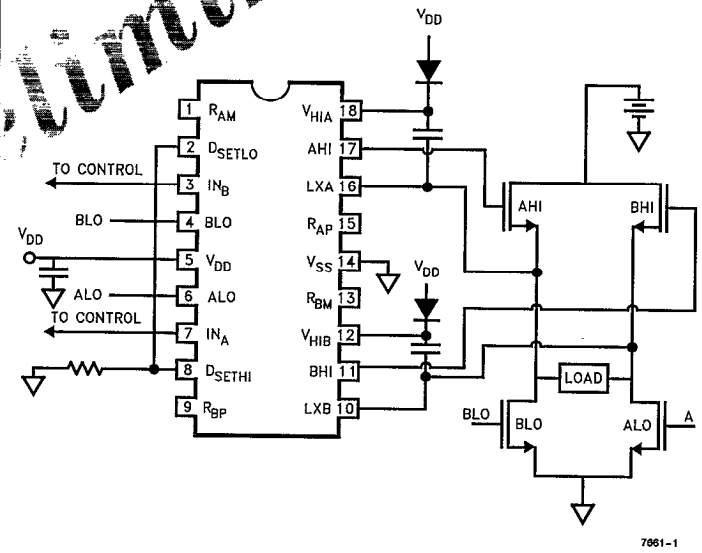
Applications
- Uninterruptible Power Supplies
- Distributed Power Systems
- IGBT Drive
- DC-DC Converters
- Motor Control
- Power MOSFET Drive
- Switch Mode Power Supplies

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7661CN	−40°C to +85°C	18-Pin P-DIP	MDP0031
EL7661CS	−40°C to +85°C	18-Pin SOIC	MDP0027

General Description
The EL7661 provides a low cost solution to many full bridge applications. The EL7661 is DC coupled so that there are no start up problems associated with AC coupled schemes. A single resistor from the D_{SET} pins to GND provides "dead time" programmability. Shorting the D_{SET} pins to V_{DD} gives the minimum delay (~100 ns).

Connection Diagram



EL7661C

Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{HI} to GND)	100V	Storage Temperature Range	−65°C to +150°C
Supply (V_{DD} to GND)	18V	Ambient Operating Temperature	0°C to +75°C
Input Pins	−0.3V below GND, +0.3V above V_{DD}	Power Dissipation SOIC	910 mW
		PDIP	1400 mW
Operating Junction Temperature	125°C		
Combined Peak Output Current	4A		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (T_A = 25C, V_{DD} = 15V, C_{LOAD} = 1000 pF, unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input/Output							
V_{IL}	Logic "1" Input Voltage		3.0			I	V
I_{IH}	Logic "1" Input Current			0.1	10.0	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current			0.1	10.0	I	µA
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		5.0	10.0	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		5.0	10.0	I	Ω
I_{PK}	Peak Output Current			1.0		IV	A
I_{DC}	Continuous Output Current Source/Sink		100.0			IV	mA
Power Supply							
I_{DD}	Supply Current into V_{DD}	R_{SET} = 5.1k Inputs = 15V			10.0	I	mA
I_{HIA}	Supply Current into V_{HIA}				4.0	I	mA
I_{HIB}	Supply Current into V_{HIB}				4.0	I	mA
V_{DD}	Operating Voltage		4.5		15.0	I	V

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AC Electrical Characteristics (T_A = 25C, V_{DD} = 15V, C_{LOAD} = 1000 pF, unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	 40.0	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	 40.0	IV	ns
$t_{D\ ON\ HI}$	High Side Turn On Delay Time	D_{SETHI} = V_{DD} D_{SETHI} = 5.1k D_{SETHI} = 400k	50.0 50.0 1000.0	100.0 100.0 1100.0	150.0 150.0 1200.0	IV I I	ns
$t_{D\ ON\ LO}$	Low Side Turn On Delay Time	D_{SETLO} = V_{DD} D_{SETLO} = 5.1k D_{SETLO} = 400k	50.0 50.0 1000.0	100.0 100.0 1100.0	150.0 150.0 1200.0	IV I I	ns
$t_{D\ OFF\ HI}$	High Side Turn Off Delay Time	D_{SET} = V_{DD}		100.0	150.0	IV	ns
$t_{D\ OFF\ LO}$	Low Side Turn Off Delay Time	D_{SET} = V_{DD}		100.0	150.0	IV	ns
$t_{D\ MISMATCH}$	High to Lo Side Turn On Delay Mismatch	D_{SET} = 400k			+ /-10.0	I	%