



3.3V CMOS REGISTERED ADDRESS LINE DRIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16345

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP, and 0.40mm pitch TVSOP packages
- Extended commercial range of - 40°C to + 85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16345:

- High Output Drivers: ±24mA
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems
- High Speed Synchronous DRAM Modules
- PC Motherboards

DESCRIPTION:

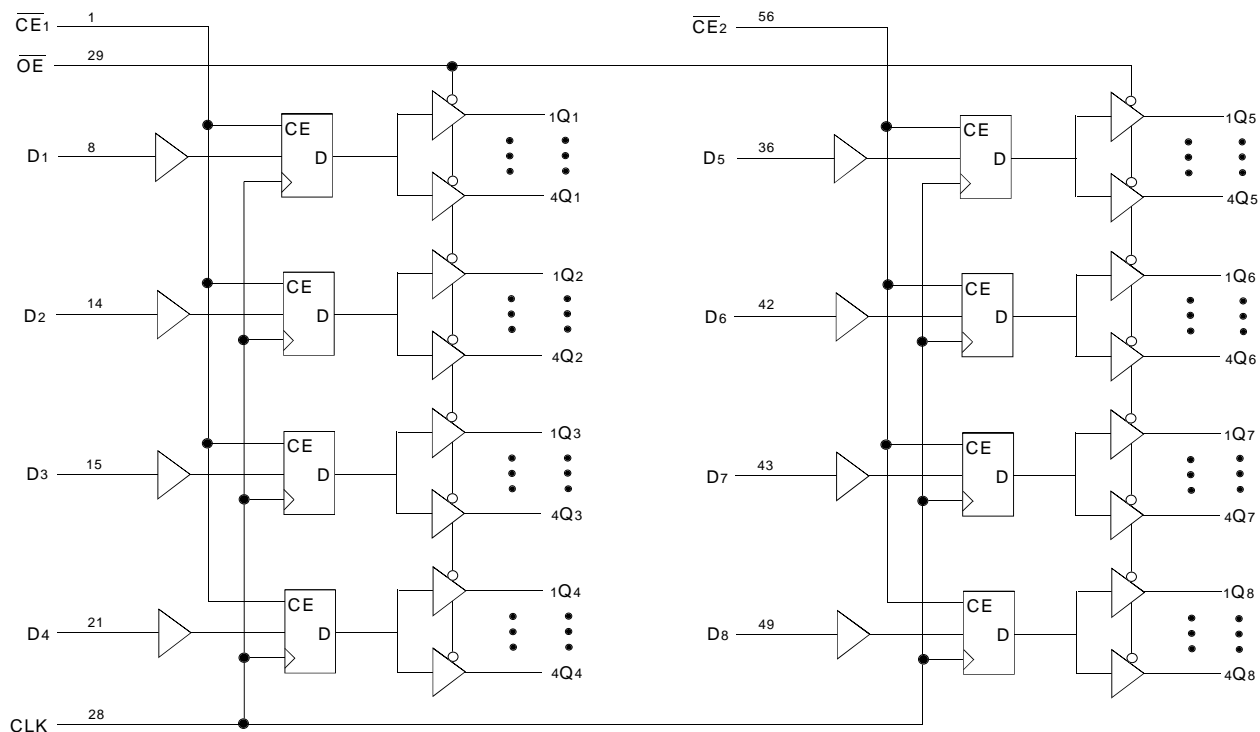
This registered address line driver is built using advanced dual metal CMOS technology. The ALVCH16345 is configured with banks of four drivers, each to be used in high speed synchronous memory applications.

The ALVCH16345 is ideal for driving memory modules in systems where multiple memory modules are used. One each of the four output banks drives a different module; modules can be added or removed without affecting the signal integrity of the other modules in the system. Dual clock enables (\overline{CEx}) allow use of the device in high speed memory interleaving applications where the clock can be alternately enabled and disabled, allowing the address to be held for additional cycles during memory access.

The ALVCH16345 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16345 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

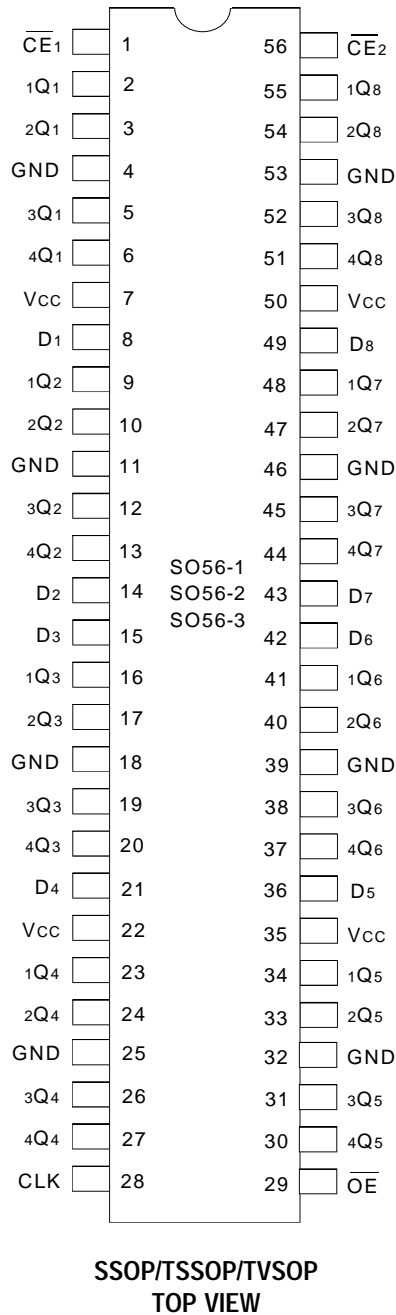
Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

APRIL 1999

PIN CONFIGURATION



PIN DESCRIPTION

Pin Names	Description
\overline{OE}	3-State Output Enable Inputs (Active LOW)
Dx	Data Inputs ⁽¹⁾
xQx	3-State Data Outputs
CLK	Clock Input
\overline{CEx}	Clock Enable Inputs (Active LOW)

NOTE:

1. These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	- 0.5 to VCC + 0.5	V
TSTG	Storage Temperature	- 65 to + 150	°C
IOUT	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	- 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	± 100	mA

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NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VCC terminals.
3. All terminals except VCC.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

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NOTE:

1. As applicable to the device type.

FUNCTION TABLE (1)

Inputs				Output
\overline{CEx}	CLK	\overline{OE}	Dx	xQx
H	X	L	X	B ₀
X	L	L	X	B ₀
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
B₀ = Indicates the previous state

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	± 5	μA
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	± 5	
I _{OZH}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	± 10	μA
I _{OZL}			V _O = GND	—	—	± 10	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL}	Quiescent Power Supply Current	V _{CC} = 3.6V		—	0.1	40	μA
I _{CCH}		V _{IN} = GND or V _{CC}					
I _{CCZ}							
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	750	μA

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NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BHH}	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	-75	—	—	μA
I _{BHL}			V _I = 0.8V	75	—	—	
I _{BHH}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	-45	—	—	μA
I _{BHL}			V _I = 0.7V	45	—	—	
I _{BHHO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	± 500	μA
I _{BHLO}							

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = - 0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = - 6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = - 12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = - 24mA	2	—	
VOL	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

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NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V _{CC} = 2.5V ± 0.2V	V _{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C _L = 0pF, f = 10MHz			pF
CPD	Power Dissipation Capacitance Outputs disabled				pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	150	—	MHz
t _{PLH}	Propagation Delay	1.5	5.4	1.5	4.4	1.5	4	ns
t _{PHL}	CLK to xQx							
t _{PZH}	Output Enable Time	1.5	5.2	1.5	5.1	1.5	4.5	ns
t _{PZL}	\overline{OE} to xQx							
t _{PHZ}	Output Disable Time	1.5	5.5	1.5	4.5	1.5	5.2	ns
t _{PLZ}	\overline{OE} to xQx							
t _{SU}	Setup Time, \overline{CE} x to CLK, HIGH or LOW	1.5	—	1.5	—	1.5	—	ns
t _{SU}	Setup Time, Dx to CLK, HIGH or LOW	1.5	—	1.5	—	1.5	—	ns
t _H	Hold Time, \overline{CE} x to CLK, HIGH or LOW	0.5	—	0.5	—	0.5	—	ns
t _H	Hold Time CLK to Dx, HIGH or LOW	0.5	—	0.5	—	0.5	—	ns
t _w	Pulse Width, CLK HIGH or LOW	3	—	3	—	3	—	ns
t _{sk(o)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps
t _{sk(b)}	Output Skew ⁽²⁾	—	—	—	—	—	350	ps

NOTES:

- See test circuits and waveforms. T_A = - 40°C to + 85°C.
- Skew between any two outputs of the same package and switching in the same direction. For t_{sk(o)} OUTPUT1 and OUTPUT2 are any two outputs. For t_{sk(b)} OUTPUT1 and OUTPUT2 are in the same bank.

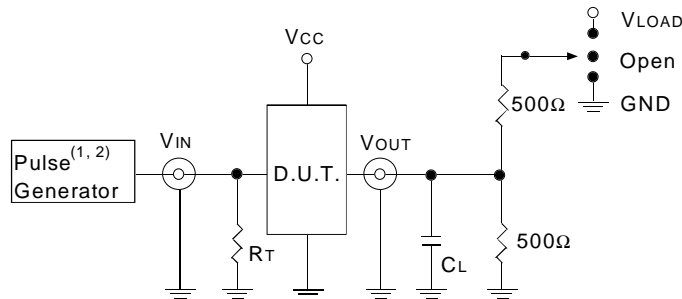
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

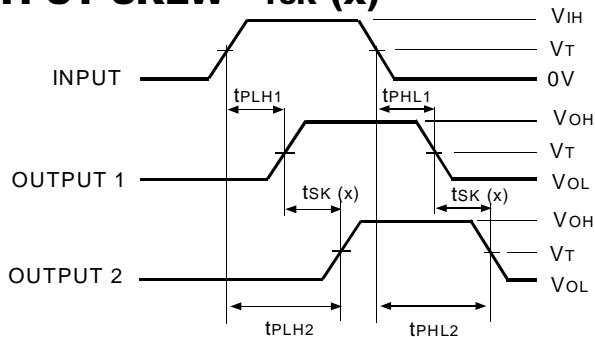
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - TSK (x)



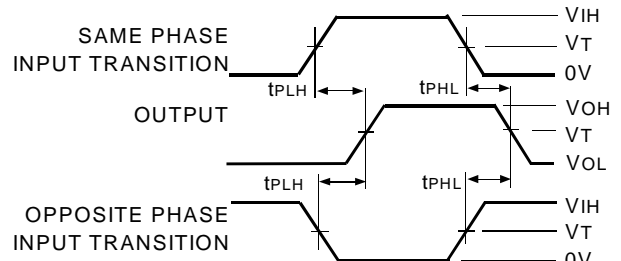
$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

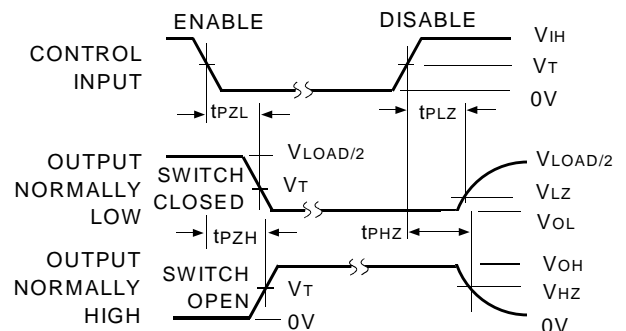
1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

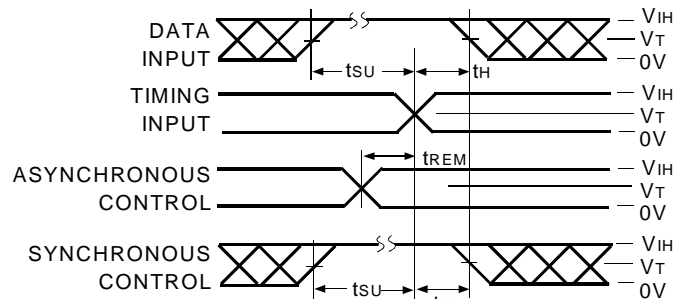


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NOTE:

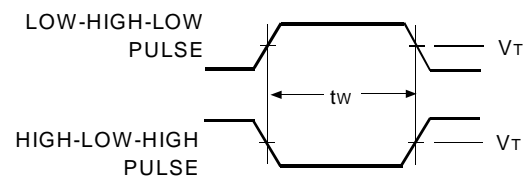
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



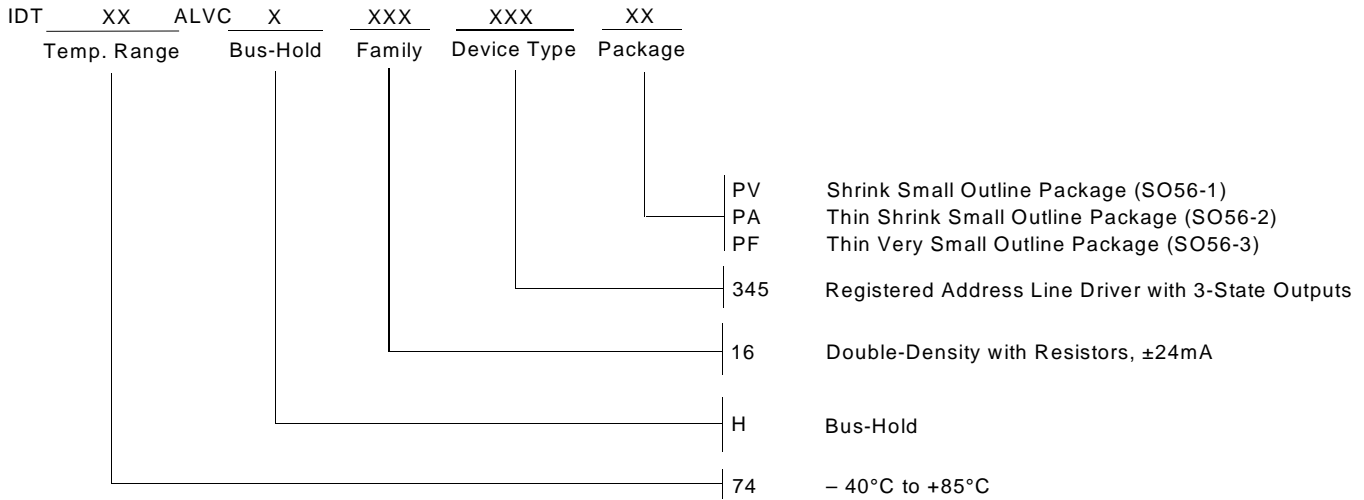
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PULSE WIDTH



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ORDERING INFORMATION



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