IR3Y48A1

CCD Signal Process & Digital Interface IC

DESCRIPTION

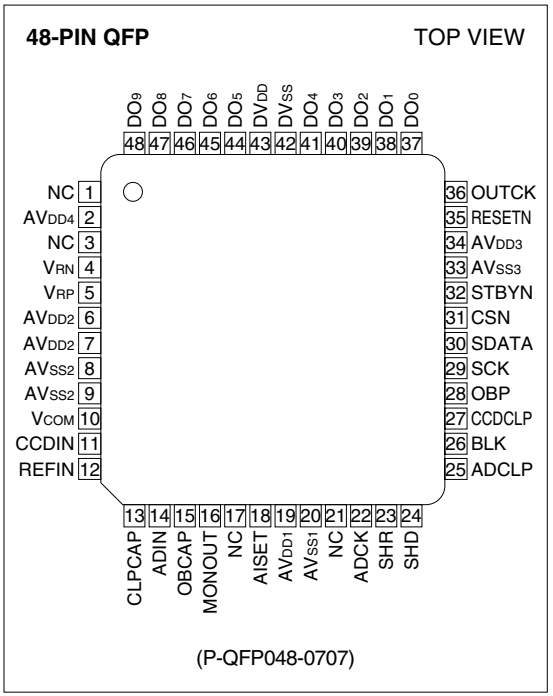
The IR3Y48A1 is a CMOS single-chip signal processing IC for CCD area sensors which includes correlated double sampling circuit (CDS), clamp circuit, programmable gain amplifier (PGA), reference voltage generator, black level detection circuit, 18 MHz 10-bit analog-to-digital converter (ADC), timing generator for internally required pulses, and serial interface for internal function control and PGA gain control.

FEATURES

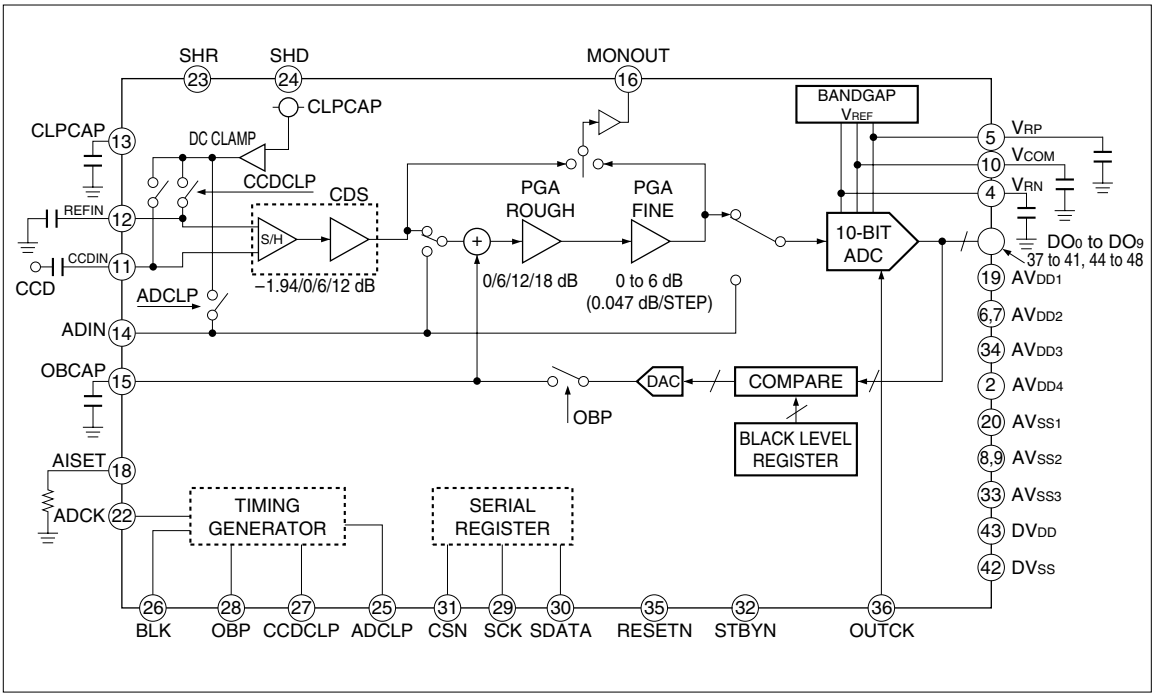
- Low power consumption : 80 mW (TYP.)
- Wide gain range : –1.94 to 36 dB
  (Gain step : 0.047 dB/step)
- High speed sample-and-hold circuits :
  pulse width 11 ns (MIN.)
- Independent CDS and PGA gain control
  – CDS : –1.94/0/6/12 dB
  – PGA : 0 to 24 dB
- Black level canceler
  – Settling target : 16 to 127 LSB
- Capable of independent input of ADC conversion clock and data output clock
- Power down mode : less than 1 mW
- Built-in serial interface
- 10-bit ADC operating up to 18 MHz
  – DNL : ±0.6 LSB (TYP.)
- Maximum input level of CCD signals : 1.1 Vp-p
- Accepts a direct signal input to ADC or PGA (input level : 1.0 Vp-p (TYP.))
- Single 2.7 to 3.6 V power supply
- Package :
  48-pin QFP* (P-QFP048-0707) 0.5 mm pin-pitch

*Contact SHARP in order to obtain the details of package dimensions of the IR3Y48A1.

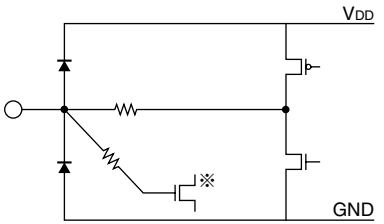
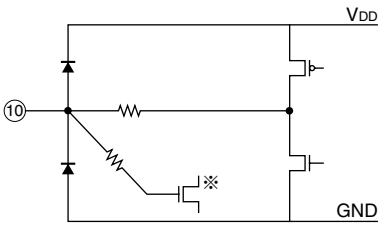
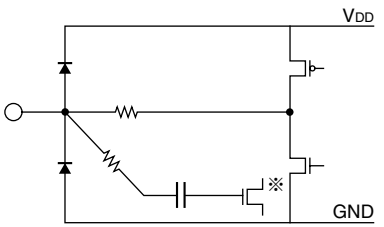
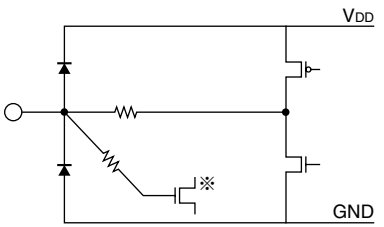
PIN CONNECTIONS



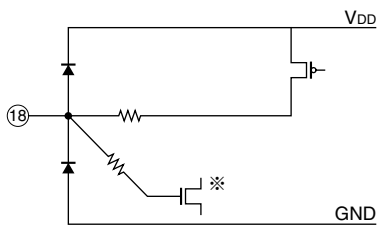
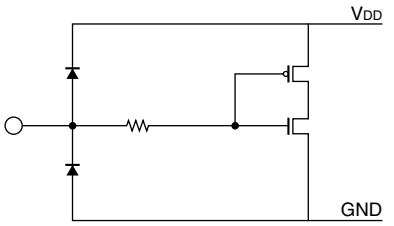
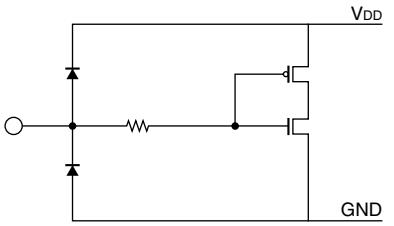
BLOCK DIAGRAM



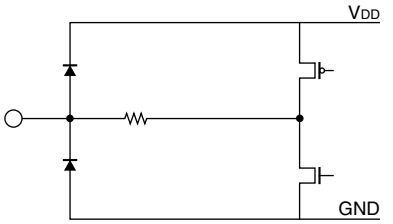
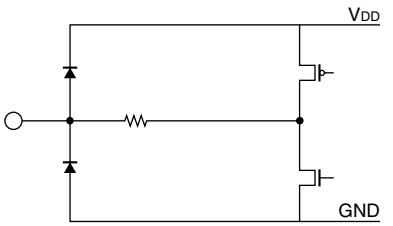
PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	EQUIVALENT CIRCUIT	DESCRIPTION
1	NC	–		No connection.
2	AV_{DD4}	–		Supply of 2.7 to 3.6 V analog power.
3	NC	–		No connection.
4	V_{RN}	O		ADC internal negative reference voltage. (Connect to AVSS via 0.1 µF.)
5	V_{RP}	O		ADC internal positive reference voltage. (Connect to AVSS via 0.1 µF.)
6	AV_{DD2}	–		Supply of 2.7 to 3.6 V analog power.
7	AV_{DD2}	–		Supply of 2.7 to 3.6 V analog power.
8	AV_{SS2}	–		An analog grounding pin.
9	AV_{SS2}	–		An analog grounding pin.
10	V_{COM}	O		ADC internal common reference voltage. (Connect to AVSS via 0.1 µF.)
11	CCDIN	I		CDS circuit data input.
12	REFIN	I		CDS circuit reference input.
13	CLPCAP	O		Clamp level output. (Connect to AVSS via 0.1 µF.)
14	ADIN	I		ADIN signal input.
15	OBCAP	O		Black level integration voltage. (Connect to AVSS via 0.1 µF.)
16	MONOUT	O		Monitor output of CDS or PGA.

※ Internal FET gate

PIN NO.	SYMBOL	I/O	EQUIVALENT CIRCUIT	DESCRIPTION
17	NC	–		No connection.
18	AISET*	I		Internal analog circuit bias current input. (Connect to AVSS via 4.7 kΩ.)
19	AVDD1	–		Supply of 2.7 to 3.6 V analog power.
20	AVSS1	–		An analog grounding pin.
21	NC	–		No connection.
22	ADCK	I		ADC sampling clock input.
23	SHR	I		Reference sampling pulse input.
24	SHD	I		Data sampling pulse input.
25	ADCLP	I		Pulse input for ADIN clamp and black calibration control.
26	BLK	I		Blanking pulse input.
27	CCDCLP	I		Clamp control input.
28	OBP	I		Black level period pulse input.
29	SCK	I		Serial port clock input.
30	SDATA	I		Serial port data input.
31	CSN	I		Serial port chip selection (active at low).
32	STBYN	I		Power down control (power down at low).
33	AVSS3	–		An analog grounding pin.
34	AVDD3	–		Supply of 2.7 to 3.6 V analog power.
35	RESETN	I		Reset signal input (reset at low).
36	OUTCK	I		Clock input for ADC output.

∗ High-Z at power down ※ Internal FET gate

PIN NO.	SYMBOL	I/O	EQUIVALENT CIRCUIT	DESCRIPTION
37	DO_0*	O		ADC digital output (3 state) (LSB).
38	DO_1*	O		ADC digital output (3 state).
39	DO_2*	O		ADC digital output (3 state).
40	DO_3*	O		ADC digital output (3 state).
41	DO_4*	O		ADC digital output (3 state).
42	DV_{SS}	–		A digital grounding pin.
43	DV_{DD}	–		Supply of 2.7 to 3.6 V digital power.
44	DO_5*	O		ADC digital output (3 state).
45	DO_6*	O		ADC digital output (3 state).
46	DO_7*	O		ADC digital output (3 state).
47	DO_8*	O		ADC digital output (3 state).
48	DO_9*	O		ADC digital output (3 state) (MSB).

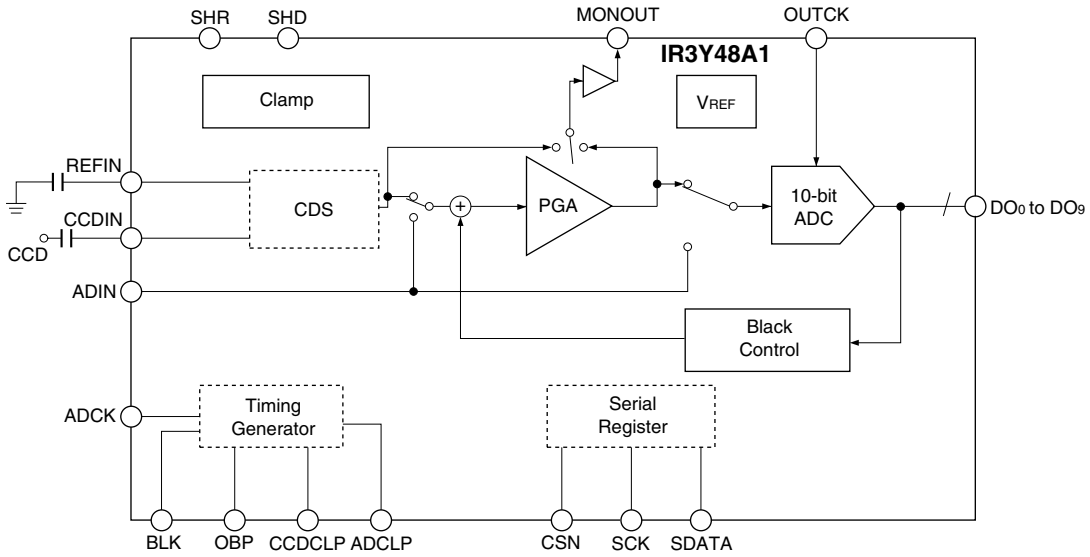
* High-Z at power down

NOTE : NC pins are not connected internally, but recommended to be connected to AV_{SS}.

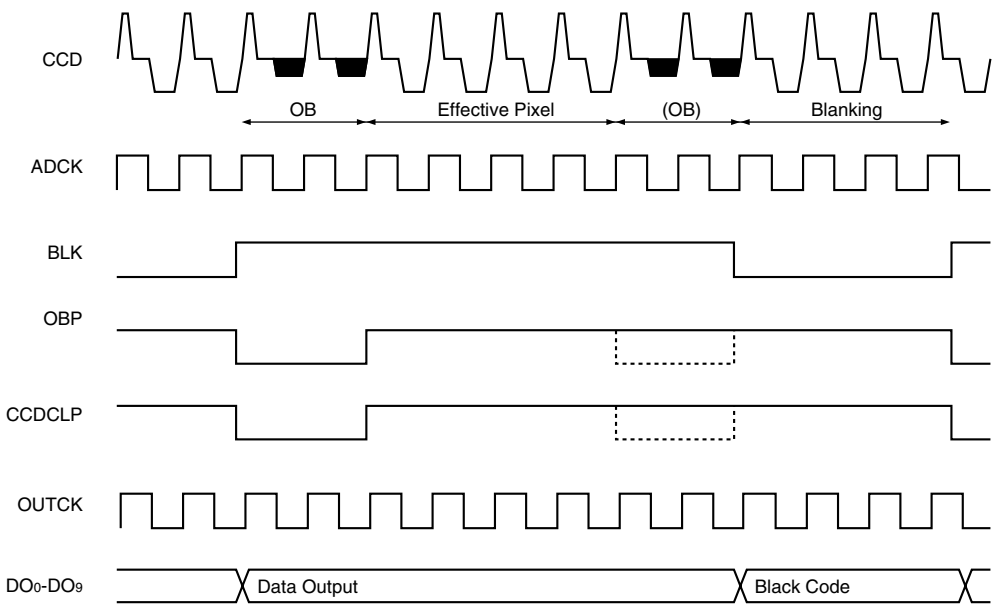
FUNCTIONAL DESCRIPTION

Outline

The configuration of the IR3Y48A1 is described below.



GENERAL TIMING



NOTE : In this chart, the cycles of the OBP and CCDCLP show the same timing. But the OBP and CCDCLP can be input at different timing.

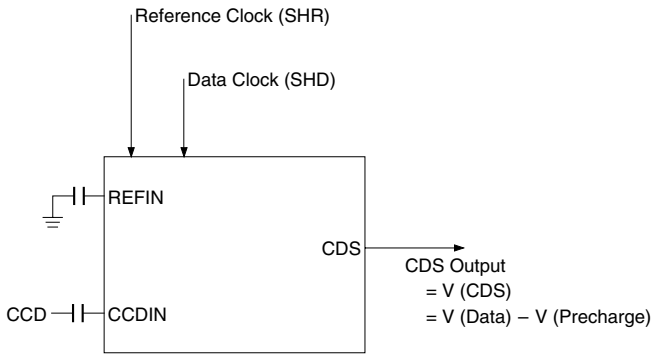
CDS (Correlated Double Sampling) Circuit

Connect the signal from a CCD sensor to the CCDIN pin via a capacitor and connect the REFIN pin to AVSS via a capacitor.

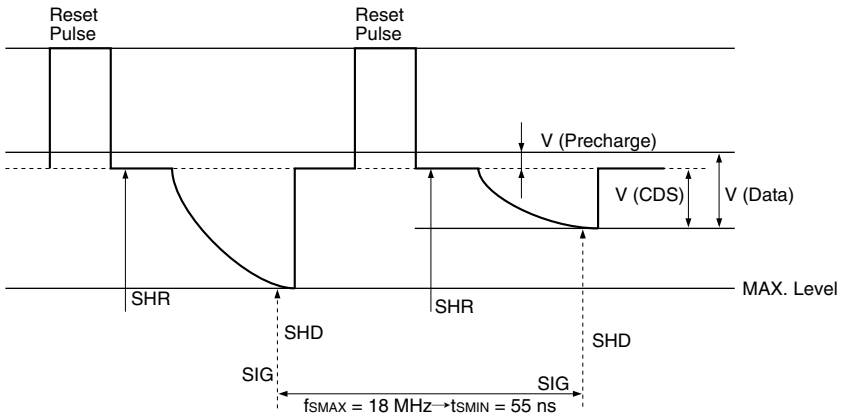
The CDS circuit holds the CCD precharge (reference) level at SHR pulse, then it samples the CCD pixel data at SHD pulse. Correlated (common) noise is removed by the subtracting precharge level from the pixel data level.

CDS can choose a gain setting from 0, 6.02, 12 or −1.94 dB (Mode (3) Register D_4 & D_5 bits). A CDS gain is controlled separately from a PGA gain. To reduce noise as much as possible, it is recommended to increase the CDS gain first before increasing the PGA gain.

CDS Circuit



CDS Operation



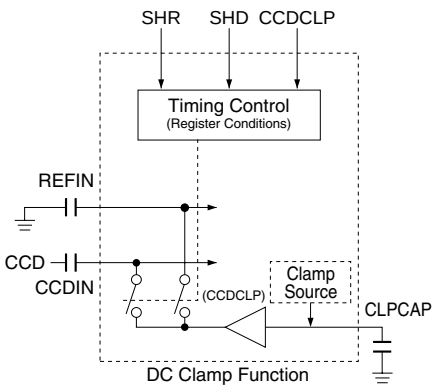
Clamp Circuits

DC CLAMP

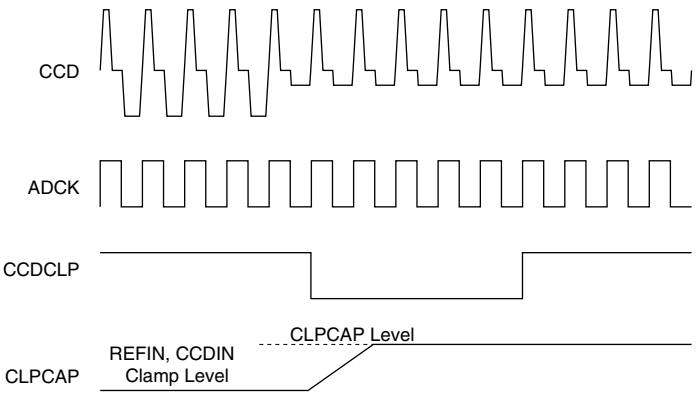
DC level of the CCDIN/REFIN input is fixed by internal DC clamp circuit. DC level of C-coupled CCD signal at the CDS input is set to CLPCAP by the internal DC clamp circuit.

Normally clamp switches are turned on at the black level calibration period. Place 0.1 µF external capacitance between CLPCAP and AVSS.

DC Clamp



Clamp Timing



NOTE : For ADIN input, clamp operation is controlled by ADCLP.
(Black level calibration is performed at the same time.)

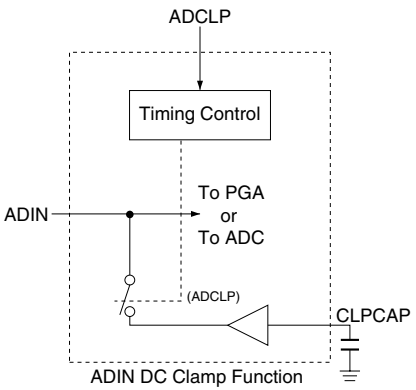
CLAMP OF THE ADIN SIGNAL

Clamp operation for the ADIN path is also available. Note that clamp voltage [CLPCAP] is different between CCDIN/REFIN input and the ADIN input.

Clamp operation of ADIN signal can be turned off by register setting.

Clamp circuit is controlled by ADCLP signal at "ADIN signal to ADC" mode. Black level calibration circuit is also controlled by ADCLP at "ADIN signal to PGA" mode.

ADIN DC Clamp



CLAMP CONTROL

Following items are selectable by the register setting.

a) Clamp current [Mode (2) Register D7]
Normal or fast clamp is selectable for charge current. (Select normal clamp in general.)

b) Clamp target [Mode (2) Register D5 & D4]
Input signals (REFIN and CCDIN) to be clamped are selectable. It is also possible to turn off the clamp function.

Black Level Cancel Circuit

The purpose of a black level cancel circuit is to control the DC level of the PGA input so that the ADC output code at a optical black period may correspond to the black level code set up by the register. The black level code of (1 to) 16 to 127 LSB (default : 64 LSB) is available.

A black level cancel loop is established while the OBP pin is active. In this loop, the ADC output code is compared with the black level code and the voltage of the OBCAP capacitor is controlled by the result. Thus, the OBCAP voltage settles gradually, and the signal level of the optical black period corresponds to the established value.

The charge of the OBCAP capacitor is reset under following conditions :

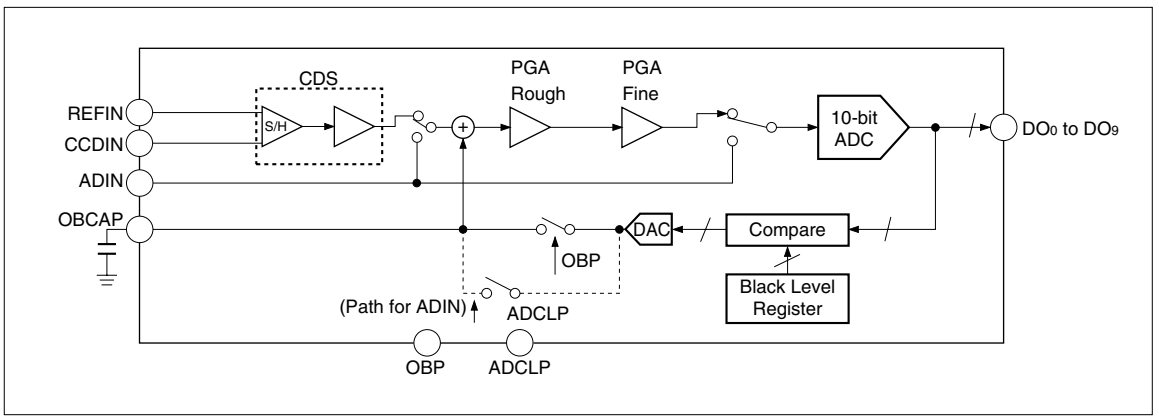
① Set the black level reset register to "1". [Mode (1) Register D_1 = 1]

② Set the RESET pin to low.

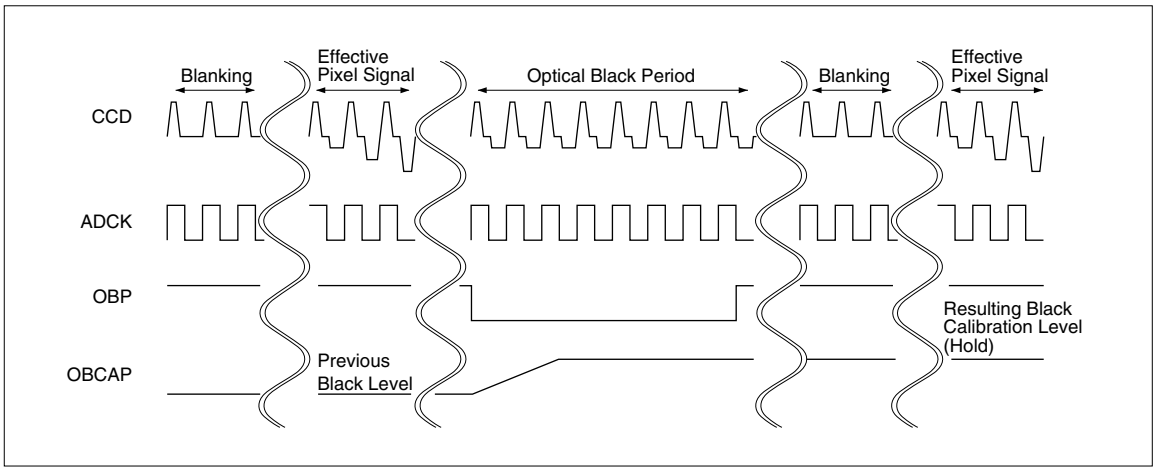
③ Power down (by the STBYN pin or register control)

The DC clamping [CCDCLP] is allowed while the OBP pin is low.

The black level cancellation is also available in "ADIN signal to PGA" mode. (See the broken line path of "**Black Level Calibration**" below.) The black level cancellation is available at the ADCLP period in this mode. (That means a clamping and a black level cancelling are done simultaneously.)



Black Level Calibration



Black Level Calibration Timing

High-speed Black Level Cancellation

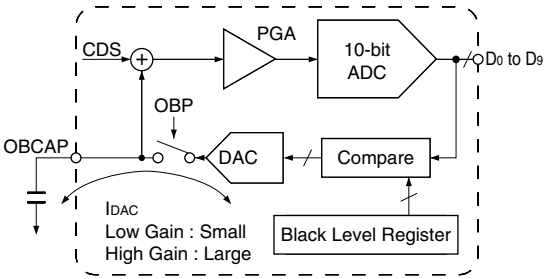
The IR3Y48A1 has the function that settles a black level at high speed. The function that increases a settling speed in a fixed period from the access to the serial interface can become available by the register setting. This function increases the gain of the settling DAC in a fixed period, and it increases the charge/discharge current to the OBCAP capacitor.

The black level boost function is set with the Mode (3) register, D_3, D_2, D_1 and D_0 bits. The default setting is always low gain ($D_3 = D_2 = D_1 = D_0 = 0$). By setting the register D_2, D_1 and D_0 bits, the gain becomes high during 1 to 7 times of OBP pulse period after any access to the serial interface. After that period, the gain returns to low.

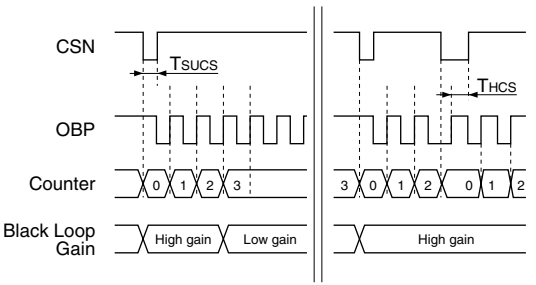
When setting D_3 to "1", the gain is always high. The CSN signal becomes the starting point of the OBP pulse count.

The right figure of "Black Loop Settling Gain Boost Timing" is the timing chart when the boost control is on and the boost period is set to 3. The left figure of "Black Level Settling" below is the image of the settlement when the gain is high or low.

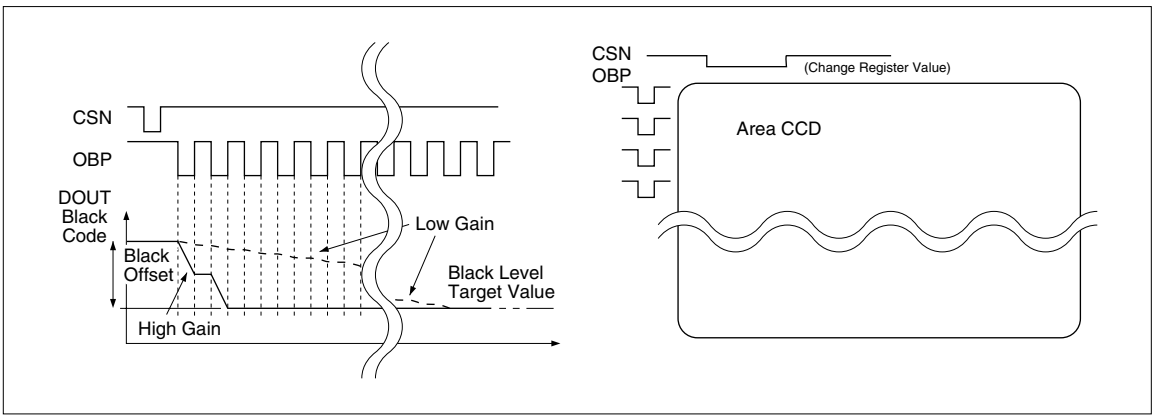
Black Level Boost



Black Loop Settling Gain Boost Timing



Gain boost function ON (Mode (3) $D_3 = 1$)
High gain for 3 pulses (Mode (3) $D_2 = 0$, $D_1 = 1$, $D_0 = 1$)



Black Level Settling

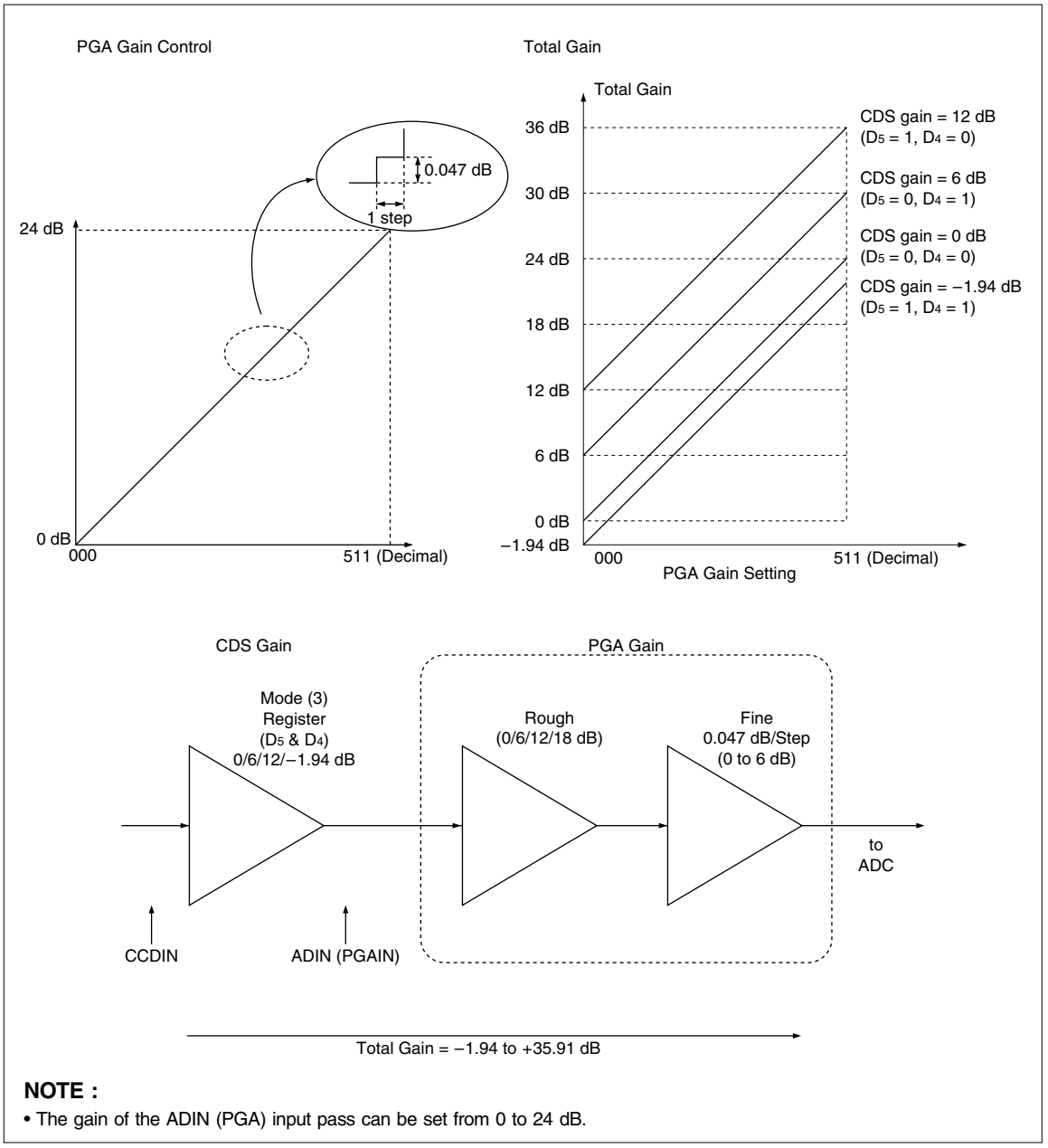
CSN & OBP TIMING

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CSN setup time	T_{SUCS}		0			µs
CSN hold time	T_{HCS}		5			clock

Gain Control Circuit

The total gain for a CCD input signal covers from −1.94 to +36 dB.

This range consists of CDS (0/6/12/−1.94 dB), PGA rough (0/6/12/18 dB), and PGA fine (0 to 6 dB (0.047 dB/step)). The CDS gain is controlled by a 2-bit register and the PGA gain is controlled by a 9-bit register.



NOTE :

• The gain of the ADIN (PGA) input pass can be set from 0 to 24 dB.

Gain Control

A/D Converter Circuit

The IR3Y48A1 integrates an 18 MHz 10-bit full pipeline A/D converter (ADC).

This ADC converts following signals :

1. The signal from the CCDIN input through a CDS and a PGA
2. The signal from the ADIN input through a PGA at the ADIN (PGA input) mode.
3. The signal from the ADIN input at the ADIN (ADC input) mode.

A/D CONVERSION RANGE

The analog input range of the ADC is determined by the internal reference voltage.

The full scale of the ADC is 1.0 Vp-p (single end).

A/D CONVERTER OUTPUT CODE (AT MODE (1) REGISTER D_5 = 1)

The format of an ADC digital output is a straight binary.

Thus, when input a zero reference voltage, the output code is "all 0", and when input a full scale voltage, the output code is "all 1".

CLOCK, PIPELINE DELAY, DIGITAL DATA OUTPUT TIMING

The ADCK input is used for an A/D conversion.

The ADC input signal is sampled at the falling edge of the ADCK input and 10-bit parallel data is output at the rising edge of the ADCK input after 5.5 clocks of pipeline delay.

HIGH-Z CONTROL OF ADC DIGITAL OUTPUT

ADC digital outputs become High-Z under following conditions :

① Set the ADC output bit to "1".
[Mode (1) Register D_2 = 1]

② Set the SYBYN pin to low.

③ Set the power control bit to "1".
[Mode (1) Register D_0 = 1]

ADC Data Output (Coding : Straight Binary)

A/D INPUT	DIGITAL OUTPUT CODE									
	MSB									LSB
	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Full scale	1	1	1	1	1	1	1	1	1	1
:					:					
:	1	0	0	0	0	0	0	0	0	0
:	0	1	1	1	1	1	1	1	1	1
:					:					
Zero scale	0	0	0	0	0	0	0	0	0	0

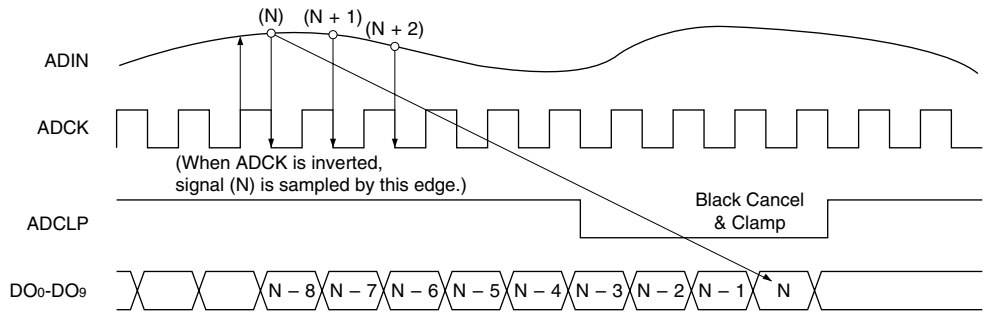
Miscellaneous Functions

ADC DIRECT INPUT (ADIN MODE)

The direct input path to the ADC or the PGA becomes available by register setting. The selectable paths are shown below :

1. Function disable (default)
   [Mode (1) Register D_5 = 0, D_4 = 0]
2. ADIN input to the PGA
   [Mode (1) Register D_5 = 0, D_4 = 1]
3. ADIN input to the ADC
   [Mode (1) Register D_5 = 1, D_4 = don't care]

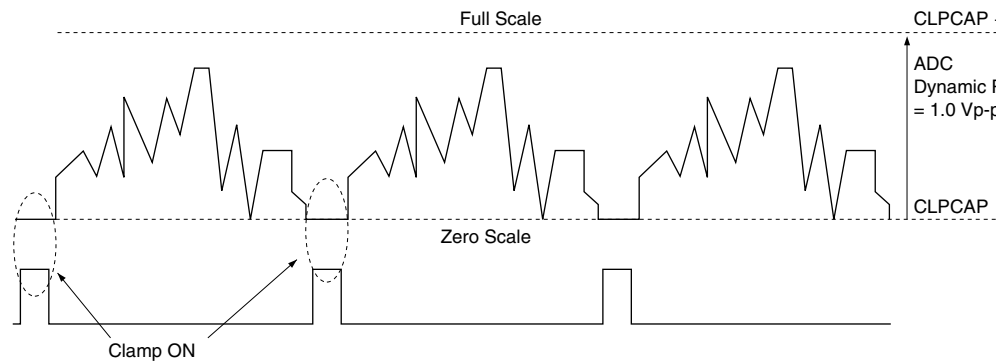
At the ADIN mode, the BLK, SHD and SHR inputs are ignored.



NOTE : This figure shows the timing when an OUTCK input function is disabled (Mode (1) D_8 = 0). When it is enabled (D_8 = 1), the data is output at the rising (D_7 = 0) or the falling (D_7 = 1) edge of the OUTCK input.
When ADCLP input is low, both black level cancel and clamp are active at the PGA input mode, and only the clamp is active at ADC input mode.

ADIN Signal Processing (PGA Input)

The operation at ADC direct input is shown below. Thus, the clamped level at the ADCLP timing becomes a reference (CLPCAP at the figure below), and the ADIN input dynamic range is +1.0 V (TYP.) from the reference level.



ADIN Signal Input Level

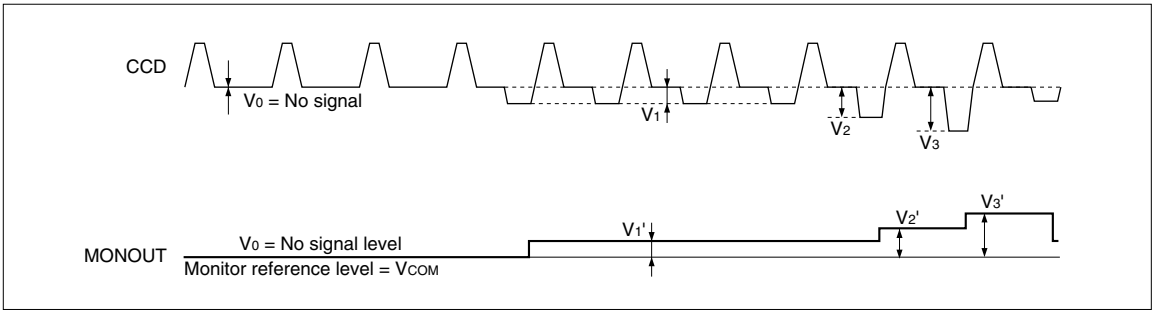
POWER DOWN MODE

The power down mode can be set either by register setting or STBYN pin.

If one of them is set, the IR3Y48A1 powers down. ("OR" logic)

MONITOR OUTPUT

By setting the register [Mode (2) Register D_1 & D_0], the signal from MONOUT is selectable. Alternatives are OFF, CDS output, PGA output, or REFIN/CCDIN output. Note that the gain of the MONOUT pin is fixed to 0 dB regardless the setting of gain control register when the CDS output is selected. The output level of MONOUT is shown below. The MONOUT level becomes V_{COM} at zero reference level. The signals are output in reverse for the CCD input.



Monitor Output Level

POLARITY INVERSION

The following input polarities can be inverted by register setting :

① ADCK (A/D converter sampling clock)
[Mode (1) Register D_6]

② SHR and SHD (CDS sampling clock)
[Mode (2) Register D_3 & D_2]

③ BLK, OBP, CCDCLP and ADCLP (Enable controls)
[Mode (2) Register D_3 & D_2]

Power Control

Usually, make the power control register (Mode (1) Register D_3) "1" to select low power mode.
The default setting of this register is "1".

Data Output Clock

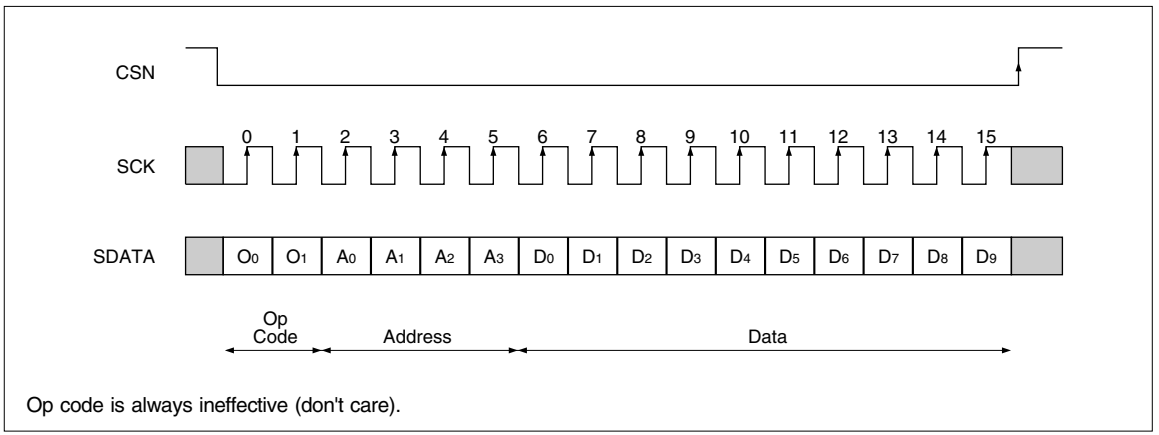
The ADCK input or the OUTCK input is selectable as an ADC data output clock.

General Notice for Power Supply

It is recommended to supply power to both AV_{DD} and DV_{DD} from a single regulator.
(Keep the absolute maximum rating; $DV_{DD} \leq (AV_{DD} + 0.3\ V)$ even at the power-up or the power-down sequence.)
Refer to **"APPLICATION CIRCUIT EXAMPLE"** for power supply decouplings.

Serial Interface Circuit

The internal registers of IR3Y48A1 are controlled by the 3-wire serial interface. The data is a 16-bit-length serial data that consists of a 2-bit operation code, a 4-bit address, and a 10-bit data. The each bit is fetched at the rising edge of the SCK input and the data is executed at the rising edge of the CSN input. When not access, make the CSN input high.
It is prohibited to write to a non-defined address. When a data length is below 16-bit, the data is not executed.



Op code is always ineffective (don't care).

Serial Interface Write Control

Registers

The IR3Y48A1 has 10-bit x 7 registers to control its operations. Two of the seven registers are used for the LSI testing.

All registers are write only. The serial registers are written by the serial interface.

Register Map

R/W	ADDRESS				REGISTER NAME	MAJOR FUNCTIONS [DATA]
	A_3	A_2	A_1	A_0		
W	0	0	0	0	Mode (1)	DOUT timing control/OUTCK polarity/ADCK polarity/ADIN connection/Power control/ADC output/Black level reset/Power down
W	0	0	0	1	Mode (2)	Clamp current/ADIN clamp/Clamp target/ S/H, enable logic/Monitor selection
W	0	0	1	0	Mode (3)/CDS gain	CDS gain control/Black loop gain boost/Boost period
W	0	0	1	1	PGA gain	PGA gain
W	0	1	0	0	Black level	ADC code at black level (1 LSB step)
W	1	0	0	0	Test (1)	Test mode (1) (ADIN coupling mode)
W	1	0	0	1	Test (2)	Test mode (2)

1. Register name Mode (1)
2. Register address
   [Write]

A_3	A_2	A_1	A_0
0	0	0	0

3. Register bit assignment

	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Default	X	0	0	0	0	0	0	0	0	0
Functions										
DOUT timing control		<->								
OUTCK polarity			<->							
ADCK polarity				<->						
ADIN connection					<---->					
Power control							<->			
ADC output								<->		
Black level reset									<->	
Power down										<->

4. Register operations

	CONTROLS										OPERATIONS	NOTE
	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
DOUT timing control		0									DOUT synchronizes to ADCK	
		1									DOUT synchronizes to OUTCK	
OUTCK polarity			0								DOUT changes at OUTCK rising edge	1
			1								DOUT changes at OUTCK falling edge	1
ADCK polarity				0							Normal operation as timing chart	
				1							ADCK clock inversion	
ADIN connection					0	0					ADIN function OFF	
					0	1					ADIN signal to PGA	
					1	X					ADIN signal to ADC	
Power control							0				Not recommended	
							1				Low power	2
ADC output								0			Normal operation [ADC data output]	
								1			ADC output High-Z [or logic of STBYN]	3
Black level reset									0		Normal operation	
									1		Black level reset [or logic of RESETN]	4
Power down										0	Normal operation	
										1	Power down [or logic of STBYN]	

X : Don't care

NOTES :

1. DOUT edge control is effective when D_8 = 1 (DOUT synchronizes to OUTCK).
2. Power control bit (D_3) must be "1" to operate as specified value.
   The default value is "1" (low power).
3. ADC output is set to high impedance if one of the following case is true.
   Case 1 : Set "ADC output" bit to "1".
   Case 2 : Set STBYN pin to low.
   Case 3 : Set "Power down" bit to "1".
4. Black level integral CAP [OBCAP] is discharged if the following case is true.
   Case 1 : Set "Black level reset" bit to "1".
   Case 2 : Set RESETN pin to low.

1. Register name Mode (2)
2. Register address
   [Write]

A_3	A_2	A_1	A_0
0	0	0	1

3. Register bit assignment

	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Default	X	X	0	0	0	0	0	0	0	0
Functions										
Clamp current			<->							
ADIN clamp				<->						
Clamp target					<---->					
S/H, enable logic							<---->			
Monitor selection									<---->	

X : Don't care

4. Register operations

	CONTROLS										OPERATIONS	NOTE
	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Clamp current			0								Normal clamp (±50 µA)	
			1								Fast clamp (±100 µA)	
ADIN clamp				0							Clamp operation active for ADIN	
				1							No clamp for ADIN	
Clamp target					0	0					Normal mode [Clamp both REFIN and CCDIN]	
					0	1					Clamp REFIN only	
					1	0					Clamp CCDIN only	
					1	1					Clamp OFF	
S/H, enable logic							0	0			Normal operation as timing chart	
							0	1			S/H control polarity inversion	1
							1	0			Enable control polarity inversion	2
							1	1			Both of S/H and enable inversion	
Monitor selection									0	0	Monitor OFF	
									0	1	CDS signal to monitor	3
									1	0	PGA output monitor	4
									1	1	Output REFIN and CCDIN (for calibration)	

NOTES :

1. The S/H signals are SHR and SHD.
2. The enable controls are BLK, OBP, CCDCLP, and ADCLP.
3. At this mode, monitor output gain = 0 dB regardless of CDS gain.
4. At this mode, monitor output depends on CDS gain.

1. Register name Mode (3)
2. Register address
   [Write]

A_3	A_2	A_1	A_0
0	0	1	0

3. Register bit assignment

	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Default	X	X	X	X	0	0	0	0	0	0
CDS gain control					<---->					
Black loop gain boost							<->			
Boost period								<------->		

X : Don't care

4. Register operations

	CONTROLS										OPERATIONS	NOTE
	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
CDS gain control					0	0					CDS gain = 0 dB	
					0	1					CDS gain = +6.02 dB	
					1	0					CDS gain = +12.04 dB	
					1	1					CDS gain = −1.94 dB	
Black loop gain boost							0				Boost control ON	1
							1				Always high gain	2
Boost period								0	0	0	Always low gain	3
								0	0	1	High gain for 1 OBP pulse	1, 3
								0	1	0	High gain for 2 OBP pulses	1, 3
								0	1	1	High gain for 3 OBP pulses	1, 3
								1	0	0	High gain for 4 OBP pulses	1, 3
								1	0	1	High gain for 5 OBP pulses	1, 3
								1	1	0	High gain for 6 OBP pulses	1, 3
								1	1	1	High gain for 7 OBP pulses	1, 3

NOTES :

1. Black loop settling gain is boosted [speed up] for defined period.
   Gain is boosted n OBP pulse(s) after rising edge of CSN [SIO data write].
   Boosted period n (1 to 7 pulses) is determined by "boost period" (D_2...D_0).
   After n OBP pulse(s), black loop gain returns automatically to low gain.
2. Black loop settling is always high gain [boosted].
3. "Boost period" register is effective only when D_3 = 1.

1. Register name PGA gain
2. Register address
   [Write]

A_3	A_2	A_1	A_0
0	0	1	1

3. Register bit assignment

	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Default	X	0	0	0	0	0	0	0	0	0
Functions										
PGA gain		<----------								---------->

X : Don't care

4. Register operations

	CONTROLS										DECIMAL	HEX	PGA GAIN (dB)
	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
PGA gain		0	0	0	0	0	0	0	0	0	0	0	0.000
		0	0	0	0	0	0	0	0	1	1	1	0.047
		0	0	0	0	0	0	0	1	0	2	2	0.094
		0	0	0	0	0	0	0	1	1	3	3	0.141
		0	0	0	0	0	0	1	0	0	4	4	0.188
					...								
		0	0	0	1	1	1	1	1	0	62	3E	2.916
		0	0	0	1	1	1	1	1	1	63	3F	2.963
		0	0	1	0	0	0	0	0	0	64	40	3.010
		0	0	1	0	0	0	0	0	1	65	41	3.057
					...								
		0	0	1	1	1	1	1	1	1	127	7F	5.973
		0	1	0	0	0	0	0	0	0	128	80	6.020
		0	1	0	0	0	0	0	0	1	129	81	6.067
					...								
		0	1	1	0	0	0	0	0	0	192	C0	9.030
					...								
		0	1	1	1	1	1	1	1	1	255	FF	11.993
		1	0	0	0	0	0	0	0	0	256	100	12.040
		1	0	0	0	0	0	0	0	1	257	101	12.087
					...								
		1	0	1	0	0	0	0	0	0	320	140	15.050
					...								
		1	0	1	1	1	1	1	1	1	383	17F	18.013
		1	1	0	0	0	0	0	0	0	384	180	18.060
		1	1	0	0	0	0	0	0	1	385	181	18.107
					...								
		1	1	1	0	0	0	0	0	0	448	1C0	21.070
					...								
		1	1	1	1	1	1	1	1	0	510	1FE	23.986
		1	1	1	1	1	1	1	1	1	511	1FF	24.033

1. Register name Black level
2. Register address
   [Write]

A_3	A_2	A_1	A_0
0	1	0	0

3. Register bit assignment

	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Default	X	X	X	1	0	0	0	0	0	0
Functions										
Black level				<----------						---------->

X : Don't care

4. Register operations

	OPERATIONS [ADC CODE : BINARY]										BLACK CODE		NOTE
	B_9	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	DECIMAL	HEX	
Black level				0	0	0	0	0	0	0	FORBIDDEN	FORBIDDEN	
				0	0	0	0	0	0	1	1	1	1
							...						1
				0	0	0	1	1	1	1	15	F	1
				0	0	1	0	0	0	0	16	10	
				0	0	1	0	0	0	1	17	11	
				0	0	1	0	0	1	0	18	12	
				0	0	1	0	0	1	1	19	13	
							...						
				0	1	0	0	0	0	0	32	20	
							...						
				1	0	0	0	0	0	0	64	40	
							...						
				1	1	1	1	1	0	0	124	7C	
				1	1	1	1	1	0	1	125	7D	
				1	1	1	1	1	1	0	126	7E	
				1	1	1	1	1	1	1	127	7F	

NOTE :

1. Codes 1 to 15 are available but not recommended. Black calibration period is specified under 15 < code < 128.

1. Register name Test (1)
2. Register address
   [Write]

A_3	A_2	A_1	A_0
1	0	0	0

3. Register bit assignment

	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Default	X	X	X	0	0	0	0	0	0	0
Functions										
ADIN test mode				<->						

NOTE : X : Don't care

D_5 to D_0 must always be "0".

4. Register operations

	CONTROLS										OPERATIONS
	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
ADIN test mode				0							Normal operation
				1							V_{COM} centered ADIN for AC coupling

The Test register (D_6) is for the AC coupled ADIN input mode. At this mode, the DC bias becomes the V_{COM} voltage and no clamp signals are required. Connect a 50 kΩ resistor between the ADIN (pin 14) and CLPCAP (pin 13), and input the signal to the ADIN pin via a capacitor.

1. Register name Test (2)
2. Register address
   [Write]

A_3	A_2	A_1	A_0
1	0	0	1

3. Register bit assignment

	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Default	X	X	X	X	X	0	0	0	0	0
Functions										
Test modes						<----------				----->

NOTE : X : Don't care

D_4 to D_0 must always be "0".

ABSOLUTE MAXIMUM RATINGS

(AV_{SS} = DV_{SS} = 0 V, all voltages are with respect to GND.)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT	NOTE
Power supply voltage	AV_{DD}		–0.3 to +4.5	V	
	DV_{DD}		–0.3 to +4.5 or AV_{DD} + 0.3	V	1
Voltage difference	V_{DLT}	DV_{DD} – AV_{DD}	0.3	V	
Power consumption	P_D	$T_A \leq 25°C$	570	mW	
P_D derating ratio		$T_A > 25°C$	4.5	mW/°C	
Input current	I_{IN}	Except power supply pins	±10	mA	
Analog input voltage	V_{INA}		AV_{SS} – 0.3 to AV_{DD} + 0.3	V	
Digital input voltage (Input pin)	V_{INL}		AV_{SS} – 0.3 to AV_{DD} + 0.3	V	
Digital input voltage (Output pin)	V_{ONL}		AV_{SS} – 0.3 to AV_{DD} + 0.3	V	2
Operating temperature	T_{OPR}		–30 to +85	°C	
Storage temperature	T_{STG}		–40 to +125	°C	

NOTES :

1. The higher voltage of 4.5 V or AV_{DD} + 0.3 V specifies maximum value of DV_{DD} absolute maximum rating.
2. The V_{ONL} limits the excess voltage applied to digital output pins.

WARNING :

Operation at or beyond these limits may result in permanent damage to the device. Normal operating specifications are not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AV_{SS} = DV_{SS} = 0 V, all voltages are with respect to GND.)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage	Analog	AV_{DD}	At start-up, turn on AV_{DD} before (or at the same time as) turning on DV_{DD}.	2.7	3.0	3.6	V
	Digital output	DV_{DD}		2.7	3.0	AV_{DD}	V

ELECTRICAL CHARACTERISTICS

Supply Current (NOTE 1)

(T_A = +25°C, AV_{DD} = DV_{DD} = 3.0 V)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply current at	Analog	I_A	fs = 18 MHz		28	31	mA	2
normal operation	Digital	I_D			5	7	mA	2, 3
Supply current at monitor active		I_{PE}	fs = 18 MHz		30	34	mA	3
Supply current at power down		I_{PD}				0.1	mA	4

NOTES :

1. Specified at a 4.7 kΩ AISET resistance. Use a high precision resistor because it influences the supply current.
2. Specified when the monitor function is off.
3. Measured when connecting 10 pF capacitors between the DO_0 to DO_9 pins and GND, and inputting full scale of 1 MHz sine wave to the ADC.
4. Measured under no analog input and with clock fixed at low.

Analog Specifications

(Unless otherwise specified, AV_{DD} = DV_{DD} = 3.0 V, T_A = +25°C, signal frequency f_{IN} = 1 MHz, signal level = full scale – 1 dB.)
The current direction flowing into the pin is positive direction.

CDS & CLAMP CIRCUITS (Sampling frequency f_S = 18 MHz)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Analog input range	V_{ICDS}	CCDIN input			1.1		Vp-p	1
	V_{IAI}	ADIN input			1.0		Vp-p	
Equivalent input noise	NI	At fs = 18 MHz	At max. gain		50		μV_{rms}	2
			At min. gain		200		μV_{rms}	
Input capacitance	C_{IN}	CCDIN, ADIN & REFIN			15		pF	
Input bandwidth	CBW					1	pixel	3
Clamp voltage	V_{CLPCAP}	CCDIN input		1.65	1.8	1.95	V	
		ADIN input		1.15	1.3	1.45	V	
Black calibration time	t_{BKCAL}					200	pixel	4
Maximum calibratable offset voltage	V_{BKCAL}				±200		mV	5

NOTES :

1. The signal dynamic range is below the clamp voltage at the CCDIN input, and it is above the one at the ADIN input. The V_{ICDS} is applied at the 0 dB gain. When the gain is below 0 dB, V_{ICDS} is 1.25 Vp-p (TYP.).
2. Measured at the MONOUT pin. The noise bandwidth is 100 kHz to 5 MHz.
3. The bandwidth from the CCDIN/REFIN to the ADC. This is defined as the settling time of the ADC when the full scale – 1 dB step input is inputted and the gain is 0 dB.
4. The time that is needed to settle the average value within ±1 LSB for the set code when the PGA gain is changed. (The OBCAP capacitor is 0.1 µF.)
   The value of the OBCAP capacitor determines the bandwidth of the black calibration loop. The loop gain is also affected by the operation frequency. Therefore the maximum frequency that is needed to settle within a limited time and the minimum frequency that is needed to avoid the undesirable oscillation are defined corresponding with the external capacitance. Refer to the table below to select the capacitance.

OBCAP CAPACITANCE (µF)	MINIMUM FREQUENCY (MHz)	MAXIMUM FREQUENCY (MHz)	
		Within 200 pixels	Within 400 pixels
0.068	11	Up to 18	Up to 18
0.1	8	Up to 18	Up to 18
0.15	4	Up to 14	Up to 18
0.33	3	Up to 6	Up to 10

5. The maximum calibratable offset means the difference of the CCDIN reference level and the set data at the OBP period.

GAIN

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
CDS gain	select 0 dB	G_{MNN}	Absolute gain	−1.9	−0.9	0.1	dB	1
	select 6.02 dB	G (1)	Relative gain	5.52	6.02	6.52	dB	
	select 12.04 dB	G (2)		11.54	12.04	12.04	dB	
	select −1.94 dB	G (3)		−2.44	−1.94	−1.44	dB	
PGA input	Minimum gain	G_{MNNA}	Absolute gain	−1.3	−0.3	0.7	dB	1
	Maximum gain	G_{MXNA}	Relative gain	22.906	23.906	24.906	dB	
	Gain step	G_{STA}		0	0.047	0.094	dB	
Total (CDS + PGA) gain monotonicity		ER_{PA}				±2	LSB	2

NOTES :

1. Measured at the digital output pins (DO_0 to DO_9). When the input voltage is 1.0 Vp-p and ADC output is the full scale, the absolute gain is defined as a 0 dB. The relative gain is the relative value from the absolute gain. The gain monotonicity is guaranteed except least significant bit.
2. Measured at the digital output pins (DO_0 to DO_9).

A/D CONVERTER CIRCUIT (fs = 18 MHz, Input signals to ADIN.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Resolution	RES				10	bits	
Differential nonlinearity	DNL	fs = 18 MHz		±0.6	±1.0	LSB	1
S/N	SN			58		dB	
S/(N + D)	SND			56		dB	
ADC common voltage	V_{COM}		1.0	1.1	1.2	V	
V_{REF} voltage (positive)	V_{RP}		1.25	1.35	1.45	V	
V_{REF} voltage (negative)	V_{RN}		0.75	0.85	0.95	V	
ADC output black level calibration code	C_{CAL}		16		127	LSB	
			1		127	LSB	2
Calibration code resolution	ST_{CAL}			1		LSB	

NOTES :

1. Non missing code is guaranteed.
2. Black calibration period (t_{BKCAL}) is specified when the C_{CAL} is from 16 to 127 LSB.
   Although black level codes of 1 to 15 could be set, t_{BKCAL} is not guaranteed for these codes.

Switching Characteristics

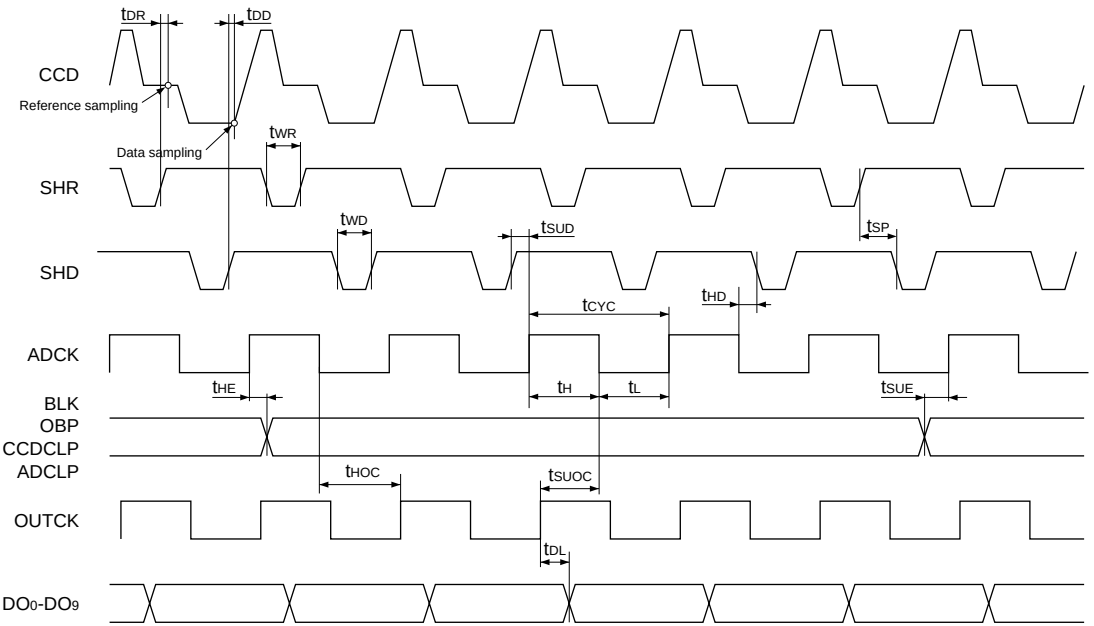
(AV_{DD}, DV_{DD} = 2.7 to 3.6 V, AV_{SS}, DV_{SS} = 0 V, T_A = –30 to +85°C, C_L < 10 pF)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Conversion frequency	f_S		0.5		18	MHz	
Clock cycle time	t_{CYC}		55			ns	
Clock rise time	t_R	(30%→70%) AV_{DD}, DV_{DD}			2	ns	
Clock fall time	t_F	(70%→30%) AV_{DD}, DV_{DD}			2	ns	
Clock low period	t_L		23			ns	
Clock high period	t_H		23			ns	
SHR pulse width	t_{WR}		11			ns	
SHD pulse width	t_{WD}		11			ns	
SHR sampling aperture	t_{DR}				4	ns	
SHD sampling aperture	t_{DD}				4	ns	
Data pulse setup	t_{SUD}		2			ns	1
Data pulse hold	t_{HD}		5			ns	
Sampling pulse non-overlap	t_{SP}		1			ns	
Enable pulse setup	t_{SUE}		10			ns	
Enable pulse hold	t_{HE}		10			ns	
OUTCK setup	t_{SUOC}		0			ns	
OUTCK hold	t_{HOC}		10			ns	
3 state disable delay	t_{DLD}	Active→High-Z		20		ns	
3 state enable delay	t_{DLE}	High-Z→Active		20		ns	
ADC output data delay	t_{DL1}		2			ns	
	t_{DL2}				35	ns	

NOTE :

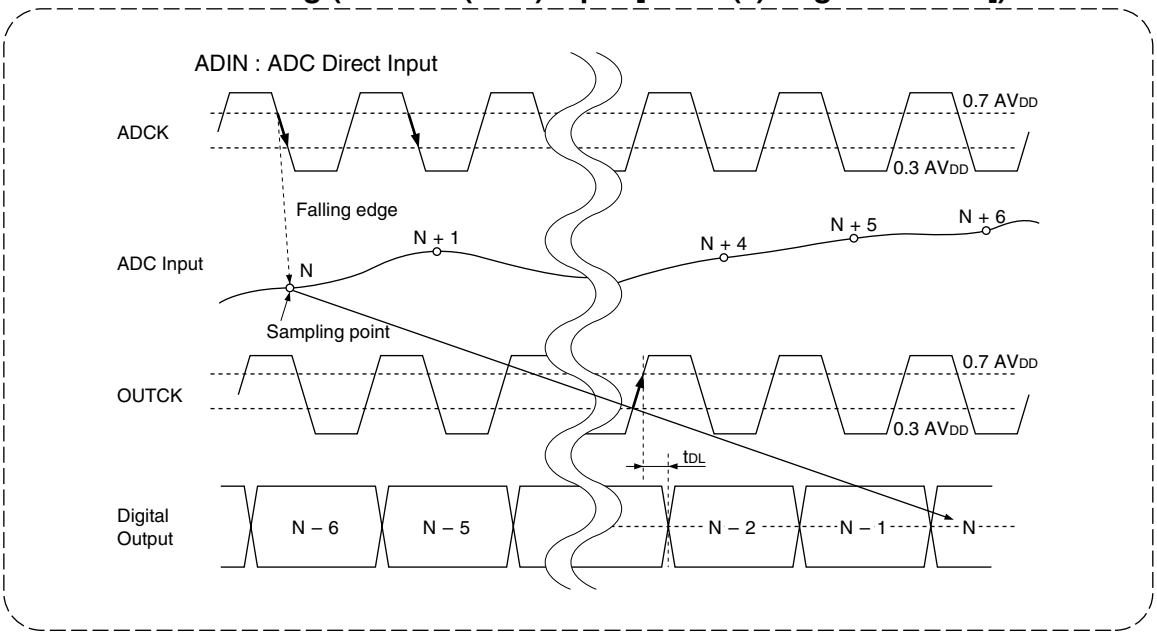
1. When SHD ↑ is earlier than ADCK ↓, assumed positive.
   (In the above table, SHD ↑ must be earlier at least 2 ns than ADCK ↑.)

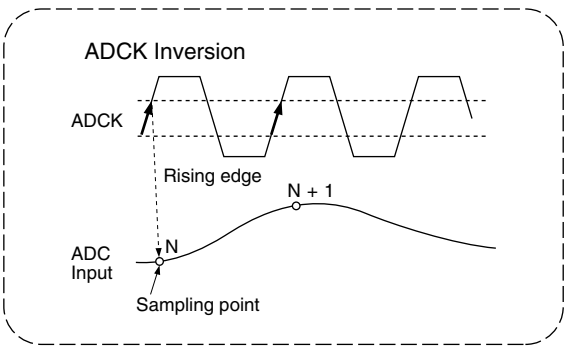
TIMING CHART

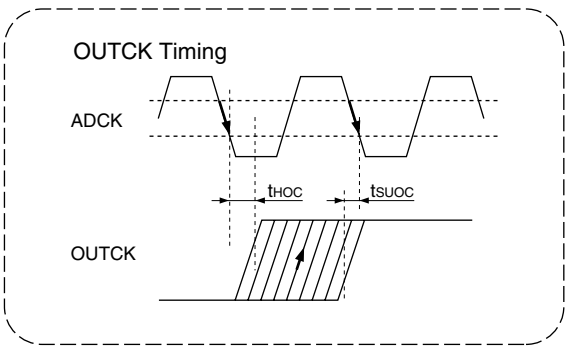


This chart is shown when the Mode (1) D_8 bit is set to "1", and an external clock is input to the OUTCK pin. When setting D_8 bit to "0", the ADCK is used as OUTCK.

AD Conversion Timing (At ADIN (ADC) Input [Mode (1) Register D_5 = 1])







These figures are shown when the Mode (1) D_8 bit is set to "1", and an external clock is input to the OUTCK pin. When setting D_8 bit to "0", the ADCK is used as OUTCK.

NOTE :

At default condition in ADIN mode, data are sampled at the falling edge of the ADCK clock, and are output at the rising edge of the OUTCK clock. When the data are sampled and are output at the falling edge of the ADCK clock, set ADCK polarity register to "1".

(The upper figure on the previous page shows default timing, and the lower left figure on the previous page shows inverted timing.)

Delay from data sampling to data output

ADCK normal : At [Mode (1) Register D_6 = 0]

5.5 clk delay

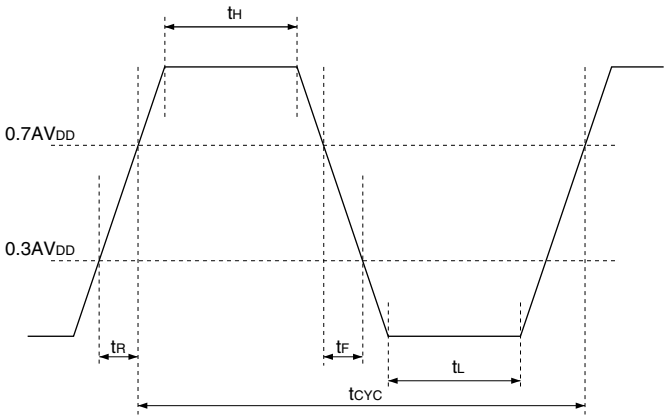
ADCK inversion : At [Mode (1) Register D_6 = 1]

6.0 clk delay

In ADIN input mode, the above-mentioned register setting is available.

At ADIN (PGA) input [Mode (1) Register D_5 = 0 & D_4 = 1] digital data output is delayed from above timing by 2 clk.

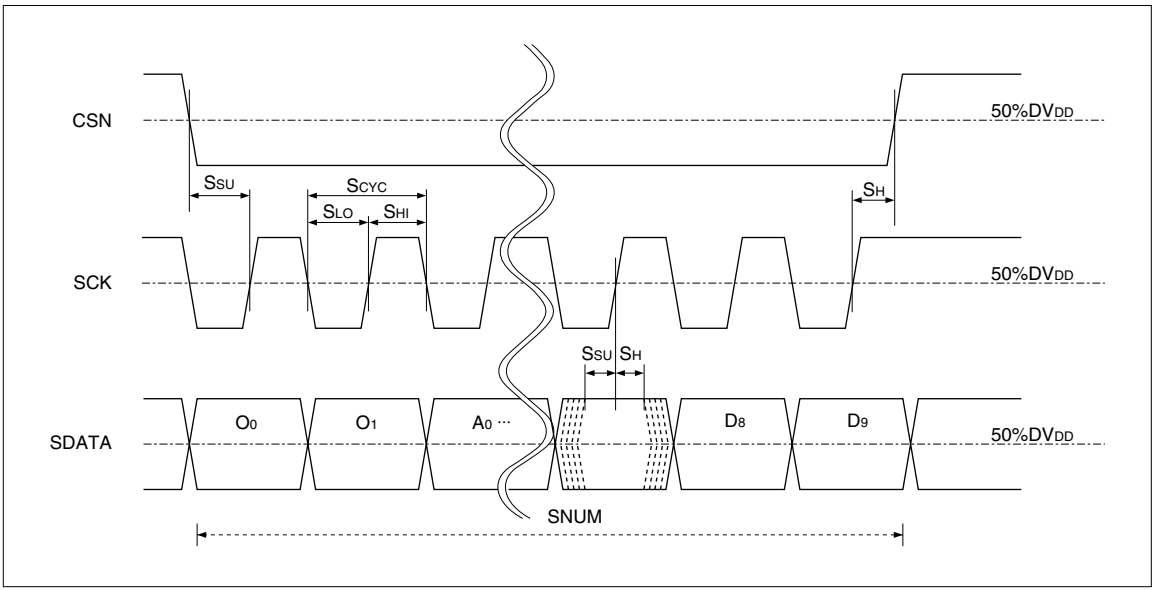
ADCK Clock Waveform



CONTROL INTERFACE TIMING

(AV_{DD}, DV_{DD} = 2.7 to 3.6 V, AV_{SS}, DV_{SS} = 0 V, T_A = −30 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCK clock frequency	S_{CYC}				10	MHz
SCK clock low level width	S_{LO}		40			ns
SCK clock high level width	S_{HI}		40			ns
Data setup time	S_{SU}		20			ns
Data hold time	S_H		20			ns
SCK, CSN rise time	S_R	30%→70%			6	ns
SCK, CSN fall time	S_F	70%→30%			6	ns
Number of serial data	SNUM			16		pcs



Serial I/F Timing

Digital DC Characteristics

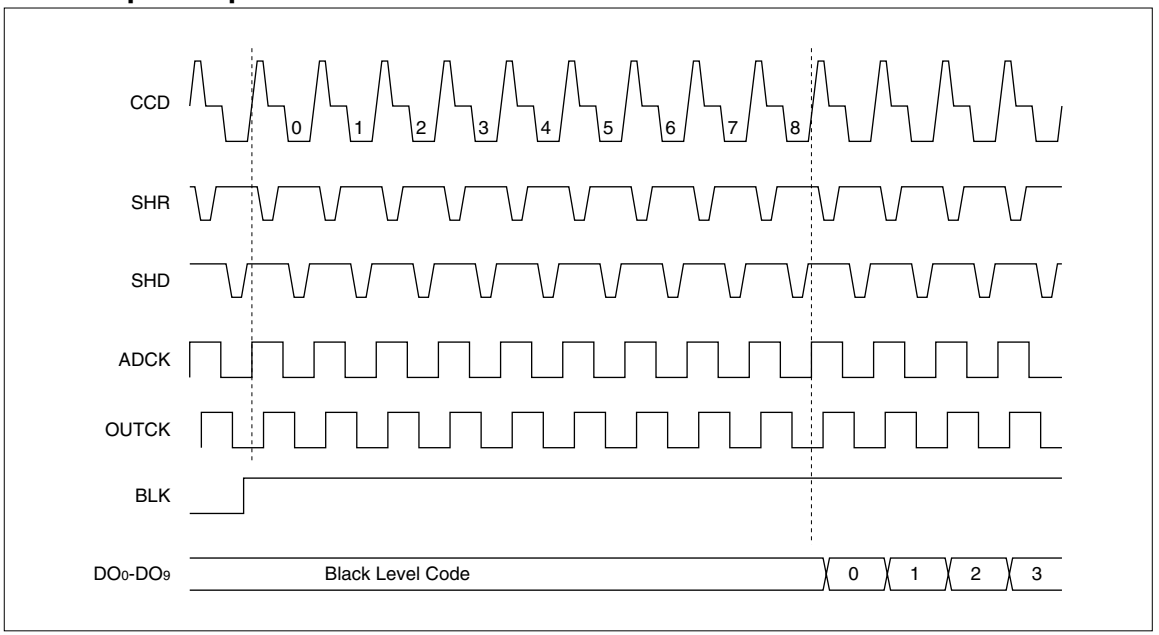
(AV_{DD}, DV_{DD} = 2.7 to 3.6 V, AV_{SS}, DV_{SS} = 0 V, T_A = −30 to +85°C, Measured as a DC characteristics.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL1}				0.3AV_{DD}	V	1
Input "High" voltage	V_{IH1}		0.7AV_{DD}			V	
Output "Low" voltage	V_{OL}	I_{OL} = 1 mA			0.3DV_{DD}	V	
Output "High" voltage	V_{OH}	I_{OH} = −1 mA	0.7DV_{DD}			V	
Input "High" leakage current	I_{LIKG}				±10	µA	
High-Z leakage current	I_{OZ}				±10	µA	

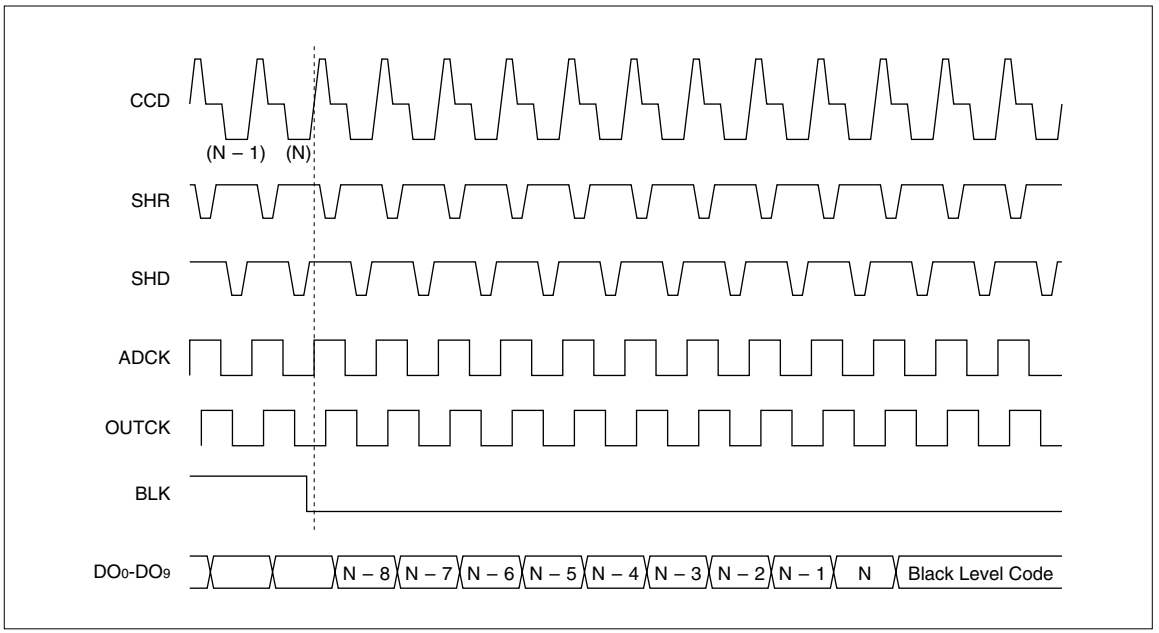
NOTE :

1. Applied to SHD, SHR, ADCK, BLK, OBP, CCDCLP, ADCLP, CSN, SCK, SDATA, RESETN, STBYN and OUTCK.

Data Output Sequence



Pixel Data Readout Sequence (1) : Conversion Start

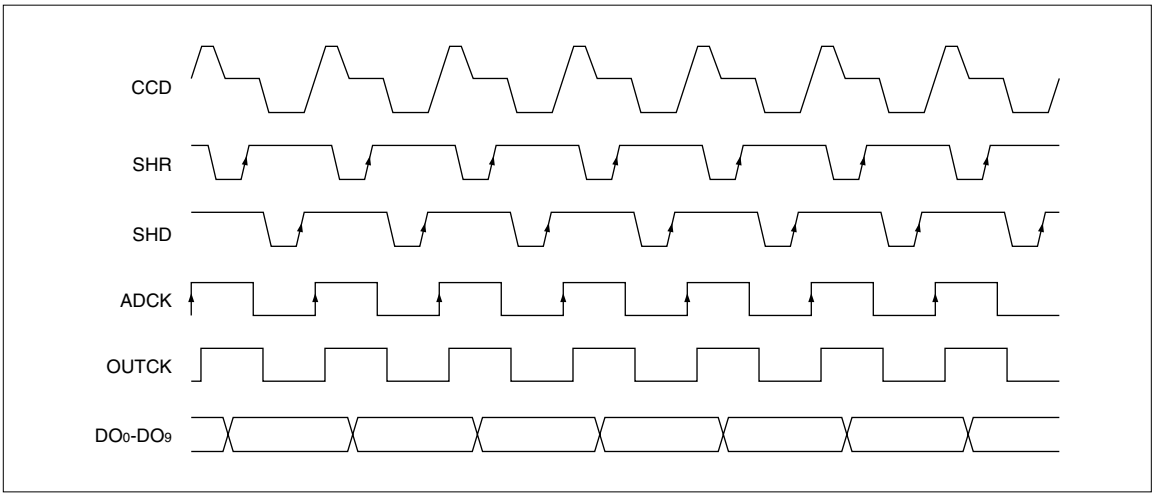


Pixel Data Readout Sequence (2) : Conversion End

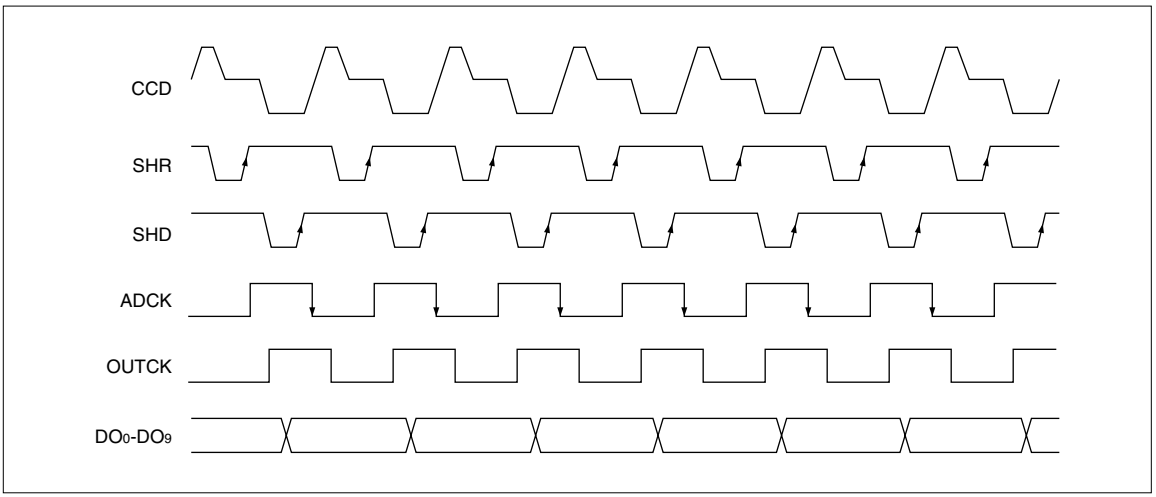
Clock Timing Variations by Register Setting

The variations of clock timings when it is inverted by register settings.

1. No inversion
   (Mode (1) Register D_6 = 0, Mode (2) Register D_2 = 0; Default) (Upper figure)
2. ADCK inversion
   (Mode (1) Register D_6 = 1, Mode (2) Register D_2 = 0) (Lower figure)



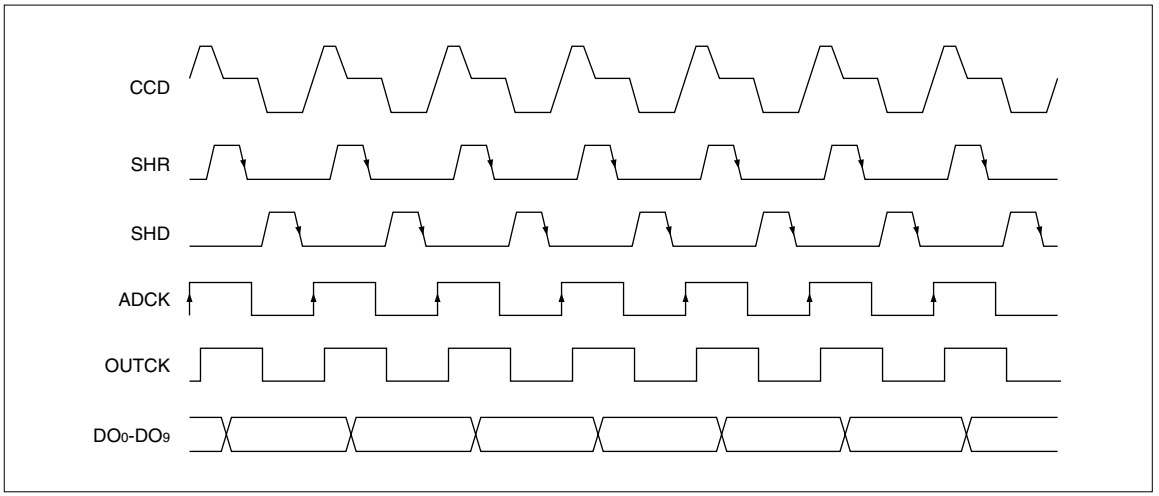
Pulse Control (Default : No Inversion)



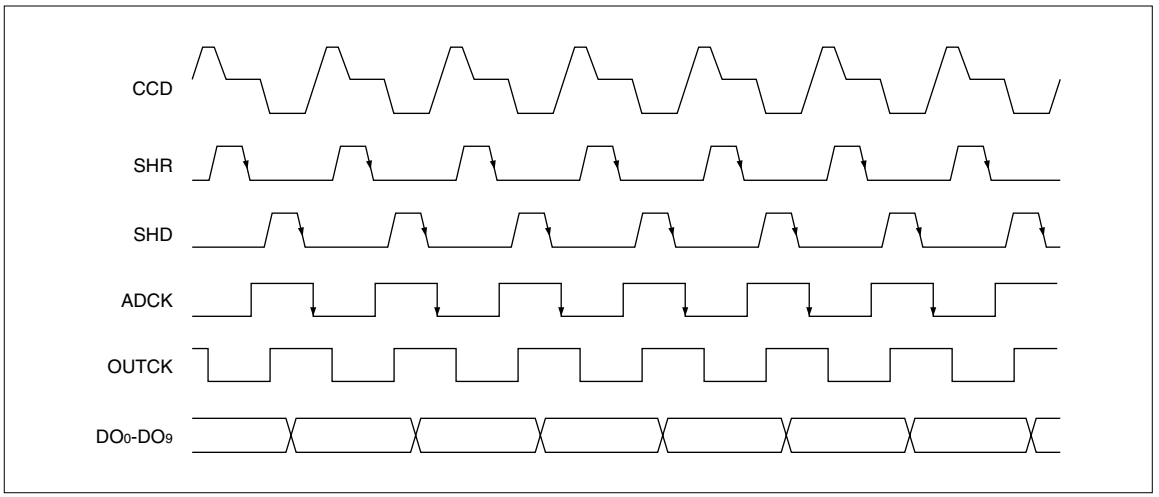
Pulse Control (ADCK Inversion)

3. SHR & SHD inversion
(Mode (1) Register D_6 = 0, Mode (2) Register D_2 = 1) (Upper figure)

4. ADCK, SHR & SHD inversion
(Mode (1) Register D_6 = 1, Mode (2) Register D_2 = 1) (Lower figure)



Pulse Control (SHR & SHD Inversion)



Pulse Control (ADCK, SHR & SHD Inversion)

APPLICATION CIRCUIT EXAMPLE

The following schematic is the reference circuit for system design.
Optimize capacitance and resistance according to the system environment.