

IR53H(D)420(-P2)

SELF-OSCILLATING HALF BRIDGE

Features

- Output power MOSFETs in half-bridge configuration
- High side gate drive designed for bootstrap operation
- Bootstrap diode integrated into package (HD type)
- Tighter initial deadtime control
- Low temperature coefficient deadtime
- 15.6V zener clamped V_{CC} for offline operation
- Half-bridge output is out of phase with R_T
- True micropower startup
- Shutdown feature (1/6th V_{CC}) on C_T lead
- Increased undervoltage lockout hysteresis (1Volt)
- Lower power level-shifting circuit
- Lower di/dt gate drive for better noise immunity
- Excellent latch immunity on all inputs and outputs
- ESD protection on all leads
- Constant V_O pulse width at startup
- Heatsink package version (P2 type)

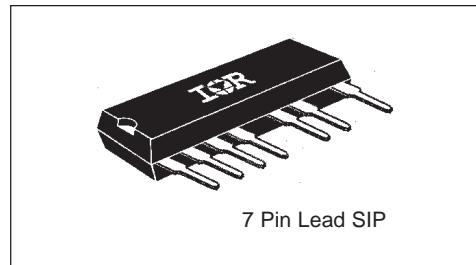
Description

The IR53H(D)420(-P2) are complete high voltage, high speed, self-oscillating half-bridge circuits. Proprietary HVIC and latch immune CMOS technologies, along with the HEXFET® power MOSFET technology, enable ruggedized single package construction. The front-end features a programmable oscillator which functions similar to the CMOS 555 timer. The supply to the control circuit has a zener clamp to simplify offline operation. The output features two HEXFETs in a half-bridge configuration with an internally set deadtime designed for minimum cross-conduction in the half-bridge. Propagation delays

Product Summary

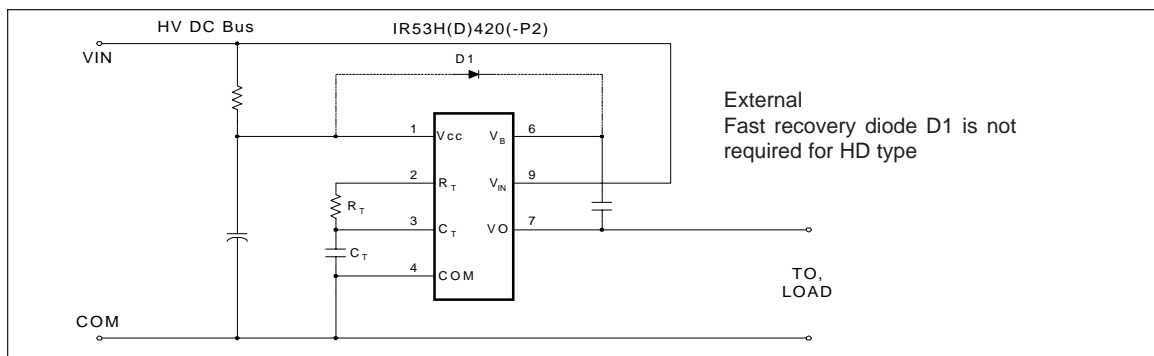
V _{IN} (max)	500V
Duty Cycle	50%
Deadtime (type.)	1.2μs
R _{ds(on)}	3.0Ω
P _D (T _A = 25°C)	2.0W or 3.0W

Package



for the high and low side power MOSFETs are matched to simplify use in 50% duty cycle applications. The device can operate up to the V_{IN} (max) rating.

Typical Connection



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, unless stated otherwise. All currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

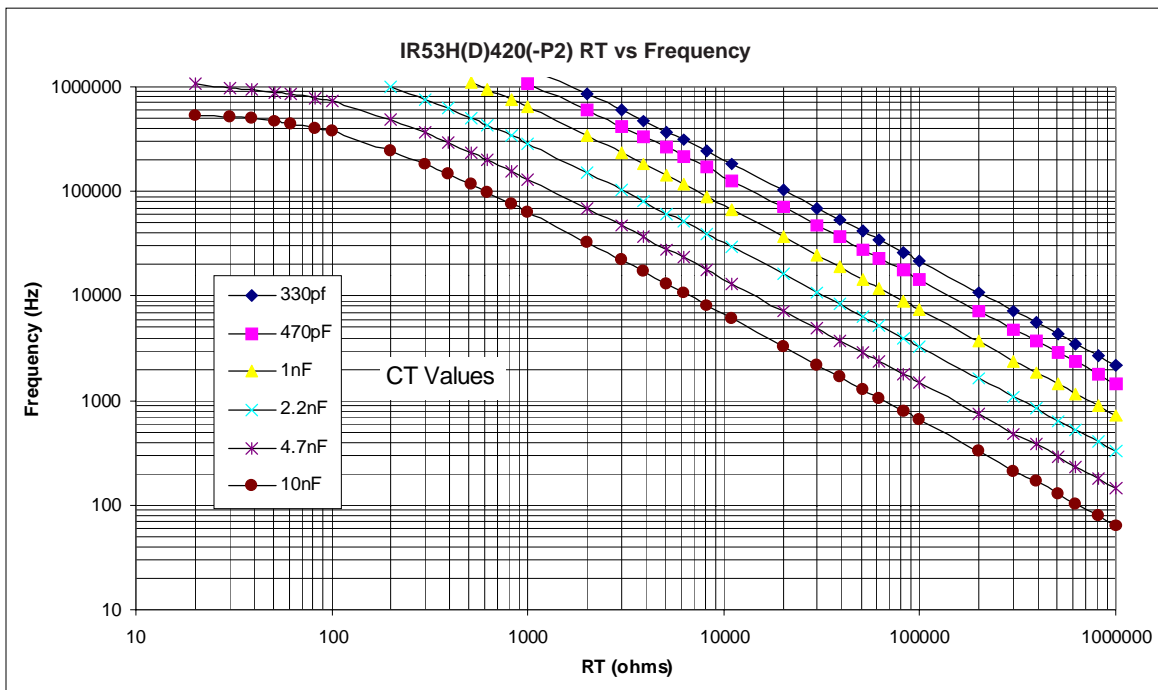
Symbol	Definition	Minimum	Maximum	Units	
V_{IN}	High voltage supply	- 0.3	500	V	
V_B	High side floating supply	$V_O - 0.3$	$V_O + 25$		
V_O	Half-bridge output	-0.3	$V_{IN} + 0.3$		
V_{RT}	R_T voltage	- 0.3	$V_{CC} + 0.3$		
V_{CT}	C_T voltage	- 0.3	$V_{CC} + 0.3$		
I_{CC}	Supply current (note 1)	—	25	mA	
I_{RT}	R_T output current	- 5	5	W	
dV/dt	Peak diode recovery	—	3.50		V/ns
P_D	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	—	2		
		-P2	3		
R_{thJA}	Thermal resistance, junction to ambient	—	60	$^\circ\text{C}/\text{W}$	
		-P2	40		
R_{thJC}	Thermal resistance, junction to case (heatsink)	-P2	20		
T_J	Junction temperature	-55	150		
T_S	Storage temperature	-55	150	$^\circ\text{C}$	
T_L	Lead temperature (soldering, 10 seconds)	—	300		

NOTE 1:

This IC contains a zener clamp structure between V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics Section

Recommended Component Values

Symbol	Definition	Minimum	Maximum	Units
R_T	Timing resistor value	10	—	$k\Omega$
C_T	C_T pin capacitor value	330	—	pF



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Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation, the device should be used within the recommended conditions.

Symbol	Definition	Minimum	Maximum	Units
V_B	High side floating supply absolute voltage	$V_O + 10$	$V_O + V_{clamp}$	V
V_{IN}	High voltage supply	—	500	
V_O	Half-bridge output voltage	-3.0 (note 3)	500	
I_D	Continuous drain current (TA = 25°C)	—	0.7	A
		-P2	0.85	
		(TA = 85°C)	0.5	
		-P2	0.6	
		(TC = 25°C) -P2	1.2	
I_{CC}	Supply current	(note 3)	5	mA
T_A	Ambient temperature	-40	125	°C

NOTE 2:

Care should be taken to avoid switching conditions where the V_S node flies inductively below ground by more than 5V.

NOTE 3:

Enough current should be supplied to the V_{CC} lead of the IC to keep the internal 15.6V zener diode clamping the voltage at this lead.

Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 12V, C_T = 1 nF and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM.

MOSFET Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{rr}	Reverse recovery time (MOSFET body diode)	—	240	—		$I_F=700mA$ $di/dt = 100 A/\mu s$
Q_{rr}	Reverse recovery charge (MOSFET body diode)	—	0.5	—	μC	
$R_{ds(on)}$	Static drain-to-source on resistance	—	3.0	—	Ω	
V_{SD}	Diode forward voltage	—	0.8	—	V	
Dynamic Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
D	RT duty cycle	—	50	—	%	fosc = 20 kHz
tsd	Shutdown propagation delay	—	660	—	nsec	

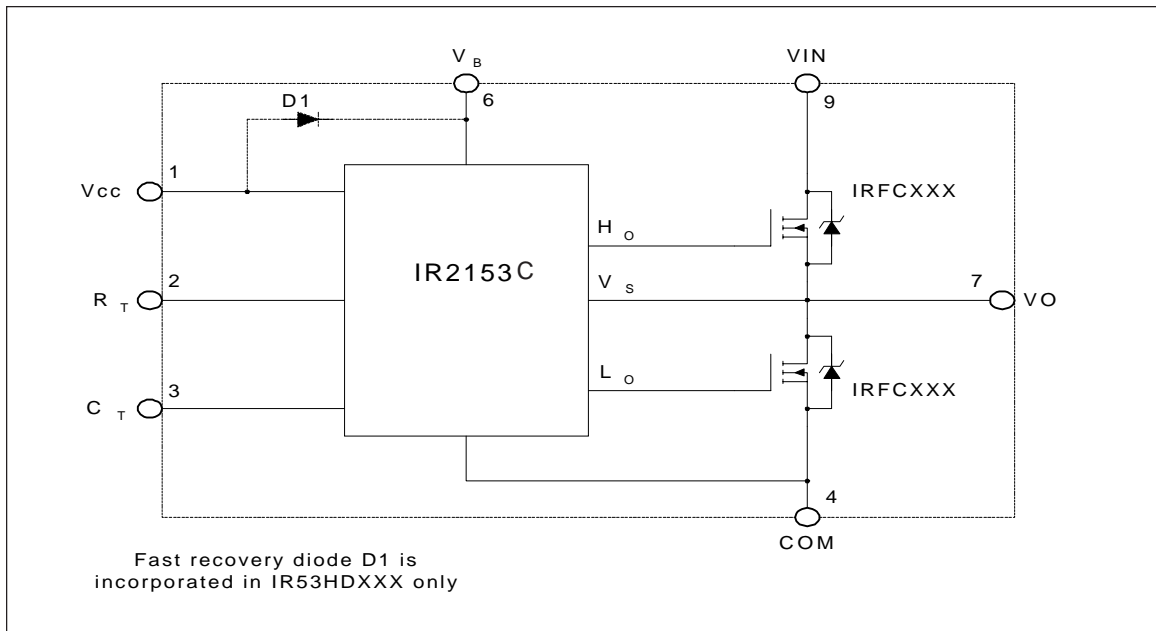
Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 12V, C_T = 1 nF and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM.

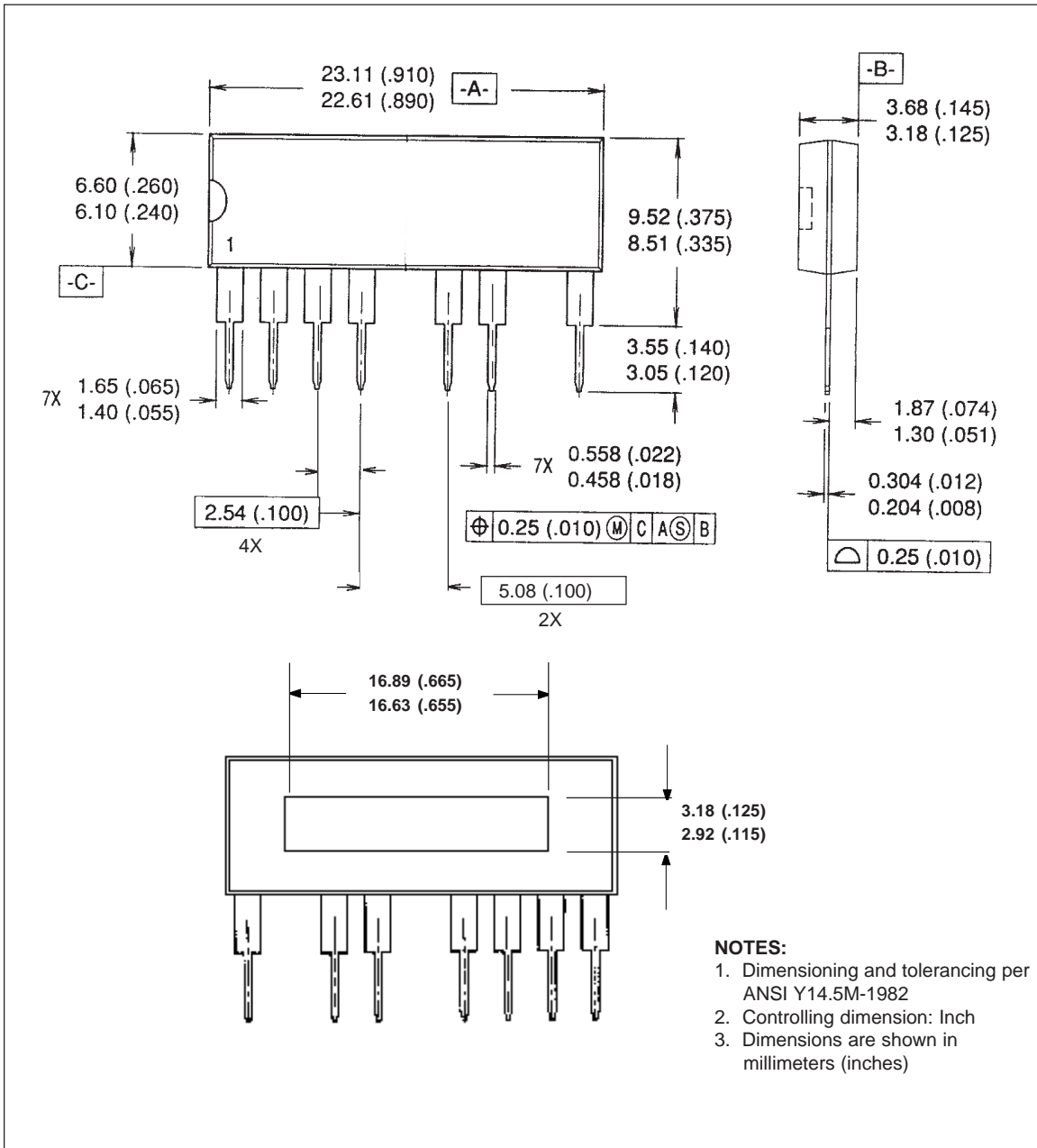
Low Voltage Supply Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	Rising V_{CC} undervoltage lockout threshold	8.1	9.0	9.9	V	
V_{CCUV-}	Falling V_{CC} undervoltage lockout threshold	7.2	8.0	8.8		
V_{CCUVH}	V_{CC} undervoltage lockout Hysteresis	0.5	1.0	1.5		
I_{QCCUV}	Micropower startup V_{CC} supply current	—	75	150	μ A	$V_{CC} \leq V_{CCUV-}$
I_{QCC}	Quiescent V_{CC} supply current	—	500	950		
V_{CLAMP}	V_{CC} zener clamp voltage	14.4	15.6	16.8	V	$I_{CC} = 5mA$
Floating Supply Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{QBSUV}	Micropower startup V_{BS} supply current	—	0	10	μ A	$V_{CC} \leq V_{CCUV-}$
I_{QBS}	Quiescent V_{BS} supply current	—	30	50		
V_{BSMIN}	Minimum required V_{BS} voltage for proper functionality from R_T to HO	—	4.0	5.0	V	$V_{CC} = V_{CCUV+} + 0.1V$
I_{OS}	Offset supply leakage current	—	—	50	μ A	$V_B = V_S = 600V$
V_F	Bootstrap diode forward voltage (IR2153D)	0.5	—	1.0	V	$I_F = 250mA$
Oscillator I/O Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
f_{osc}	Oscillator frequency	19.4	20	20.6	kHz	$R_T = 36.9k\Omega$
		94	100	106		$R_T = 7.43k\Omega$
d	R_T pin duty cycle	48	50	52	%	$f_o < 100kHz$
I_{CT}	C_T pin current	—	0.001	1.0	μ A	
I_{CTUV}	UV-mode C_T pin pulldown current	0.30	0.70	1.2	mA	$V_{CC} = 7V$
V_{CT+}	Upper C_T ramp voltage threshold	—	8.0	—	V	
V_{CT-}	Lower C_T ramp voltage threshold	—	4.0	—		
V_{CTSD}	C_T voltage shutdown threshold	1.8	2.1	2.4		
V_{RT+}	High-level R_T output voltage, $V_{CC} - V_{RT}$	—	10	50	mV	$I_{RT} = 100\mu A$
		—	100	300		$I_{RT} = 1mA$
V_{RT-}	Low-level R_T output voltage	—	10	50		$I_{RT} = 100\mu A$
		—	100	300		$I_{RT} = 1mA$
V_{RTUV}	UV-mode R_T output voltage	—	0	100		$V_{CC} \leq V_{CCUV-}$
V_{RTSD}	SD-Mode R_T output voltage, $V_{CC} - V_{RT}$	—	10	50		$I_{RT} = 100\mu A$, $V_{CT} = 0V$
		—	10	300	$I_{RT} = 1mA$, $V_{CT} = 0V$	

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Functional Block Diagram



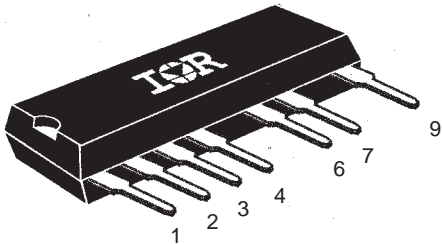
Case Outline - 7 pin



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International
IR Rectifier

Lead Assignments



1	V_{CC}	6	V_B
2	R_T	7	VO
3	C_T	9	V_{IN}
4	COM		

9 Lead SIP without Leads 5 and 8

Lead Definitions

Symbol	Lead Description
V_{CC}	Logic and internal gate drive supply voltage.
R_T	Oscillator timing resistor output
C_T	Oscillator timing capacitor input
V_B	High side gate drive floating supply.
V_{IN}	High voltage supply
VO	Half Bridge output
COM	Logic and low side of half bridge return

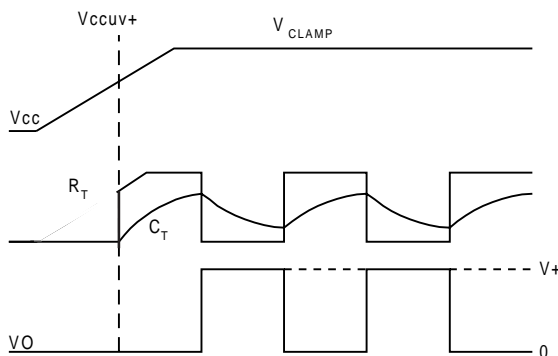


Figure 1. Input/Output Timing Diagram

International
IR Rectifier

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Data and specifications subject to change without notice. 3/22/99