

# KA3882C/KA3883C

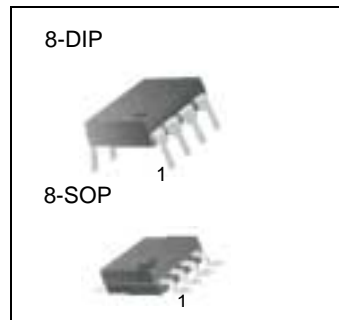
## SMPS Controller

### Features

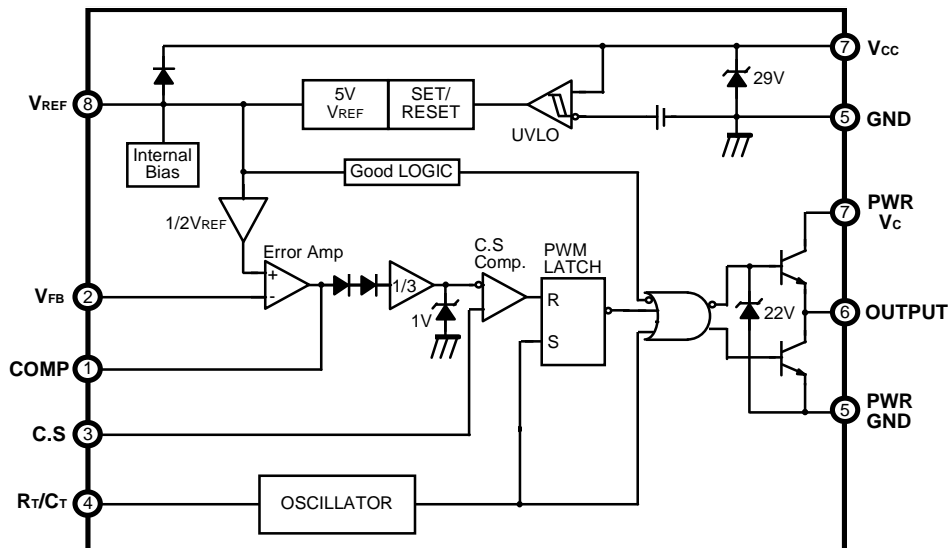
- Low Start Current 0.2mA (typ)
- Operating Range Up To 500KHz
- Cycle by Cycle Current Limiting
- Under Voltage Lock Out With Hysteresis
- Short Shutdown Delay Time: typ.100ns
- High Current Totem-pole Output
- Output Swing Limiting: 22V

### Description

The KA3882C/KA3883C are fixed PWM controller for Off-Line and DC to DC converter applications. The internal circuits include UVLO, low start up current circuit, temperature compensated reference, high gain error amplifier, current sensing comparator, and high current totem pole output for driving a POWER MOSFET. Also KA3882C/KA3883C provide low start up current below 0.3mA and short shutdown delay time typ. 100ns. The KA3882C has UVLO threshold of 16V(on) and 10V(off). The KA3883C is 8.4V(on) and 7.6V(off). The KA3882C and KA3883C can operate within 100% duty cycle.



### Internal Block Diagram



## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	30	V
Output Current	I <sub>O</sub>	± 1	A
Analog Inputs (pin 2, 3)	V <sub>I(ANA)</sub>	- 0.3 to 6.3	V
Error Amp. Output Sink Current	I <sub>SINK(EA)</sub>	10	mA
Power Dissipation	P <sub>D</sub>	1	W
Thermal Resistance, Junction-to-Air (Note4)	R <sub>θja</sub>	280	°C/W
8-SOP		95	
8-DIP			

## Electrical Characteristics

(V<sub>CC</sub> = 15V, R<sub>T</sub> = 10KΩ, C<sub>T</sub> = 3.3nF, T<sub>A</sub> = 0°C to + 70°C ,Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>REFERENCE SECTION</b>						
Output Voltage	V <sub>REF</sub>	T <sub>J</sub> = 25°C, I <sub>O</sub> = 1mA	4.9	5.0	5.1	V
Line Regulation	ΔV <sub>REF</sub>	V <sub>CC</sub> = 12V to 25V	-	6	20	mV
Load Regulation	ΔV <sub>REF</sub>	I <sub>O</sub> = 1mA to 20mA	-	6	25	mV
Output Short Circuit	I <sub>SC</sub>	T <sub>a</sub> = 25°C	-	- 100	- 180	mA
<b>OSILLATOR SECTION</b>						
Initial Accuracy	F <sub>OSC</sub>	T <sub>J</sub> = 25°C	47	52	57	KHz
Voltage Stability	ST <sub>V</sub>	V <sub>CC</sub> = 12V to 25V	-	0.2	1	%
Amplitude	V <sub>O</sub> SC	V <sub>PIN4</sub> , Peak to Peak	-	1.7	-	V
Discharge Current	I <sub>DISCHG</sub>	T <sub>J</sub> = 25°C, Pin4 = 2V	7.8	8.3	8.8	mA
<b>CURRENT SENSE SECTION</b>						
Gain	G <sub>V</sub>	(NOTE 2, 3)	2.85	3	3.15	V/V
Maximum Input Signal	V <sub>I(MAX)</sub>	V <sub>PIN1</sub> = 5V(NOTE 2)	0.9	1.0	1.1	V
PSRR	PSRR	V <sub>CC</sub> = 12V to 25V (NOTE 1, 2)	-	70	-	dB
Input Bias Current	I <sub>BIAS</sub>	-	-	- 2	-10	uA
Delay to Output	T <sub>D</sub>	V <sub>PIN3</sub> = 0 V to 2V (NOTE1)	-	100	200	ns

## Electrical Characteristics (Continued)

( $V_{CC} = 15V$ ,  $R_T = 10K\Omega$ ,  $C_T = 3.3nF$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ , Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>ERROR AMPLIFIER SECTION</b>						
Input Voltage	$V_I$	$T_{PIN1} = 2.5V$	2.42	2.50	2.58	V
Input Bias Current	$I_{BIAS}$	-	-	-0.3	-2	$\mu A$
Open Loop Gain	$G_{VO}$	$V_O = 2V$ to $4V$ (NOTE 1)	65	90	-	dB
Unity Gain Bandwidth	GBW	$T_J = 25^\circ C$ (NOTE 1)	0.7	1	-	MHz
PSRR	PSRR	$V_{CC} = 12V$ to $25V$ (NOTE 1)	60	70	-	dB
Output Sink Current	$I_{SINK}$	$V_{PIN2} = 2.7V$ $V_{PIN1} = 1.1V$	2	6	-	mA
Output Source Current	$I_{SOURCE}$	$V_{PIN2} = 2.3V$ $V_{PIN1} = 5.0V$	-0.5	-0.8	-	mA
Output High Voltage	$V_{OH}$	$V_{PIN2} = 2.3V$ $R_1 = 15K\Omega$ to GND	5	6	-	V
Output Low Voltage	$V_{OL}$	$V_{PIN2} = 2.7V$ $R_1 = 15K\Omega$ to Pin8	-	0.8	1.1	V
<b>OUTPUT SECTION</b>						
Output Low Level	$V_{OL}$	$I_{SINK} = 20mA$	-	0.1	0.4	V
		$I_{SINK} = 200mA$	-	1.5	2.2	V
Output High Level	$V_{OH}$	$I_{SOURCE} = 20mA$	13	13.5	-	V
		$I_{SOURCE} = 200mA$	12	13.5	-	V
Rise Time	$t_R$	$T_J = 25^\circ C$ , $C_1 = 1nF$ (NOTE 1)	-	40	100	ns
Fall Time	$t_F$	$T_J = 25^\circ C$ , $C_1 = 1nF$ (NOTE 1)	-	40	100	ns
Output Voltage Swing Limit	$V_{OLIM}$	$V_{CC} = 27V$ , $C_1 = 1nF$	-	22	-	V
<b>UNDER VOLTAGE LOCKOUT SECTION</b>						
Start Threshold	$V_{TH}$	KA3882C	15	16	17	V
		KA3883C	7.8	8.4	9.0	V
Min. Operating Voltage ( After turn on )	$V_{TL}$	KA3882C	9	10	11	V
		KA3883C	7.0	7.6	8.2	V
<b>PWM SECTION</b>						
Maximum Duty Cycle	$D_{MAX}$	KA3882C/KA3883C	94	96	100	%
Minimum Duty Cycle	$D_{MIN}$	-	-	-	0	%
<b>TOTAL STANDBY CURRENT</b>						
Start-Up Current	$I_{ST}$	-	-	0.2	0.4	mA
Operating Supply Current	$I_{CC}$	$V_{PIN2} = V_{PIN3} = 0V$	-	11	17	mA
$V_{CC}$ Zener Voltage	$V_Z$	$I_{CC} = 25mA$	-	29	-	V

\* Adjust  $V_{CC}$  above the start threshold before setting at 15V

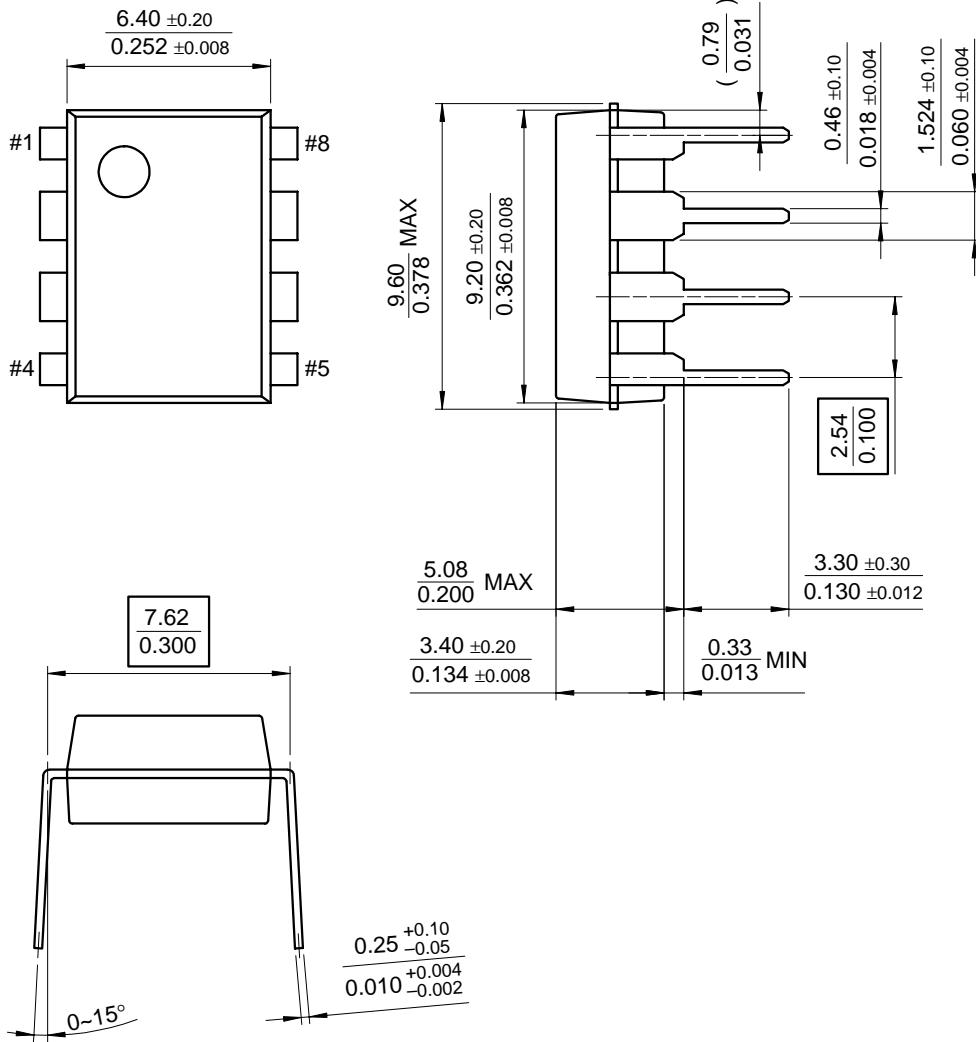
### Notes :

- These parameters, although guaranteed, are not 100% tested in production.
- Parameter measured at trip point of latch with  $V_2 = 0V$ .
- Gain defined as:  $G_V = \Delta V_{PIN1} / \Delta V_{PIN3}$  ( $V_{PIN3} = 0$  to  $0.8V$ )
- Junction-to-air thermal resistance test environments.
  - PCB information ;  
Board thickness : 1.6mm , Board dimension : 76.2 X 114.3mm<sup>2</sup> , Ref. : EIA / JSED51-3 and EIA / JSED51-7
  - Board structure; Using the single layer PCB.

# Mechanical Dimensions

## Package

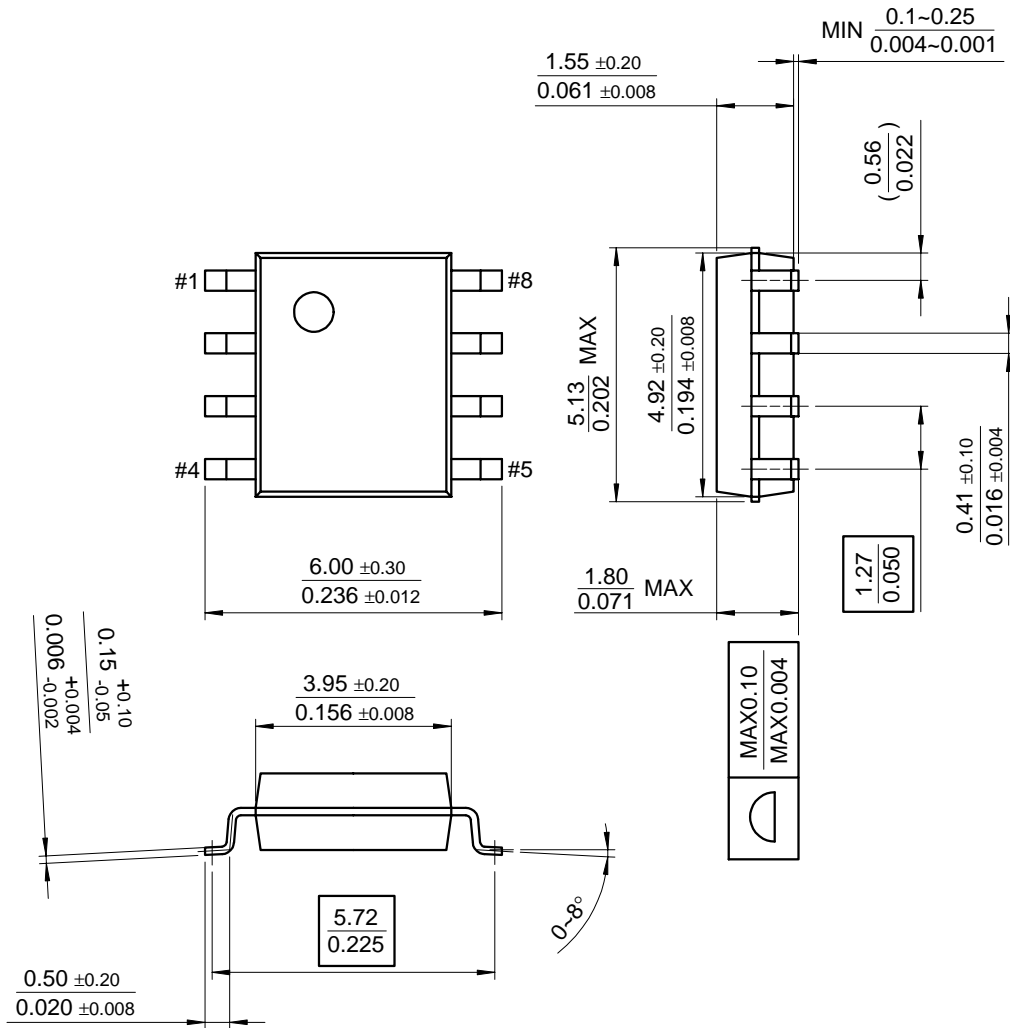
### 8-DIP



Mechanical Dimensions (Continued)

Package

8-SOP



**Ordering Information**

<b>Product Number</b>	<b>Package</b>	<b>Operating Temperature</b>
KA3882C	8 DIP	0 ~ + 70°C
KA3882CD	8 SOP	
KA3883C	8 DIP	
KA3883CD	8 SOP	



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