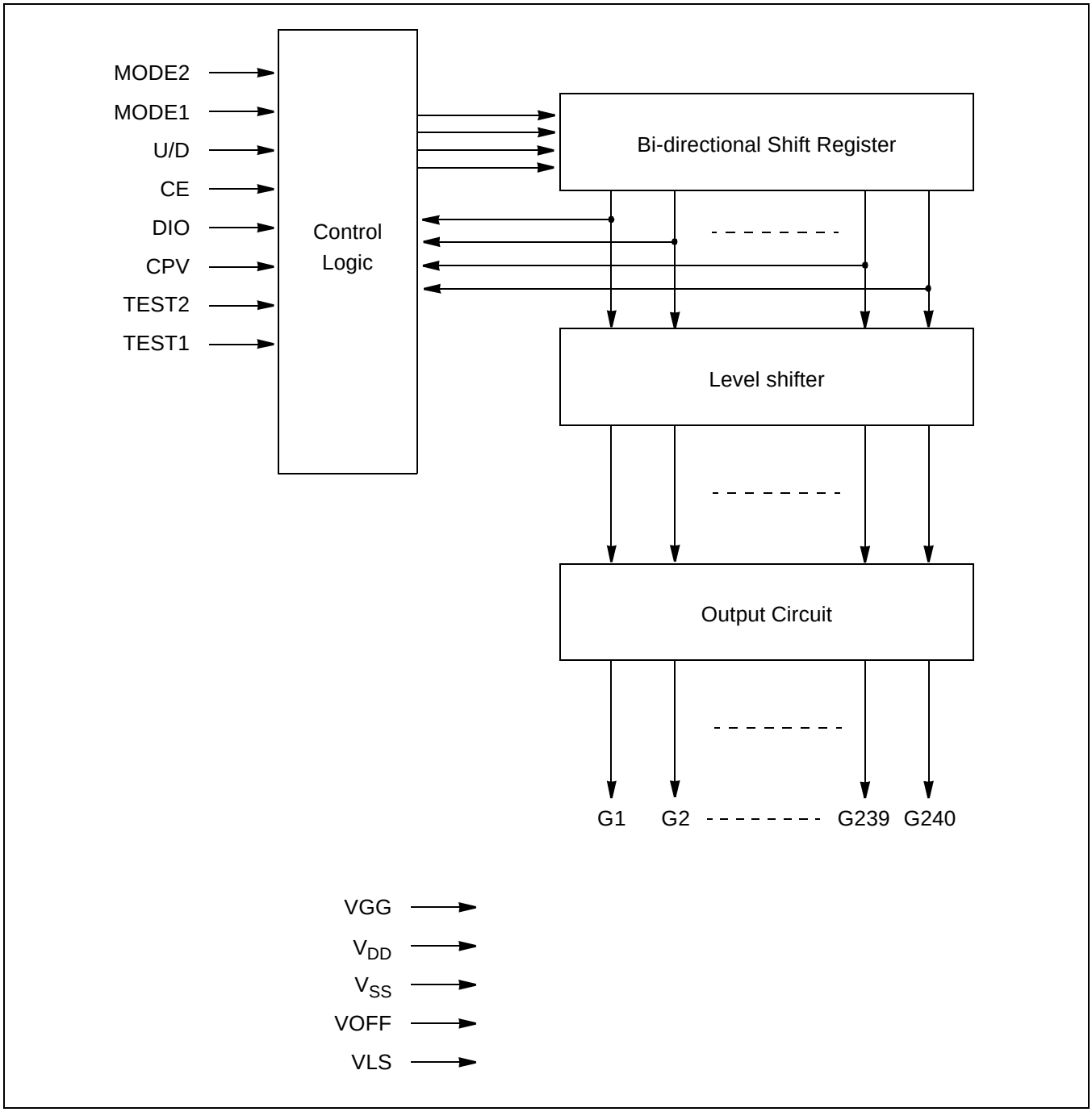
INTRODUCTION

The KS0607 is a gate driver for TFT LCD panel used for AV set such as TV, CNS etc.
This product has 240 LCD driver outputs.

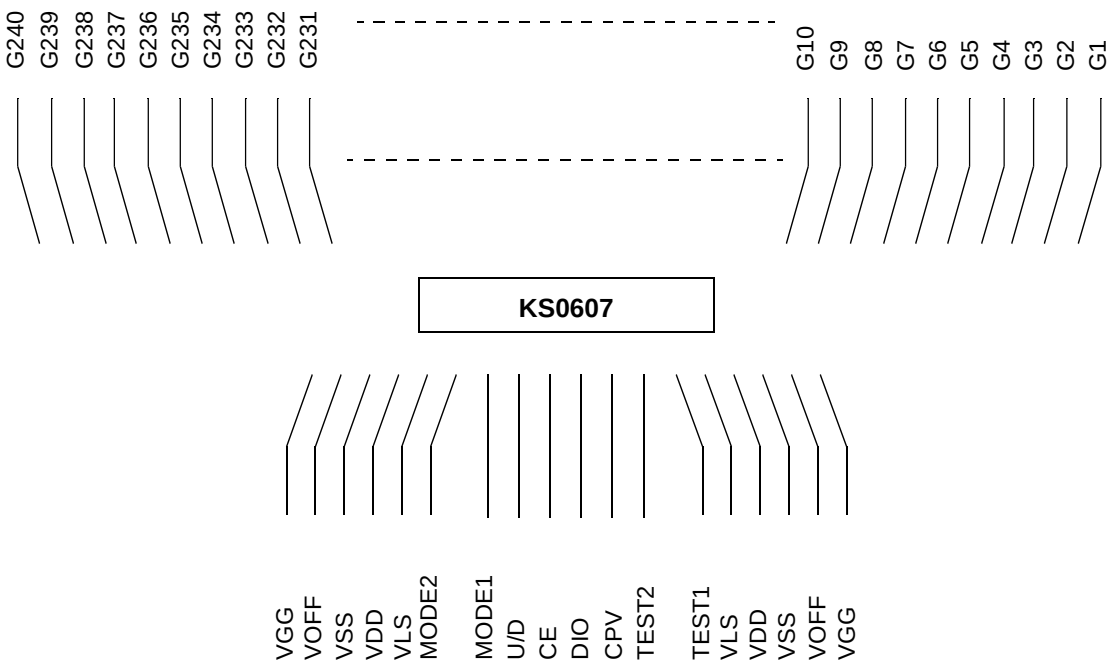
FEATURES

- ❑ TFT LCD gate driver
- ❑ LCD drive output sequence: output shift direction can be selected. (G1 → G240 or G240 → G1)
- ❑ Output mode switching:
  - — Normal mode (1-pulse scanning)
  - — Continuous 2-pulse mode (2-pulse scanning)
  - — Jumping 2-pulse mode.
- ❑ LCD drive voltage: 16.0 to 35.0 V
- ❑ Number of LCD drive outputs: 240 outputs
- ❑ Package: TCP/COG

BLOCK DIAGRAM

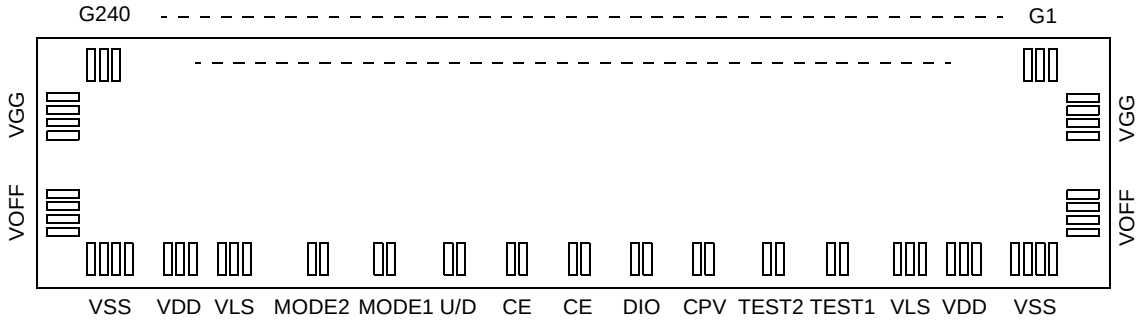


PIN CONFIGURATION



NOTE: This figure does not specify the dimensions of the TCP package

Figure 1. KS0607 TCP Assignment Diagram



NOTE: This PAD location is applied for the COG(chip on glass).

Figure 2. KS0607 Pad Assignment Diagram

PIN DESCRIPTIONS

<table>
<tr><th>Symbol</th><th>Pin Name</th><th>Description</th></tr>
<tr><td>V_{DD}</td><td>Power supply for logic system</td><td>Used as power supply pin for logic system, which is normally connected to V_{SS} + 5.0 V.</td></tr>
<tr><td>V_{SS}</td><td>Power supply for logic system</td><td>Used as logic ground pin.</td></tr>
<tr><td>VGG</td><td>Power supply for LCD drive</td><td>Used as power supply pin for low level LCD drive.</td></tr>
<tr><td>VOFF</td><td>Power supply for LCD drive</td><td>Used as power supply pin for low level LCD drive.</td></tr>
<tr><td>VLS</td><td>Power supply for input level shifter</td><td>Used as power supply for input level shifters.</td></tr>
<tr><td>G1 to G240</td><td>LCD drive output</td><td>Used as output pins for LCD drive output, which outputs data at levels. Selecting data is output at VGG level.
Non-selecting data is output at VOFF level.</td></tr>
<tr><td>DIO</td><td>Vertical scanning start pulse input</td><td>Used as vertical scanning start pulse input pin.</td></tr>
<tr><td>CPV</td><td>Vertical shift clock input</td><td>Used as vertical shift clock pulse input pin.</td></tr>
<tr><td>U/D</td><td>Shift direction selecting input</td><td>Used as input pin for selecting the shifting direction of bidirectional shift register and setting the sequence of cascade sequence.
Up mode(U/D = “H”): G1 → G20
Down mode(U/D = “L”):G240 → G1</td></tr>
<tr><td>CE</td><td>Cascade sequence setting input</td><td>Used as input pin for setting of chip cascade sequence.
Referring to below table, set the cascaded sequence signal inside the LSI.
<table>
<tr><th rowspan="2">CE</th><th colspan="2">Cascade Sequence</th></tr>
<tr><th>U/D=H</th><th>U/D=L</th></tr>
<tr><td>H</td><td>1st</td><td>2nd</td></tr>
<tr><td>L</td><td>2nd</td><td>1st</td></tr>
</table></td></tr>
<tr><td>MODE1
MODE2</td><td>Output mode selecting input</td><td>Used as input pins for selecting output mode.
Output mode is set as shown in table below by setting MODE1 and MODE2 pin.
<table>
<tr><th>Mode1</th><th>Mode2</th><th>Output Mode</th></tr>
<tr><td>H</td><td>H</td><td>Normal mode</td></tr>
<tr><td>L</td><td>H</td><td>Continuous 2-pulse mode</td></tr>
<tr><td>H</td><td>L</td><td>Jumping 2-pulse mode</td></tr>
<tr><td>L</td><td>L</td><td>Set all outputs to VOFF level</td></tr>
</table></td></tr>
<tr><td>TEST1
TEST2</td><td>LSI test input</td><td>Used as input pins for LSI testing must be set to “H”.</td></tr>
</table>

FUNCTIONAL DESCRIPTION

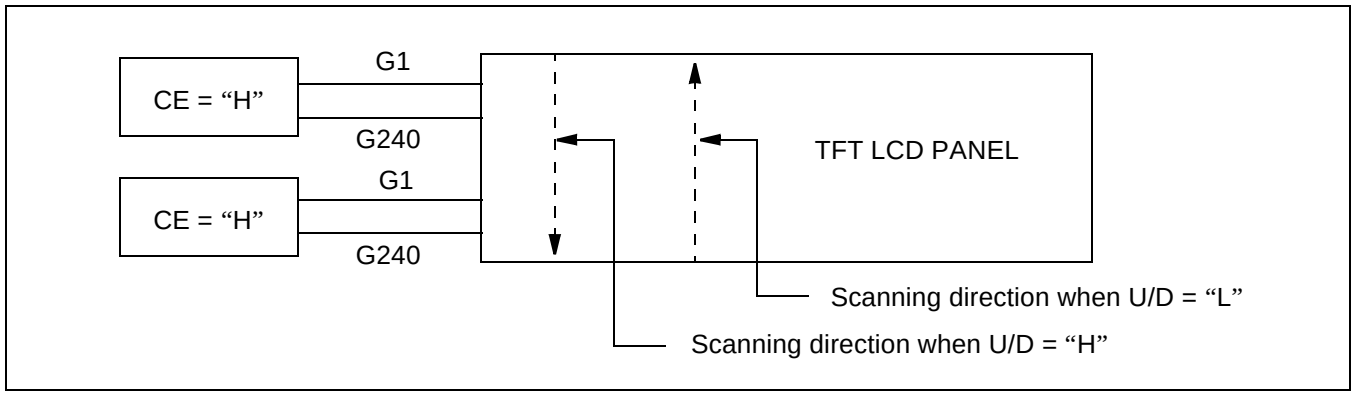


Figure 3. Examples of Cascade Sequence

At this time

- Normal mode (1-pulse scanning) is set when MODE1 = “H”, MODE2 = “H”.
- Jumping 2-pulse mode (2-pulse scanning) is set when MODE1 = “H”, MODE2 = “L”.
- Continued 2-pulse mode (2-pulse scanning) is set when MODE1 = “L”, MODE2 = “H”.
- Output VOFF is set when MODE1 = “L”, MODE2 = “L”.

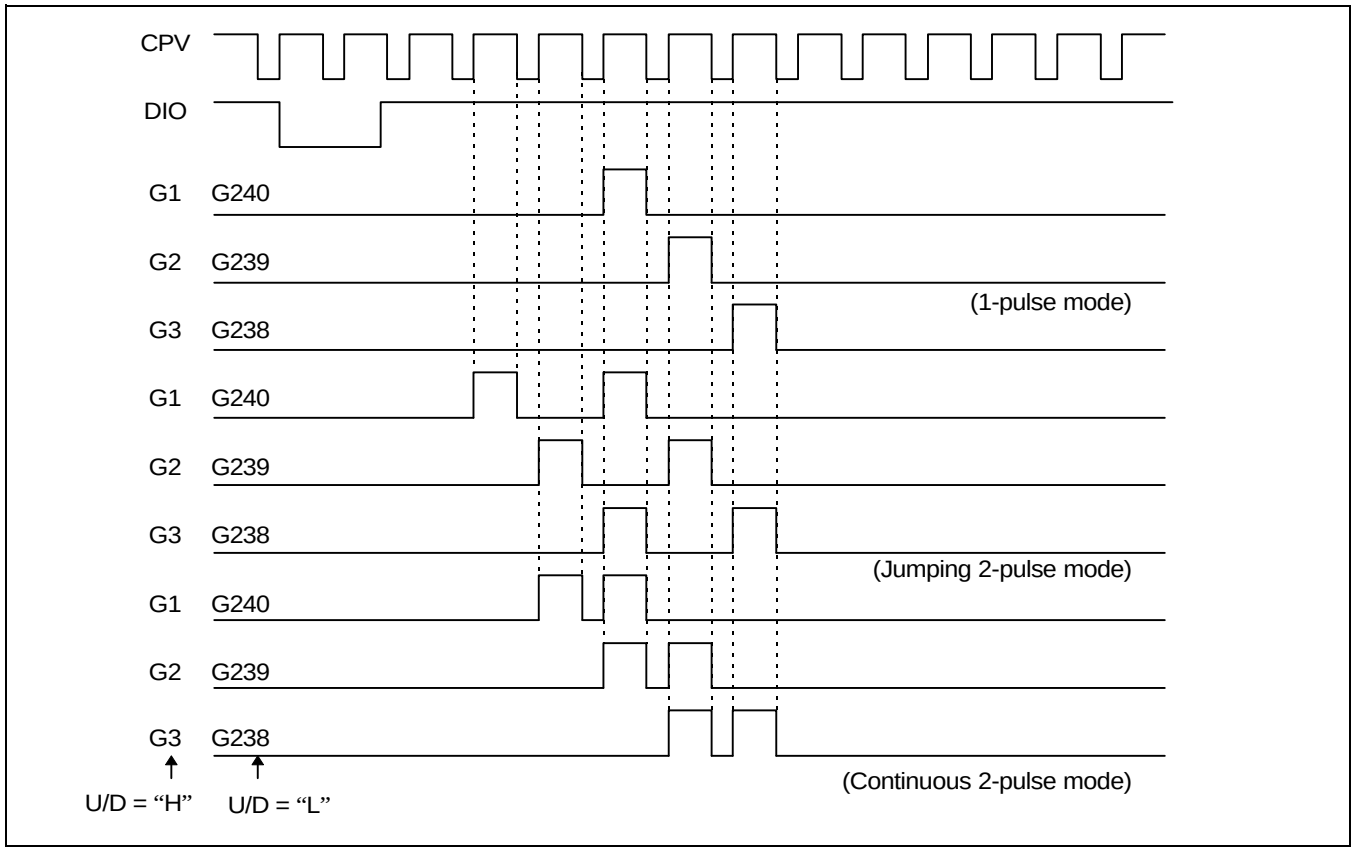


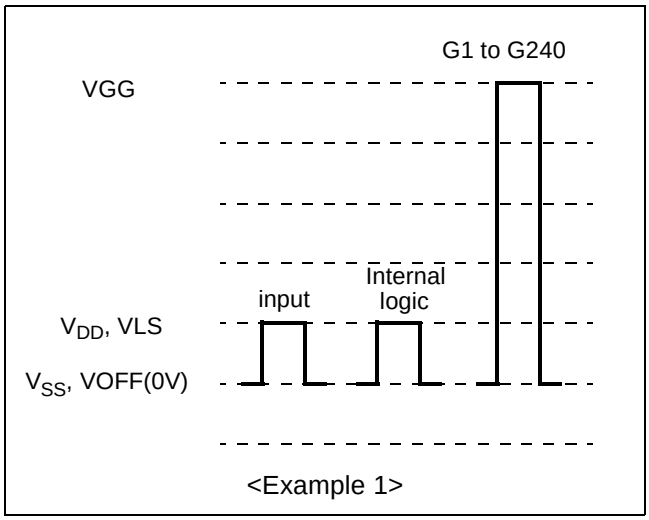
Figure 4. Example of Input/Output Timing (For Cascade Sequence 1st)

VOLTAGE BIAS

When power supply pins are set as shown below, the KS0607can output positive voltage and negative voltage to LCD drive output.

Example 1:

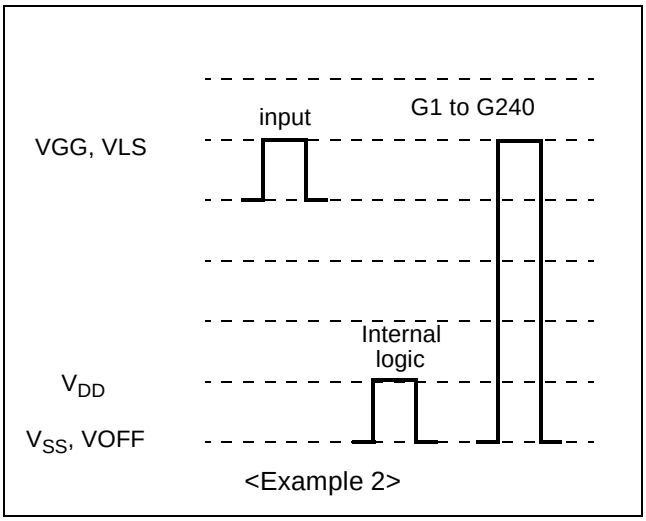
- For positive voltage output
- Input voltage(logic): 3.3 V
- Supply voltage:
  - VGG = 3.3 V
  - VDD = 3.3 V
  - VLS = 3.3 V
  - VOFF = V_{SS} = 0 V
- LCD drive output:
  - High level = VGG (3.3 V)
  - Low level = VOFF (0 V)



<Example 1>

Example 2:

- For positive voltage output
- Input voltage (logic): 5.5 V
- Supply voltage:
  - VGG = 5.5 V
  - VLS = 5.5 V
  - V_{DD} = – 22 V
  - VOFF = VSS = –27.5 V
- LCD drive output:
  - High level = VGG (5.5 V)
  - Low level = VOFF (– 27.5 V)



<Example 2>

PRECAUTIONS

Turning on and shutting off power supply

This LSI has a high-voltage LC driver, so it may be permanently damage by a large current which may flow if a voltage is supplied to the LC drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, connect the LC drive power after connecting the logic system power.

When shutting off the power, shut off LC drive power and then shut off the logic system power, or simultaneously shut off the power.
Because the logic state of internal logic is unstable immediately after the system power is supplied, input CPV and DIO to send a clock during cascade sequence setting period and initialize the internal logic.

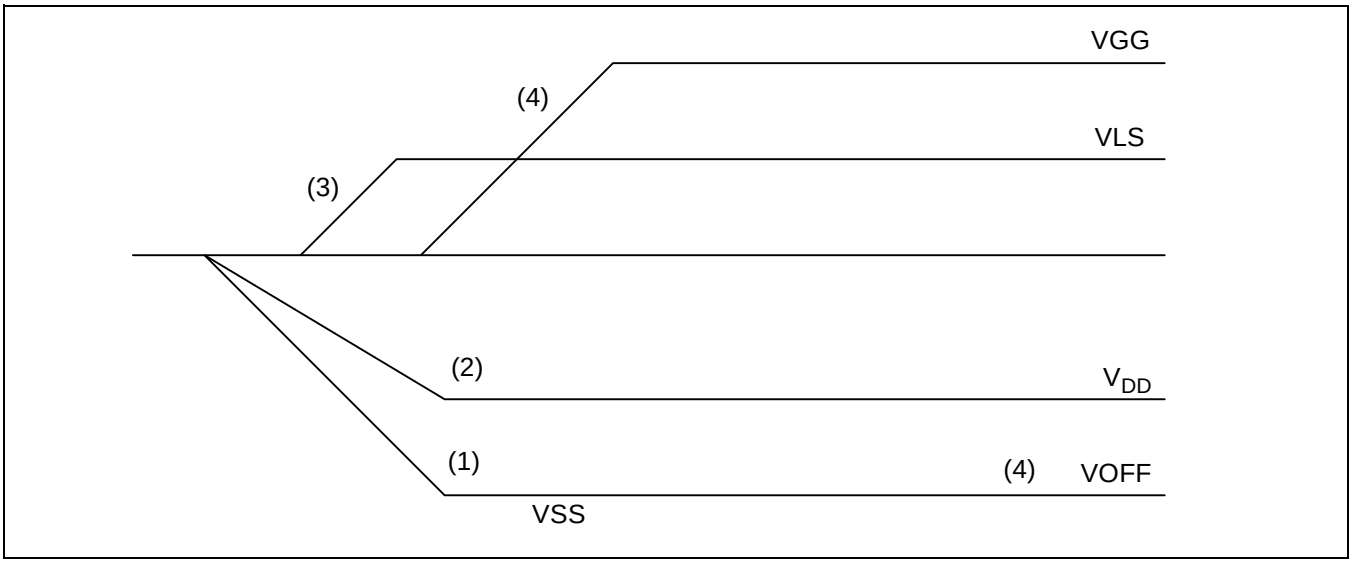


Figure 5. Turning on and shutting off power supply

Input pin setting

Input pins other than CPV and DIO must be set to “H” level or “L” level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rated value	Unit
Supply voltage	VGG	Ta = 25 °C	– 0.3 to 37.0	V
	V_{DD} – V_{SS}	Ta = 25 °C	– 0.3 to 7.0	V
	VLS	Ta = 25 °C	– 0.3 to 7.0	V
	VOFF – V_{SS}	Ta = 25 °C	– 0.3 to 37.0	V
	VGG – VOFF (V_{SS})	Ta = 25 °C	– 0.3 to 37.0	V
Input voltage	VIN	Ta = 25 °C	– 0.3 to VLS+0.3	V
Operating temperature	T_{OPR}	–	– 20 to 75	°C
Storage temperature	T_{STG}	–	– 45 to 125	

NOTE: Standard voltage is GND (0 V).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Rated value	Unit
Supply voltage	VGG	–	5.0 to 35.0	V
	V_{DD} - V_{SS}	–	3.0 to 5.5	V
	VLS	–	3.0 to 5.5	V
	VOFF-V_{SS}	–	0 to 11.0	V
	VGG-VOFF (V_{SS})	–	16 to 35.0	V
Input voltage	VIN	–	0 to VLS	V

NOTES:

1. Standard voltage is GND (0 V)
2. V_{SS}, VOFF ≤ 0 V, V_{DD} ≤ VLS ≤ VGG
3. V_{DD} - V_{SS} = VLS ± 0.1 V

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Ta = – 20 to + 75 °C, VGG – V_{SS} = 16 to 35V, VLS = 3.0 to 5.5V (= V_{DD} – V_{SS}), VOFF – VSSS = 0 to 11V, VGG ≥ VLS ≥ VOFF

Parameter	Symbol	Condition	Min.	Max.	Unit.	Application
Low input voltage	VIL	–	–	0.2 VLS	V	CPV, DIO, CE, MODE1, MODE2, U/D
High input voltage	VIH	–	0.8 VLS	–		
Low input current	IIL	VIN = 0 V	–	5.0	µA	
High input current	IIH	VIN = VLS (= 5 V)	–	5.0		
Low output resisatnce	ROL	VOUT = VOFF + 0.4 V VGG – VOFF = 33 V	–	1	kΩ	G1 to G240
High output resisatnce	RO	VOUT = VG – 0.4 V VGG – VOFF = 33 V	–	1		
Current consumption 1 (Note)	IGG	1-pulse mode (MODE1, MODE2) = VLS	–	50	µA	–
	ILS		–	150		
	IDD		–	80		
	IOFF		–	40		
Current consumption 2 (Note)	IGG	2-pulse mode continuous mode (MODE1 = 0V) Jumping mode (MODE2 = 0V)	–	100	µA	–
	ILS		–	300		
	IDD		–	100		
	IOFF		–	40		

NOTE: fCPV = 31 kHz, “L” period width tCPVL = 16.2 µs, fDIO = 60 Hz, Other input pins = VLS, All output pins are open. TEST1, TEST2 = VLS

AC CHARACTERISTICS

Ta = – 20 to + 75 °C, VGG – V_{SS} = 16 to 35V, VLS = 3.0 to 5.5V (= V_{DD} – V_{SS}), VOFF – VSSS = 0 to 11V, VGG ≥ VLS ≥ VOFF

Parameter	Symbol	Condition	Min	Max	Unit	Application
Clock frequency	fCPV	–	–	100	kHz	CPV
Minimum “L” clock pulse width	tCPVL	–	500	–	ns	
Clock rise time	trCPV	VIN = 0 V	–	100	ns	
Clock fall time	trCPV	VIN = VLS (= 5 V)	–	100		
Data setup time	tsDI	–	100	–	ns	CPV, DIO
Data hold time	thDI	–	300	–		
Pulse rise time	trDIO	–	–	100	ns	DIO
Pulse fall time	trDIO	–	–	100		
Output transfer delay time	td	CL = 500 pF	–	3.0	µs	G1 to G240
Output rise time	tr		–	1.0		
Output fall time	tf		–	1.0		

TIMING DIAGRAM