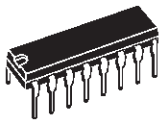
L5993

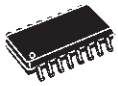
CONSTANT POWER CONTROLLER

- CURRENT-MODE CONTROL PWM
- SWITCHING FREQUENCY UP TO 1MHz
- LOW START-UP CURRENT (< 120µA)
- CONSTANT OUTPUT POWER VS. SWITCHING FREQUENCY
- HIGH-CURRENT OUTPUT DRIVE SUITABLE FOR POWER MOSFET (1A)
- FULLY LATCHED PWM LOGIC WITH DOUBLE PULSE SUPPRESSION
- PROGRAMMABLE DUTY CYCLE
- 100% AND 50% MAXIMUM DUTY CYCLE LIMIT
- PROGRAMMABLE SOFT START
- PRIMARY OVERCURRENT FAULT DETECTION WITH RE-START DELAY
- PWM UVLO WITH HYSTERESIS
- IN/OUT SYNCHRONIZATION
- LATCHED DISABLE
- INTERNAL 100ns LEADING EDGE BLANKING OF CURRENT SENSE
- PACKAGE: DIP16 AND SO16N

MULTIPOWER BCD TECHNOLOGY



DIP16



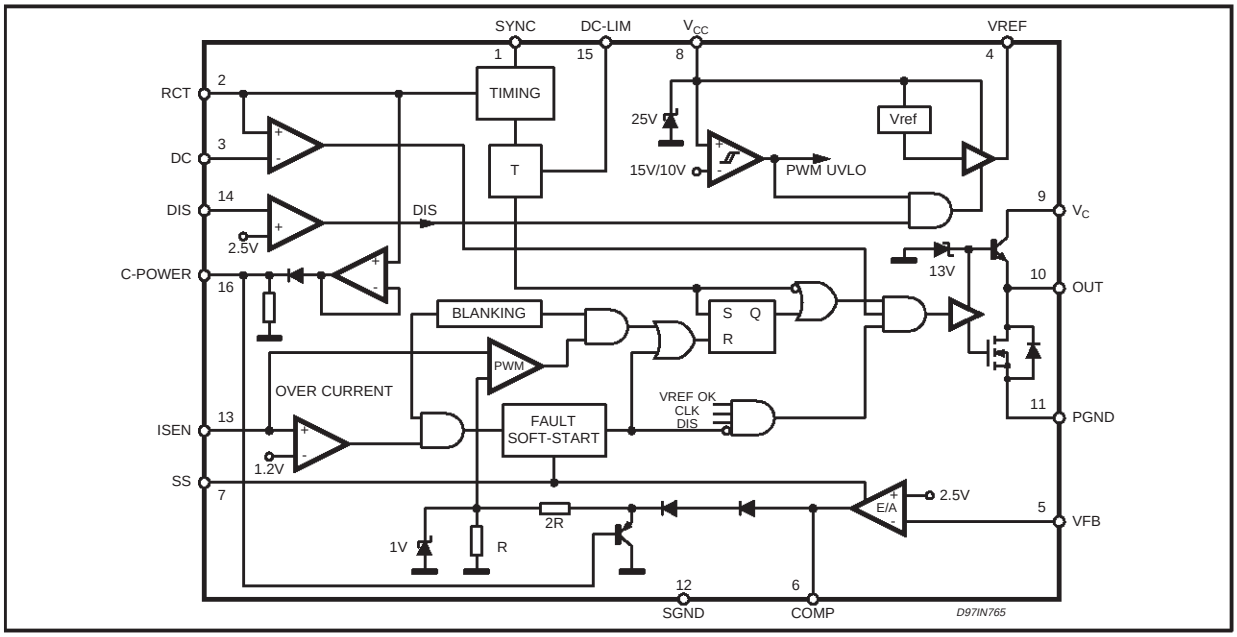
SO16N

ORDERING NUMBERS: L5993 (DIP16)
L5993D (SO16)

DESCRIPTION

This primary controller I.C., developed in BCD60II technology, has been designed to implement off line or DC-DC power supply applications using a fixed frequency current mode control.
Based on a standard current mode PWM controller this device includes some features such as programmable soft start, IN/OUT synchronization, disable (to be used for over voltage protection and for power management), precise maximum Duty Cycle Control, 100ns leading edge blanking on current sense, pulse by pulse current limit, overcurrent protection with soft start intervention and "constant power" function for cotrolling throughput power in multisync monitor SMPS.

BLOCK DIAGRAM

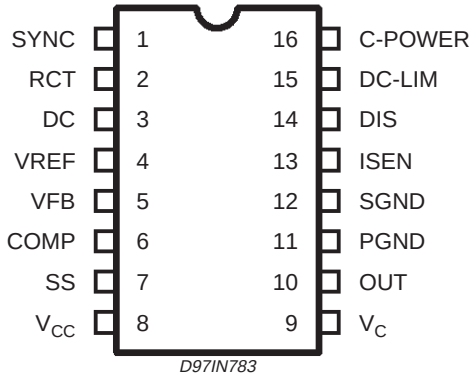


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (I_{CC} < 50mA) (*)	selflimit	V
I_{OUT}	Output Peak Pulse Current	1.5	A
	Analog Inputs & Outputs (6,7)	-0.3 to 8	V
	Analog Inputs & Outputs (1,2,3,4,5,15,14, 13, 16)	-0.3 to 6	V
P_{tot}	Power Dissipation @ T_{amb} = 70°C (DIP16) @ T_{amb} = 50°C (SO16)	1 0.83	W W
T_j	Junction Temperature, Operating Range	-40 to 150	°C
T_{stg}	Storage Temperature, Operating Range	-55 to 150	°C

(*) maximum package power dissipation limits must be observed

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction -Ambient **(DIP16)** Thermal Resistance Junction -Ambient **(SO16)**	80 120	°C/W °C/W

PIN FUNCTIONS

N.	Name	Function
1	SYNC	Synchronization. A synchronization pulse terminates the PWM cycle and discharges Ct
2	RCT	Oscillator pin for external C_t, R_t components
3	DC	Duty Cycle control
4	VREF	5.0V +/-1.5% reference voltage at 25°C
5	VFB	Error Amplifier Inverting input
6	COMP	Error Amplifier Output
7	SS	Soft start pin for external capacitor Css
8	V_{CC}	Supply for internal "Signal" circuitry
9	V_C	Supply for Power section
10	OUT	High current totem pole output
11	PGND	Power ground
12	SGND	Signal ground
13	ISEN	Current sense
14	DIS	Disable. It must never be left floating. Tie to SGND if not used.
15	DC-LIM	Connecting this pin to Vref, DC is limited to 50%. If it is left floating or grounded no limitation is imposed
16	C-POWER	Constant Power vs. Switching Frequency. Connect a capacitor to SGND. The pin must be connected to VREF if not used.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15V; T_j = 0 to 105°C; R_T = 13.3kΩ; C_T = 1nF unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
REFERENCE SECTION						
V_{Ref}	Output Voltage	T_j = 25°C; I_O = 1mA	4.925	5.0	5.075	V
	Line Regulation	V_{CC} = 12 to 20V; T_j = 25°C		2.0	10	mV
	Load Regulation	I_O = 1 to 10mA; T_j = 25°C		2.0	10	mV
T_S	Temperature Stability			0.4		mV/°C
	Total Variation	Line, Load, Temperature	4.80	5.0	5.130	V
I_{OS}	Short Circuit Current	Vref = 0V	30		150	mA
	Power Down/UVLO	V_{CC} = 8.5V; I_{sink} = 0.5mA		0.2	0.5	V
OSCILLATOR SECTION						
	Initial Accuracy	pin 15 = Vref T_j = 25°C V_{CC} = 12 to 20V	95 93	100 100	105 107	kHz kHz
	Duty Cycle	pin 3 = 0,7V, pin 15 = Vref pin 3 = 0.7V, pin 15 = OPEN			0 0	% %
	Duty Cycle	pin 3 = 3.2V, pin 15 = Vref pin 3 = 3.2V, pin 15 = OPEN	47 93			% %
	Duty Cycle Accuracy	pin 3 = 2.79V, pin 15 = OPEN	75	80	85	%
	Oscillator Ramp Peak		2.8	3.0	3.2	V
	Oscillator Ramp Valley		0.75	0.9	1.05	V
ERROR AMPLIFIER SECTION						
	Input Bias Current	V_{FB} to GND		0.2	3.0	µA
V_I	Input Voltage	V_{COMP} = V_{FB}	2.42	2.5	2.58	V
G_{OPL}	Open Loop Gain	V_{COMP} = 2 to 4V	60	90		dB
SVR	Supply Voltage Rejection	V_{CC} = 12 to 20V		85		dB
V_{OL}	Output Low Voltage	I_{sink} = 2mA, V_{FB} = 2.7V			1.1	V
V_{OH}	Output High Voltage	I_{source} = 0.5mA, V_{FB} = 2.3V	5	6		V
I_O	Output Source Current	V_{COMP} > 4V, V_{FB} = 2.3V	0.5	1.3	2.5	mA
	Output Sink Current	V_{COMP} > 1.1V, V_{FB} = 2.7V	2	6		mA
	Unit Gain Bandwidth		1.7	4		MHz
S_R	Slew Rate			8		V/µs
PWM CURRENT SENSE SECTION						
I_b	Input Bias Current	I_{sen} = 0		3	15	µA
I_S	Maximum Input Signal	V_{COMP} = 5V	0.92	1.0	1.08	V
	Delay to Output			70	100	ns
	Gain		2.85	3	3.15	V/V
SOFT START						
I_{SSC}	SS Charge Current		14	20	26	µA
I_{SSD}	SS Discharge Current	VSS = 0.6V, T_j = 25°C	5	10	15	µA
V_{SSSAT}	SS Saturation Voltage	DC = 0%			0.6	V
$V_{SSCLAMP}$	SS Clamp Voltage			7		V
LEADING EDGE BLANKING						
	Internal Masking Time			100		ns
OUTPUT SECTION						
V_{OL}	Output Low Voltage	I_O = 250mA			1.0	V
V_{OH}	Output High Voltage	I_O = 20mA; V_{CC} = 12V	10	10.5		V
		I_O = 200mA; V_{CC} = 12V	9	10		V
$V_{OUT\ CLAMP}$	Output Clamp Voltage	I_O = 5mA; V_{CC} = 20V		13		V

ELECTRICAL CHARACTERISTICS (continued.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OUTPUT SECTION						
	Collector Leakage	V_{CC} = 20V V_C = 24V		2	20	µA
	Fall Time	C_O = 1nF C_O = 2.5nF		20 35	60	ns ns
	Rise Time	C_O = 1nF C_O = 2.5nF		50 70	100	ns ns
	UVLO Saturation	V_{CC} = 0V to V_{CCON}; I_{sink} = 10mA			1.0	V
SUPPLY SECTION						
V_{CCON}	Startup voltage		14	15	16	V
V_{CCOFF}	Minimum Operating Voltage		9	10	11	V
V_{hys}	ULVO Hysteresis		4.5	5		V
I_S	Start Up Current	Before Turn-on at: V_{CC} = V_{CCON} - 0.5V	40	75	120	µA
I_{op}	Operating Current	CT = 1nF,R_T = 13.3kΩ, C_O =1nF		9	13	mA
I_q	Quiescent Current	(After turn on), CT = 1nF, R_T = 13.3kΩ, C_O = 0nF		7.0	10	mA
V_Z	Zener Voltage	I_8 = 20mA	21	25	30	V
SYNCHRONIZATION SECTION						
		Master Operation				
V_1	Clock Amplitude	I_{SOURCE} = 0.8mA	4			V
I_1	Clock Source Current	Vclock = 3.5V	3	7		mA
		Slave Operation				
V_1	Sync Pulse	Low Level			1	V
		High Level	3.5			V
I_1	Sync Pulse Current	VSYNC = 3.5V	0.5			mA
OVER CURRENT PROTECTION						
V_t	Fault Threshold Voltage		1.1	1.2	1.3	V
DISABLE SECTION						
	Shutdown threshold		2.4	2.5	2.6	V
I_{SH}	Shutdown Current	V_{CC} = 15V		330		µA
CONSTANT POWER						

Figure 1. Quiescent current vs. input voltage.

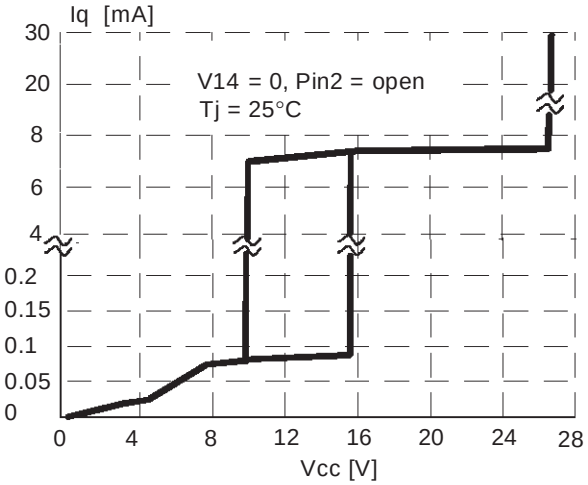


Figure 2. Quiescent current vs. input voltage (after disable).

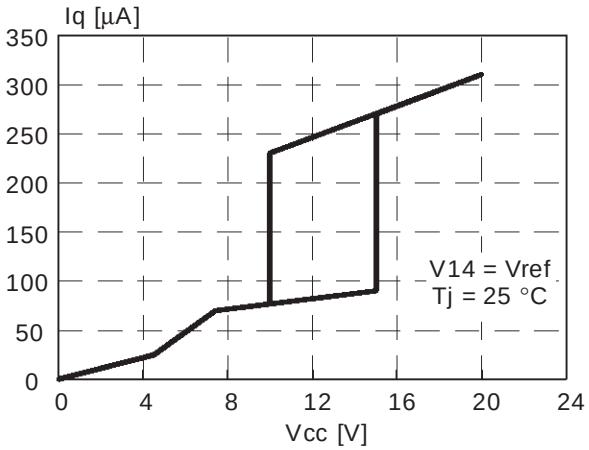


Figure 3. Quiescent current vs. input voltage.

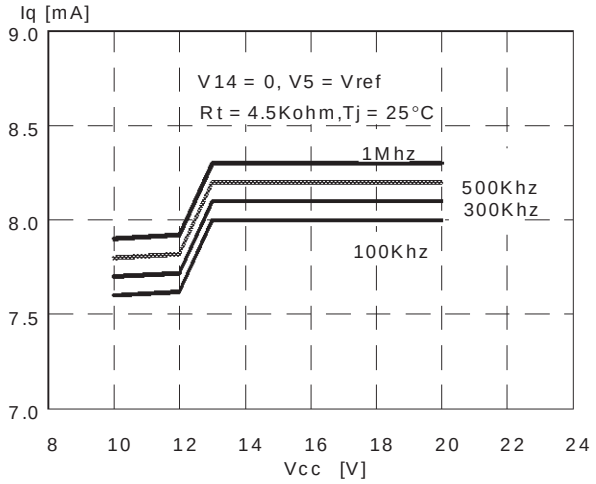


Figure 4. Quiescent current vs. input voltage and switching frequency.

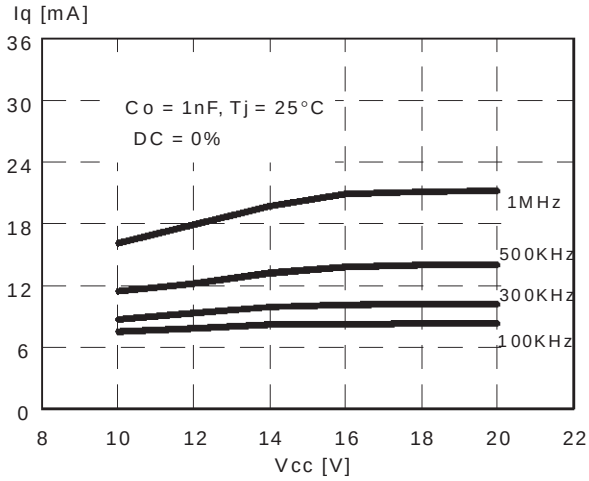


Figure 5. Quiescent current vs. input voltage and switching frequency.

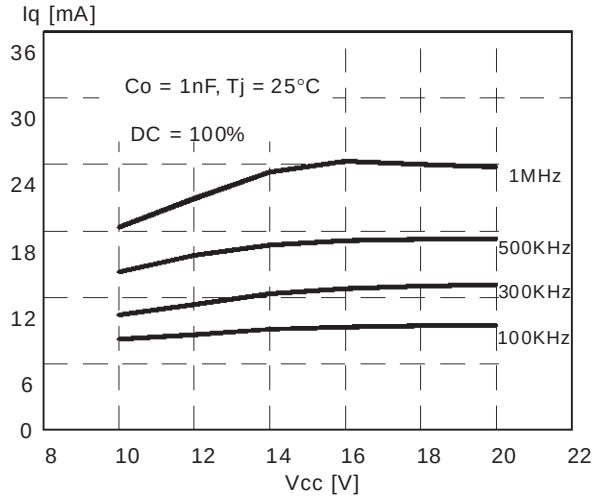


Figure 6. Reference voltage vs. load current.

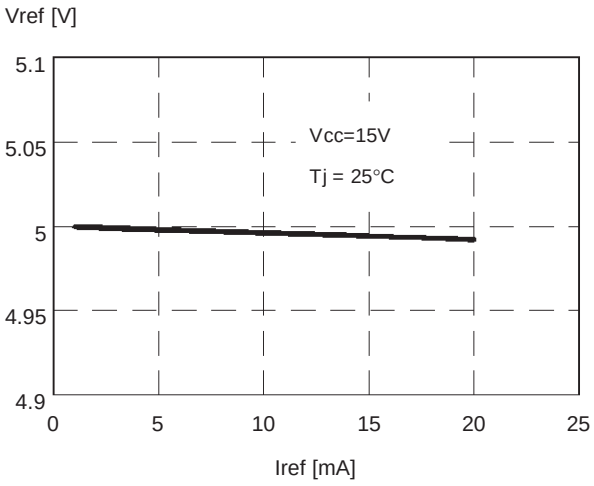


Figure 7. Vref vs. junction temperature.

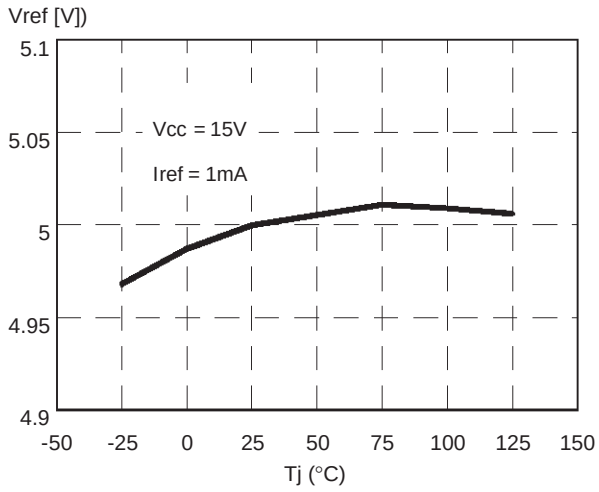


Figure 8. Vref vs. junction temperature.

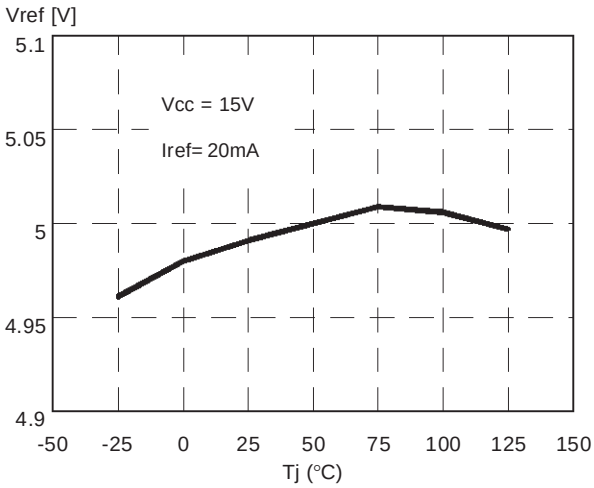


Figure 9. Vref SVRR vs. switching frequency.

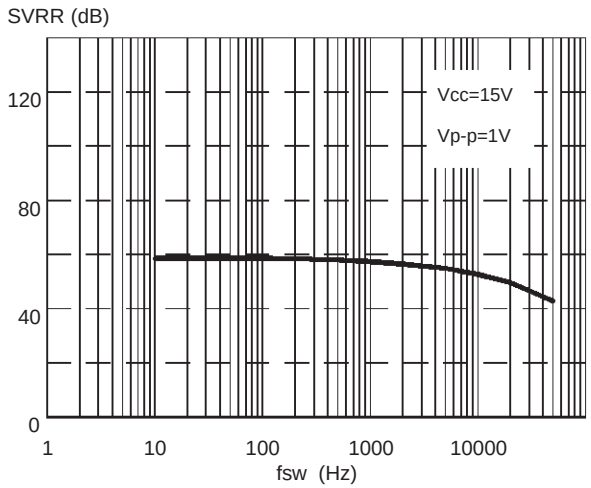


Figure 10. Output saturation.

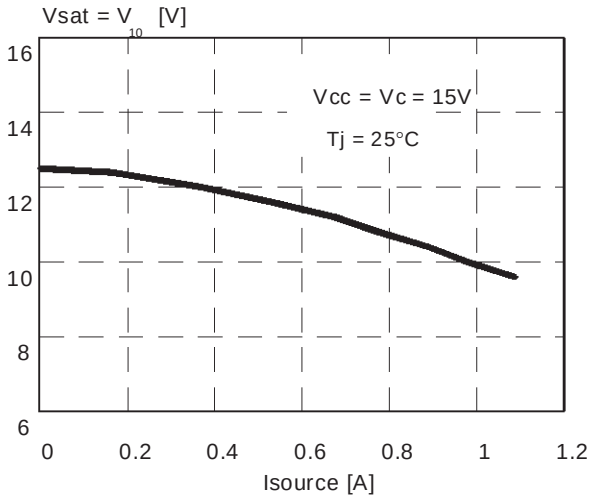


Figure 11. Output saturation.

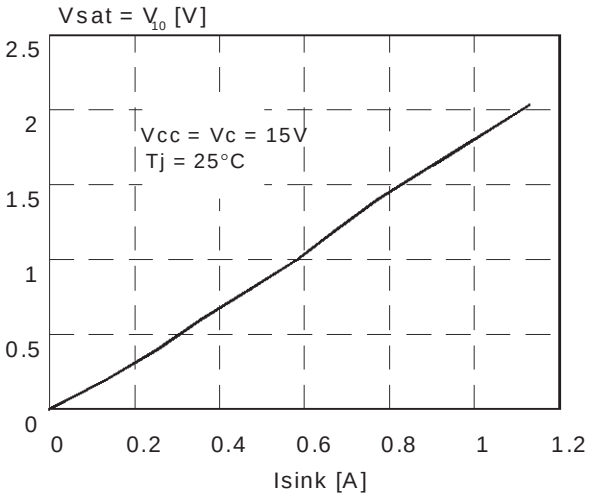


Figure 12. UVLO Saturation

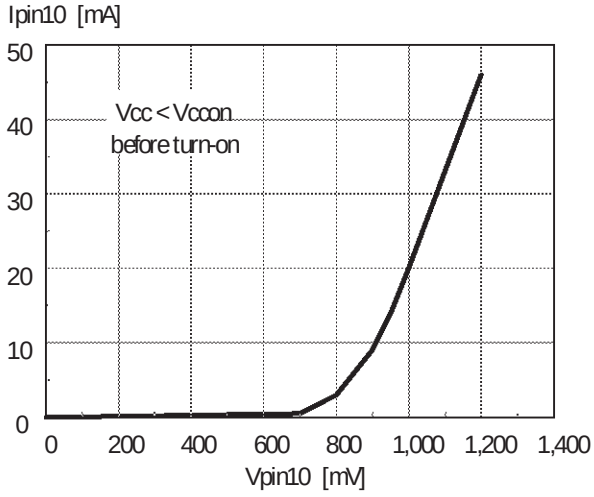


Figure 13. Timing resistor vs. switching frequency.

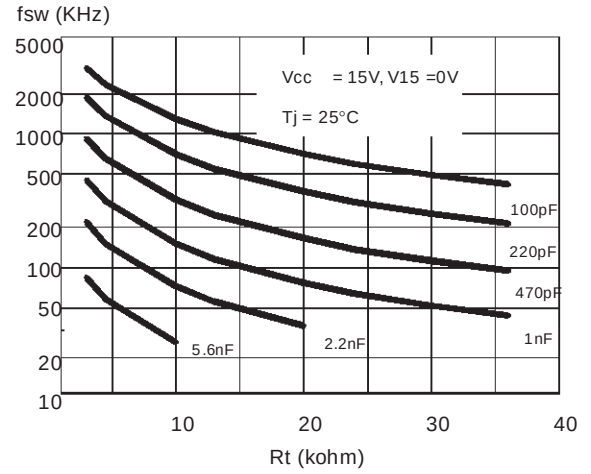


Figure 14. Switching frequency vs. temperature

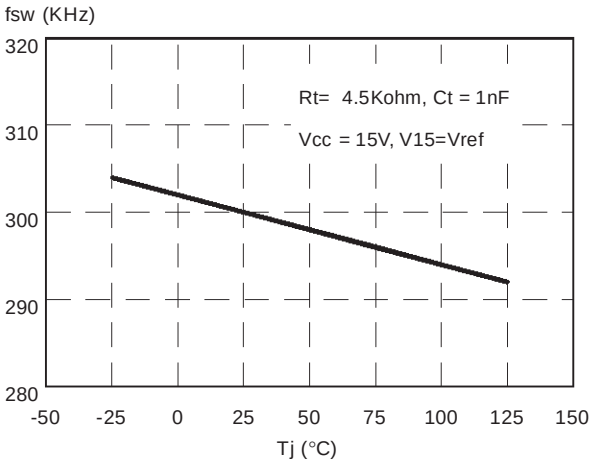


Figure 15. Switching frequency vs. temperature.

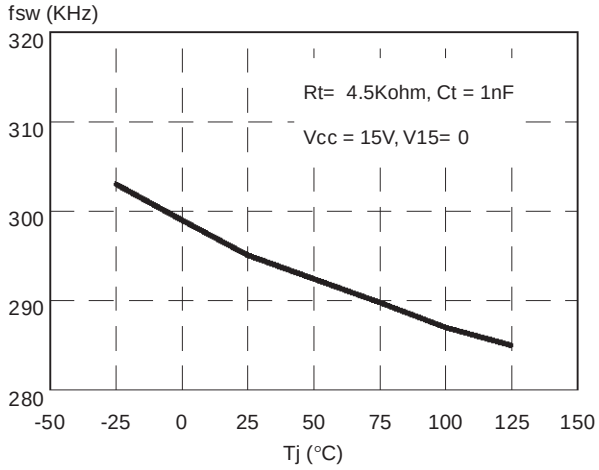


Figure 16. Dead time vs Ct.

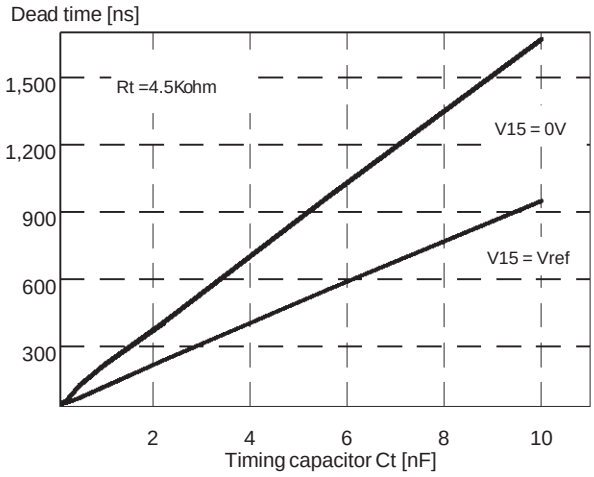


Figure 17. Maximum Duty Cycle vs Vpin3.

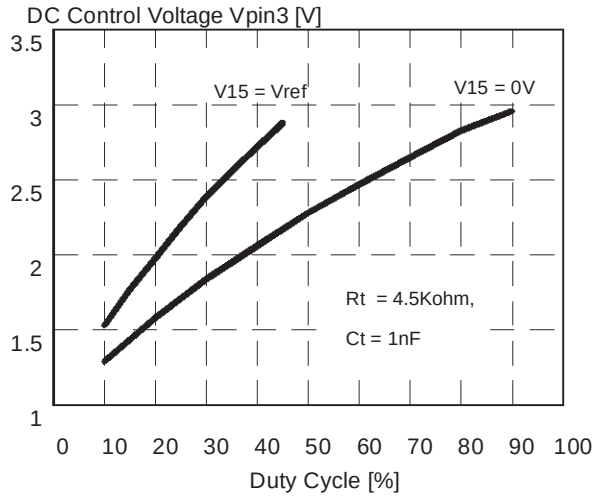


Figure 18. Delay to output vs junction temperature.

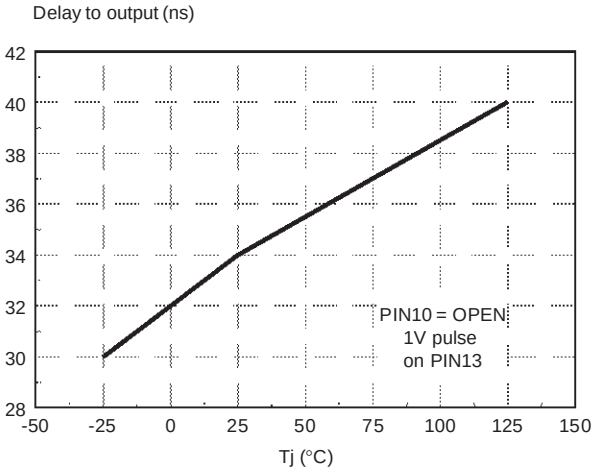
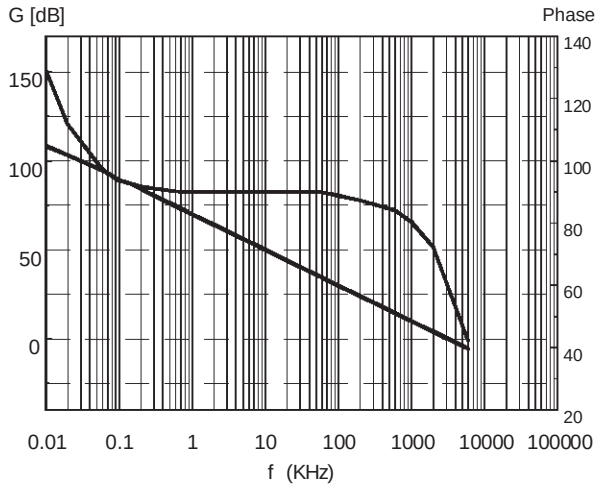


Figure 19. E/A frequency response.



CONSTANT POWER FUNCTION

Pulse-by-pulse current limitation prevents peak primary current from exceeding a given level. This, in turn, limits the maximum power deliverable to the output or, in other words, the power capability of a converter. The capability, however, depends on switching frequency: for example, in a discontinuous current mode flyback they are just proportional.

In SMPS' of raster-scanned CRT displays the switching frequency is usually synchronized to the raster line scan signal of the display in order to increase noise immunity. More and more often, CRT displays are required to operate within a range of different video frequencies (e.g. from 31 kHz to 64 kHz), thus also the switching frequency of the SMPS will vary in that range.

In case of some failure, the power throughput may be excessive without necessarily tripping the pulse-by-pulse current limitation circuit because of a high operating frequency.

For the sake of safety, it would be then desirable to design the power stage of a converter (power MOSFET, transformer, catch diode) so as to be able to withstand the maximum power throughput under failure conditions. However, this is a considerable increase of size and cost.

The "Constant Power" function of the L5993 allows to overcome this problem. The device changes the threshold of its pulse-by-pulse current limitation circuit so as to maintain fairly constant the power capability of a flyback converter despite the changes of the switching frequency.

This is accomplished by clamping the output of the error amplifier (VCOMP) to a value which decreases as the frequency of the signal fed into pin 1 (SYNC) builds up.

The frequency-to-voltage conversion needed to achieve this functionality is performed by detecting the peak voltage of the (synchronized) oscillator with a peak-holding circuit. One external capacitor only is required.

It is important to point out that shape, amplitude and duration of the synchronization pulses are of no concern with this technique.

APPLICATION INFORMATION

Detailed Pin Functions Description

Pin 1. SYNC (In/Out Synchronization). This function allows the IC's oscillator either to synchronize other controllers (master) or to be synchronized to an external frequency (slave).

As a master, the pin delivers positive pulses during the falling edge of the oscillator (see pin 2). In slave operation the circuit is edge triggered. Refer to fig. 21 to see how it works. When several IC work in parallel no master-slave designation is needed because the fastest one becomes automatically the master.
During the ramp-up of the oscillator the pin is pulled low by a 600µA internal sink current generator. During the falling edge, that is when the pulse is released, the 600µA pull-down is disconnected. The pin becomes a generator whose source capability is typically 7mA (with a voltage still higher than 3.5V).

In fig. 20, some practical examples of synchronizing the L5993 are given.

Pin 2. RCT (Oscillator). A resistor (R_T) and a capacitor (C_T), connected as shown in fig. 21 set the operating frequency f_{osc} of the oscillator.

C_T is charged through R_T until its voltage reaches 3V, then is quickly internally discharged. As the voltage has dropped to 1V it starts being charged again.

The frequency can be established with the aid of fig. 13 diagrams or considering the approximate relationship:

$$f_{osc} \cong \frac{1}{C_T \cdot (0.693 \cdot R_T + K_{T)}} \quad (1)$$

where K_T is defined as:

$$K_T = \begin{cases} 90, & V_{15} = VREF \\ 160 & V_{15} = GND/OPEN \end{cases} \quad (2)$$

and is linked to the duration of the falling edge of the sawtooth:

$$T_d \cong 30 \cdot 10^{-9} + K_T \cdot C_T \quad (3)$$

T_d is also the duration of the sync pulses deliv-

Figure 20. Sinchronizing the L5993.

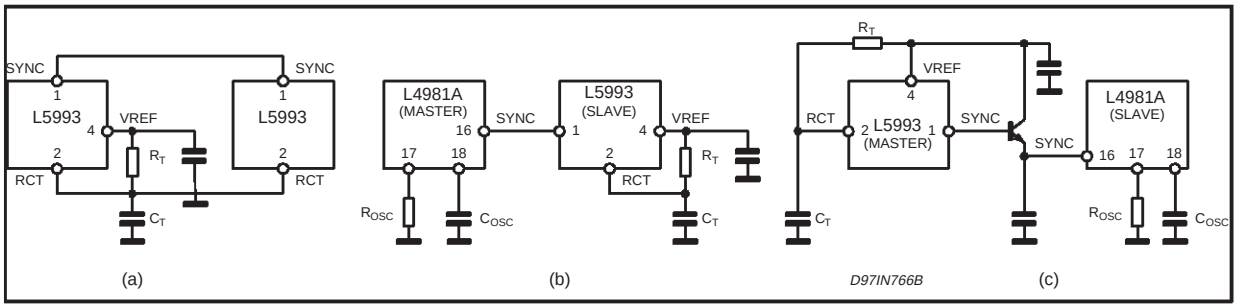
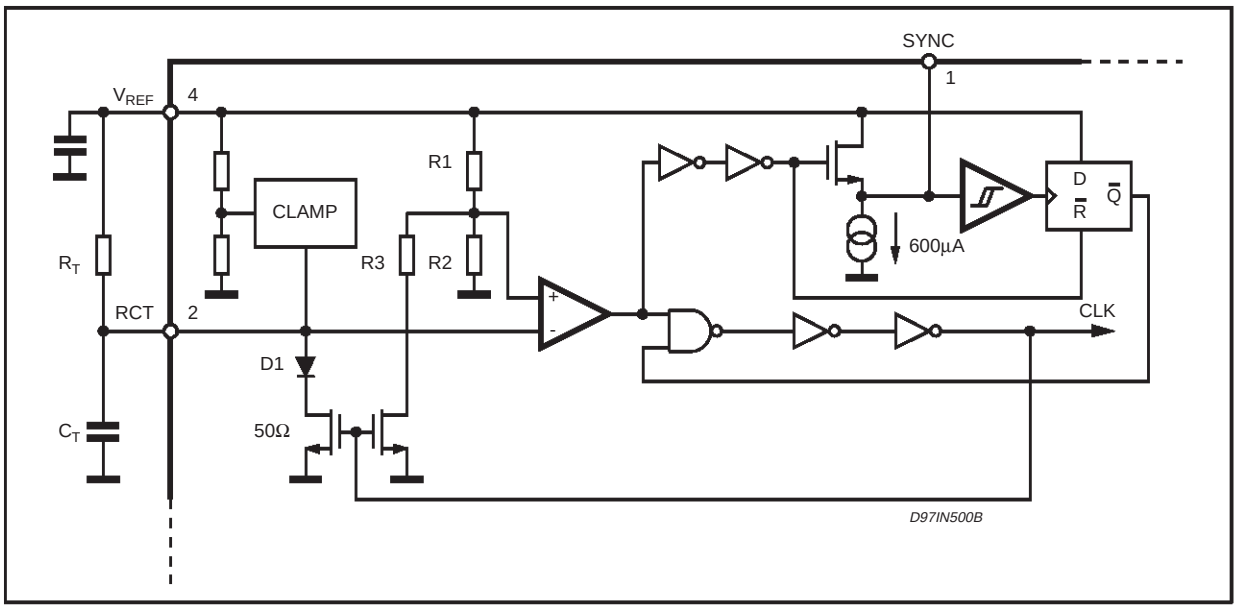


Figure 21. Oscillator and synchronization internal schematic.



ered at pin 1 and defines the upper extreme of the duty cycle range, D_X (see pin 15 for D_X definition and calculation).

In case V_{15} is connected to VREF, however, the switching frequency of the system will be a half f_{osc}.

If the IC is to be synchronized to an external oscillator, R_T and C_T should be selected for a f_{osc} lower than the master frequency in any condition (typically, 10-20%), depending on the tolerance of R_T and C_T .

Pin 3. DC (Duty Cycle Control). By biasing this pin with a voltage between 1 and 3 V it is possible to set the maximum duty cycle between 0 and the upper extreme D_X (see pin 15).

If D_{max} is the desired maximum duty cycle, the voltage V3 to be applied to pin 3 is:

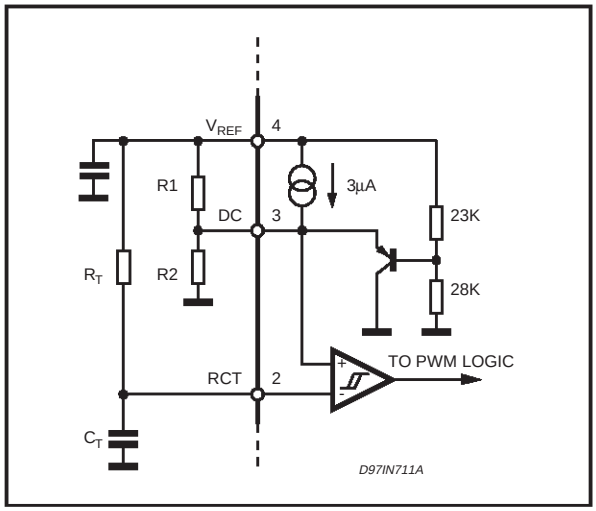
$$V_3 = 5 - 2^{(2-Dmax)} \quad (4)$$

D_{max} is determined by internal comparison between V3 and the oscillator ramp (see fig. 22), thus in case the device is synchronized to an external frequency f_{ext} (and therefore the oscillator amplitude is reduced), (4) changes into:

$$V_3 = 5 - 4 \cdot \exp\left(-\frac{D_{max}}{R_T \cdot C_T \cdot f_{ext}}\right) \quad (5)$$

A voltage below 1V will inhibit the driver output stage. This could be used for a not-latched device disable, for example in case of overvoltage protection (see application ideas).
If no limitation on the maximum duty cycle is required (i.e. $D_{MAX} = D_X$), the pin has to be left floating. An internal pull-up (see fig. 22) holds the voltage above 3V. Should the pin pick up noise (e.g. during ESD tests), it can be connected to VREF through a 4.7kΩ resistor.

Figure 22. Duty cycle control.



Pin 4. VREF (Reference Voltage). The device is provided with an accurate voltage reference (5V±1.5%) able to deliver some mA to an external circuit.

A small film capacitor (0.1 µF typ.), connected between this pin and SGND, is recommended to ensure the stability of the generator and to prevent noise from affecting the reference.

Before device turn-on, this pin has a sink current capability of 0.5mA.

Pin 5. VFB (Error Amplifier Inverting Input). The feedback signal is applied to this pin and is compared to the E/A internal reference (2.5V). The E/A output generates the control voltage which fixes the duty cycle.

The E/A features high gain-bandwidth product, which allows to broaden the bandwidth of the overall control loop, high slew-rate and current capability, which improves its large signal behavior. Usually the compensation network, which stabilizes the overall control loop, is connected between this pin and COMP (pin 6).

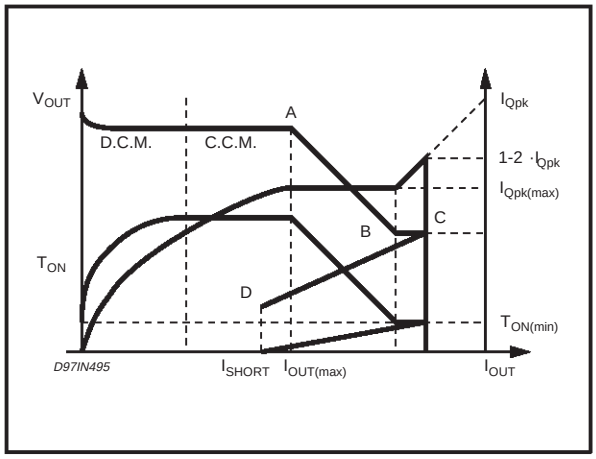
Pin 6. COMP (Error Amplifier Output). Usually, this pin is used for frequency compensation and the relevant network is connected between this pin and VFB (pin 5). Compensation networks towards ground are not possible since the L5993 E/A is a voltage mode amplifier (low output impedance). See application ideas for some example of compensation techniques.

Pin 7. SS (Soft-Start). At device start-up, a capacitor (Css) connected between this pin and SGND (pin 12) is charged by an internal current generator, ISSC, up to about 7V. During this ramp, the E/A output is clamped by the voltage across Css itself and allowed to rise linearly, starting from zero, up to the steady-state value imposed by the control loop. The maximum time interval during which the E/A is clamped, referred to as soft-start time, is approximately:

$$T_{ss} \cong \frac{3 \cdot R_{sense} \cdot I_{Qpk}}{I_{SSC}} \cdot C_{ss} \qquad (6)$$

where R_{sense} is the current sense resistor (see pin 13) and I_{Qpk} is the switch peak current (flowing through R_{sense}), which depends on the output

Figure 23. Regulation characteristic and related quantities



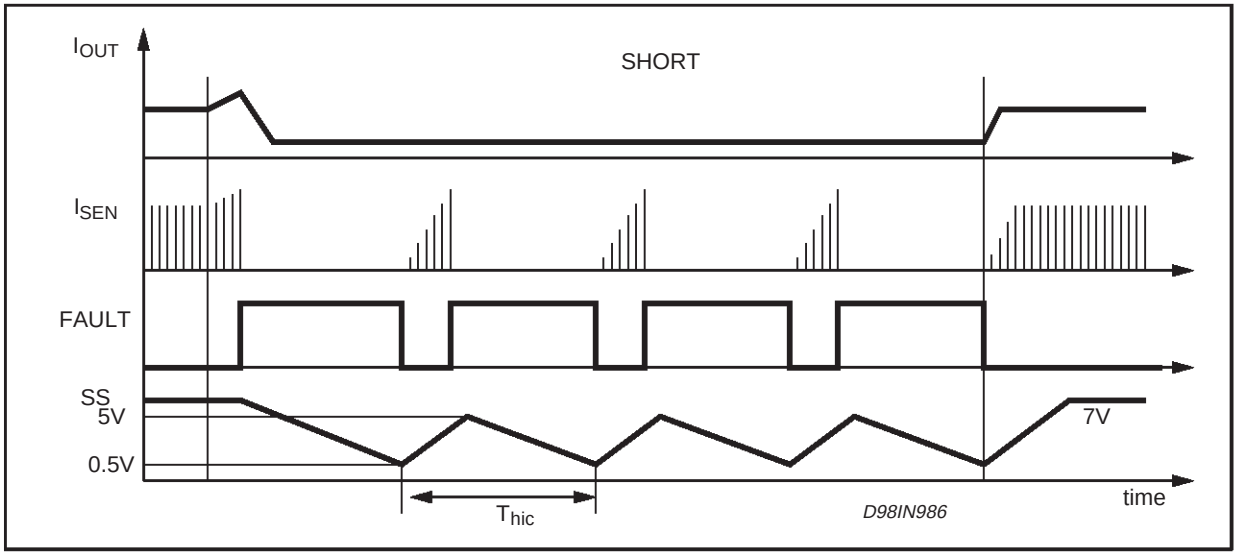
load. Usually, C_{SS} is selected for a T_{SS} in the order of milliseconds.

As mentioned before, the soft-start intervenes also in case of severe overload or short circuit on the output. Referring to fig. 23, pulse-by-pulse current limitation is somehow effective as long as the ON-time of the power switch can be reduced (from A to B). After the minimum ON-time is reached (from B onwards) the current is out of control.

To prevent this risk, a comparator trips an overcurrent handling procedure, named 'hiccup' mode operation, when a voltage above 1.2V (point C) is detected on current sense input (ISEN, pin 13). Basically, the IC is turned off and then soft-started as long as the fault condition is detected. As a result, the operating point is moved abruptly to D, creating a foldback effect. Fig. 24 illustrates the operation.

The oscillation frequency appearing on the soft-

Figure 24. Hiccup mode operation.



start capacitor in case of permanent fault, referred to as 'hiccup" period, is approximately given by:

$$T_{hic} \cong 4.5 \cdot \left(\frac{1}{I_{SSC}} + \frac{1}{I_{SSD}} \right) \cdot C_{ss} \quad (7)$$

Since the system tries restarting each hiccup cycle, there is not any latchoff risk.

"Hiccup" keeps the system in control in case of short circuits but does not eliminate power components overstress during pulse-by-pulse limitation (from A to C). Other external protection circuits are needed if a better control of overloads is required.

Pin 8. VCC (Controller Supply). This pin supplies the signal part of the IC. The device is enabled as VCC voltage exceeds the start threshold and works as long as the voltage is above the UVLO threshold. Otherwise the device is shut down and the current consumption is extremely low (<150µA). This is particularly useful for reducing the consumption of the start-up circuit (in the simplest case, just one resistor), which is one of the most significant contributions to power losses when a converter is lightly loaded.

An internal Zener limits the voltage on VCC to 25V. The IC current consumption increases considerably if this limit is exceeded.

A small film capacitor between this pin and SGND (pin 12), placed as close as possible to the IC, is recommended to filter high frequency noise.

Pin 9. VC (Supply of the Power Stage). It supplies the driver of the external switch and therefore absorbs a pulsed current. Thus it is recommended to place a buffer capacitor (towards PGND, pin 11, as close as possible to the IC) able to sustain these current pulses and in order to avoid them inducing disturbances.

This pin can be connected to the buffer capacitor directly or through a resistor, as shown in fig. 25, to control separately the turn-on and turn-off speed of the external switch, typically a PowerMOS. At turn-on the gate resistance is $R_g + R_{g'}$, at turn-off is R_g only.

Pin 10. OUT (Driver Output). This pin is the output of the driver stage of the external power switch. Usually, this will be a PowerMOS, although the driver is powerful enough to drive BJT's (1.6A source, 2A sink, peak).

The driver is made up of a totem pole with a high-side NPN Darlington and a low-side VDMOS, thus there is no need of an external diode clamp to prevent voltage from going below ground. An internal clamp limits the voltage delivered to the gate at 13V. Thus it is possible to supply the driver (Pin 9) with higher voltages without any risk

Figure 25. Turn-on and turn-off speeds adjustment

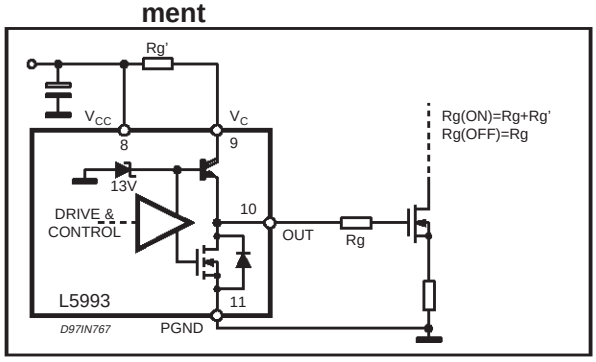
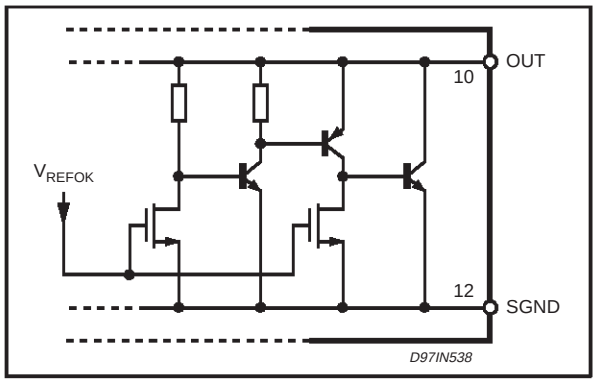


Figure 26. Pull-Down of the output in UVLO

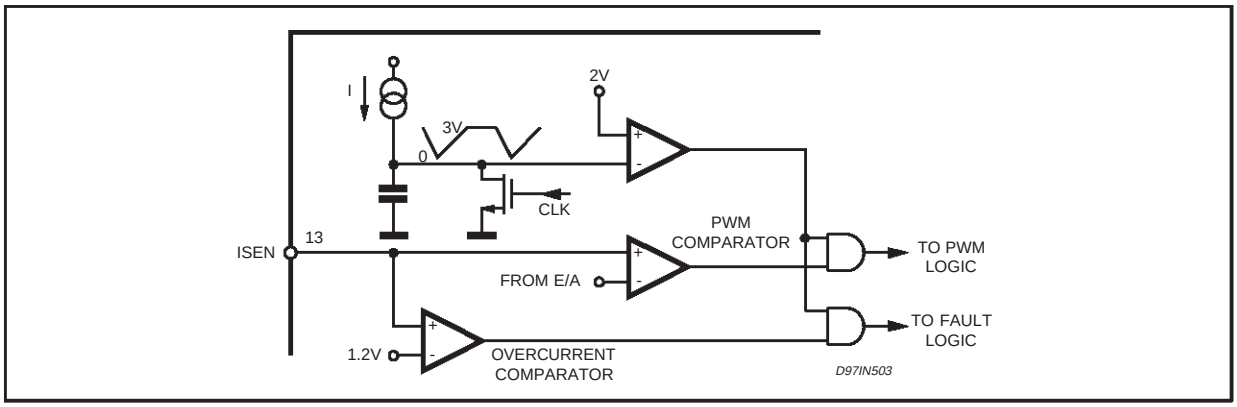


of damage for the gate oxide of the external MOS. The clamp does not cause any additional increase of power dissipation inside the chip since the current peak of the gate charge occurs when the gate voltage is few volts and the clamp is not active. Besides, no current flows when the gate voltage is 13V, steady state.

Under UVLO conditions an internal circuit (shown in fig.26) holds the pin low in order to ensure that the external MOS cannot be turned on accidentally. The peculiarity of this circuit is its ability to mantain the same sink capability (typically, 20mA @ 1V) from V_{CC} = 0V up to the start-up threshold. When the threshold is exceeded and the L5993 starts operating, V_{REFOK} is pulled high (refer to fig. 26) and the circuit is disabled.
It is then possible to omit the "bleeder" resistor (connected between the gate and the source of the MOS) ordinarily used to prevent undesired switching-on of the external MOS because of some leakage current.

Pin 11. PGND (Power Ground). The current loop during the discharge of the gate of the external MOS is closed through this pin. This loop should be as short as possible to reduce EMI and run separately from signal currents return.

Figure 27. Internal LEB.



Pin 12. SGND (Signal Ground). This ground references the control circuitry of the IC, so all the ground connections of the external parts related to control functions must lead to this pin. In laying out the PCB, care must be taken in preventing switched high currents from flowing through the SGND path.

Pin 13. ISEN (Current Sense). This pin is to be connected to the "hot" lead of the current sense resistor R_{sense} (being the other one grounded), to get a voltage ramp which is an image of the current of the switch (I_Q). When this voltage is equal to:

$$V_{13pk} = I_{Qpk} \cdot R_{sense} = \frac{V_{COMP} - 1.4}{3} \quad (8)$$

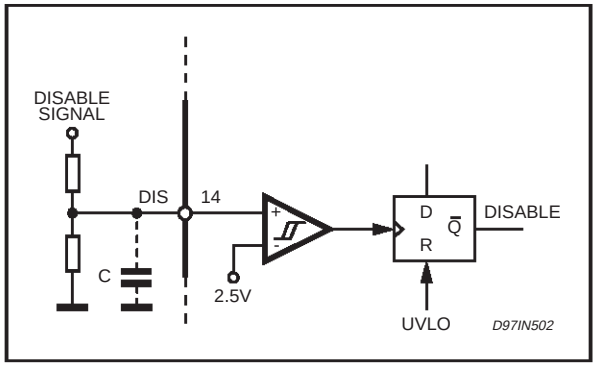
the conduction of the switch is terminated.
To increase the noise immunity, a "Leading Edge Blanking" of about 100ns is internally realized as shown in fig. 27. Because of that, the smoothing RC filter between this pin and R_{sense} could be removed or, at least, considerably reduced.

Pin 14. DIS (Device Disable). When the voltage on pin 14 rises above 2.5V the IC is shut down and it is necessary to pull VCC (IC supply voltage, pin 8) below the UVLO threshold to allow the device to restart.

The pin can be driven by an external logic signal in case of power management, as shown in fig. 28. It is also possible to realize an overvoltage protection, as shown in the section " Application Ideas".If used, bypass this pin to ground with a filter capacitor to avoid spurious activation due to noise spikes. If not, it must be connected to SGND.

Pin 15. DC-LIM (Maximum Duty Cycle Limit). The upper extreme, Dx, of the duty cycle range depends on the voltage applied to this pin. Approxi-

Figure 28. Disable (Latched)



mately,

$$D_X \cong \frac{R_T}{R_T + 230} \quad (9)$$

if DC-LIM is grounded or left floating. Instead, connecting DC-LIM to VREF (half duty cycle option), Dx will be set approximately to:

$$D_X \cong \frac{R_T}{2 \cdot R_T + 260} \quad (10)$$

and the output switching frequency will be halved with respect to the oscillator one because an internal T flip-flop (see block diagram, fig. 1) is activated. Fig. 29 shows the operation.

The half duty cycle option speeds up the discharge of the timing capacitor C_T (in order to get duty cycles as close as possible to 50%) so the oscillator frequency - with the same R_T and C_T - will be slightly higher.

The halving of frequency can be used to reduce losses at light load in all those systems that must comply with requirements regarding energy consumption (e.g. monitor displays, see "Application Ideas").

Figure 29. Half duty cycle option.

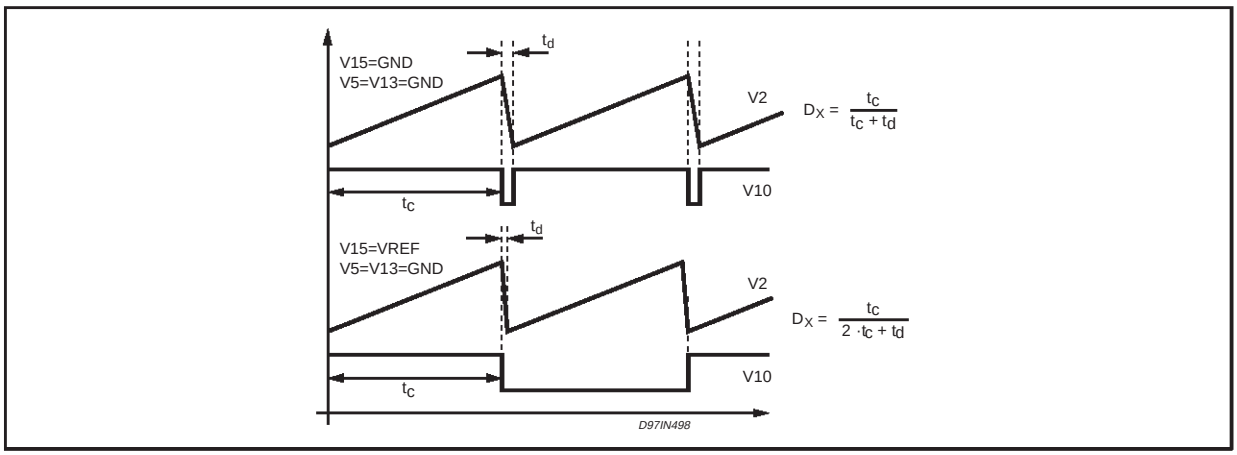
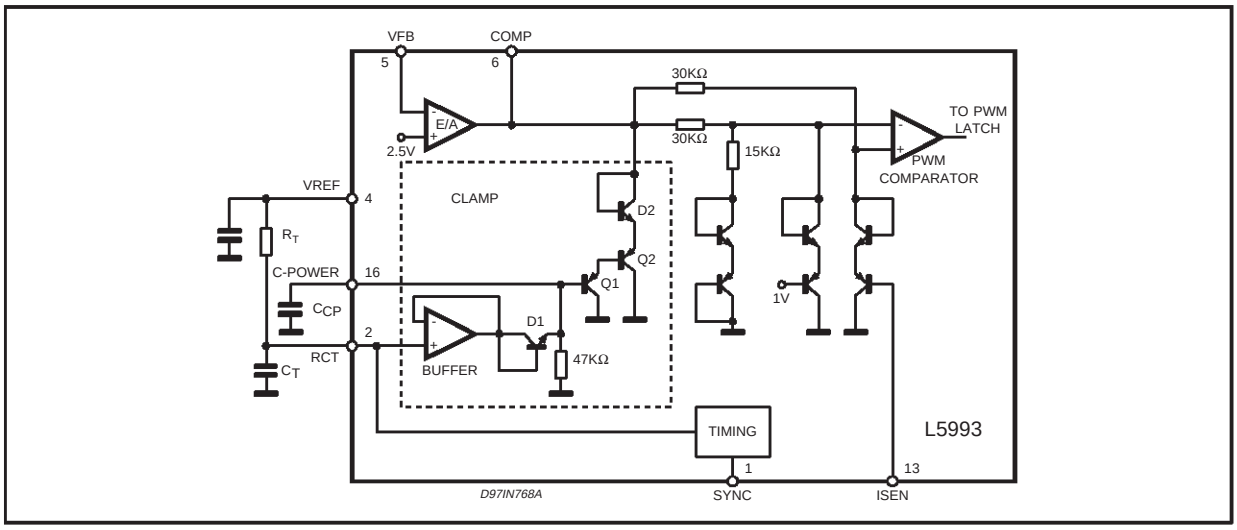


Figure 30. Constant Power circuit internal schematic



Pin 16. C-POWER (Constant Power Function). An external capacitor connected between this pin and SGND completes the peak-holding circuit that detects the peak voltage of the synchronized oscillator. The circuit gets a DC voltage (which decreases as the synchronizing frequency fed into pin 1 (SYNC) rises) used to clamp the error amplifier output (V_{COMP}), as shown in the detailed internal schematic of fig. 30.

In this way the pulse-by-pulse setpoint is moved downwards as the frequency rises (and vice versa for a frequency decrease, due to the 47kΩ discharge resistor) and, as a result, the maximum power deliverable to the load is held roughly constant.

The external capacitor must be large enough to get a real DC voltage on the pin. Considering the spread of the internal 47kΩ resistor, the minimum capacitance value (C_{CP}) needed to have less than 1% ripple superimposed on the DC voltage is:

$$C_{CP} > \frac{1}{330 \cdot f_{min}},$$

where f_{min} (Hz) is the minimum synchronizing frequency.

When this function is not used, pin 16 has to be connected directly to pin 4.

Considering the ordinary design criteria for the transformer, the circuit usually works well without any adjustment. Anyway, the variations of the maximum power limit on varying the switching frequency and/or the mains voltage can be minimized by modifying one or more of the following parameters:

- Primary inductance;
- Transformer turns ratio;
- Oscillator free-running frequency;
- Sense resistor.

A trial process is required, involving the parameters that are more practicable to modify. In fact, the optimum behavior is achieved for a specific combination of the above parameters and de-

pends both on the mains voltage range and the synchronization frequency range.

An additional "fine tuning" can be achieved by adding a small DC offset (in the ten mV) on the current sense pin (13, ISEN).

For wide range mains applications it is anyway recommended to compensate the propagation delay of the current sense path (PWM comparator + latch + driver) with the circuit shown in the "Application Ideas" section, fig. 41.

Layout hints

Generally speaking a proper circuitboard layout is vital for correct operation but is not an easy task. Careful component placing, correct traces routing, appropriate traces widths and, in case of high voltages, compliance with isolation distances are the major issues. The L5993 eases this task by putting two pins at disposal for separate current returns of bias (SGND) and switch drive currents (PGND) The matter is complex and only few important points will be here reminded.

1) All current returns (signal ground, power ground, shielding, etc.) should be routed separately and should be connected only at a single ground point.
2) Noise coupling can be reduced by minimizing the area circumscribed by current loops. This applies particularly to loops where high pulsed currents flow.
3) For high current paths, the traces should be doubled on the other side of the PCB whenever possible: this will reduce both the resistance and the inductance of the wiring.
4) Magnetic field radiation (and stray inductance) can be reduced by keeping all traces carrying switched currents as short as possible.
5) In general, traces carrying signal currents should run far from traces carrying pulsed currents or with quickly swinging voltages. From this viewpoint, particular care should be taken of the high impedance points (current sense input, feedback input, ...). It could be a good idea to route signal traces on one PCB side and power traces on the other side.
6) Provide adequate filtering of some crucial points of the circuit, such as voltage references, IC's supply pins, etc.

APPLICATION IDEAS

Here follows a series of ideas/suggestions aimed at either improving performance or solving common application problems of L5993 based supplies.

Figure 31. Typical application circuit for 15" Multisync monitor (70W)

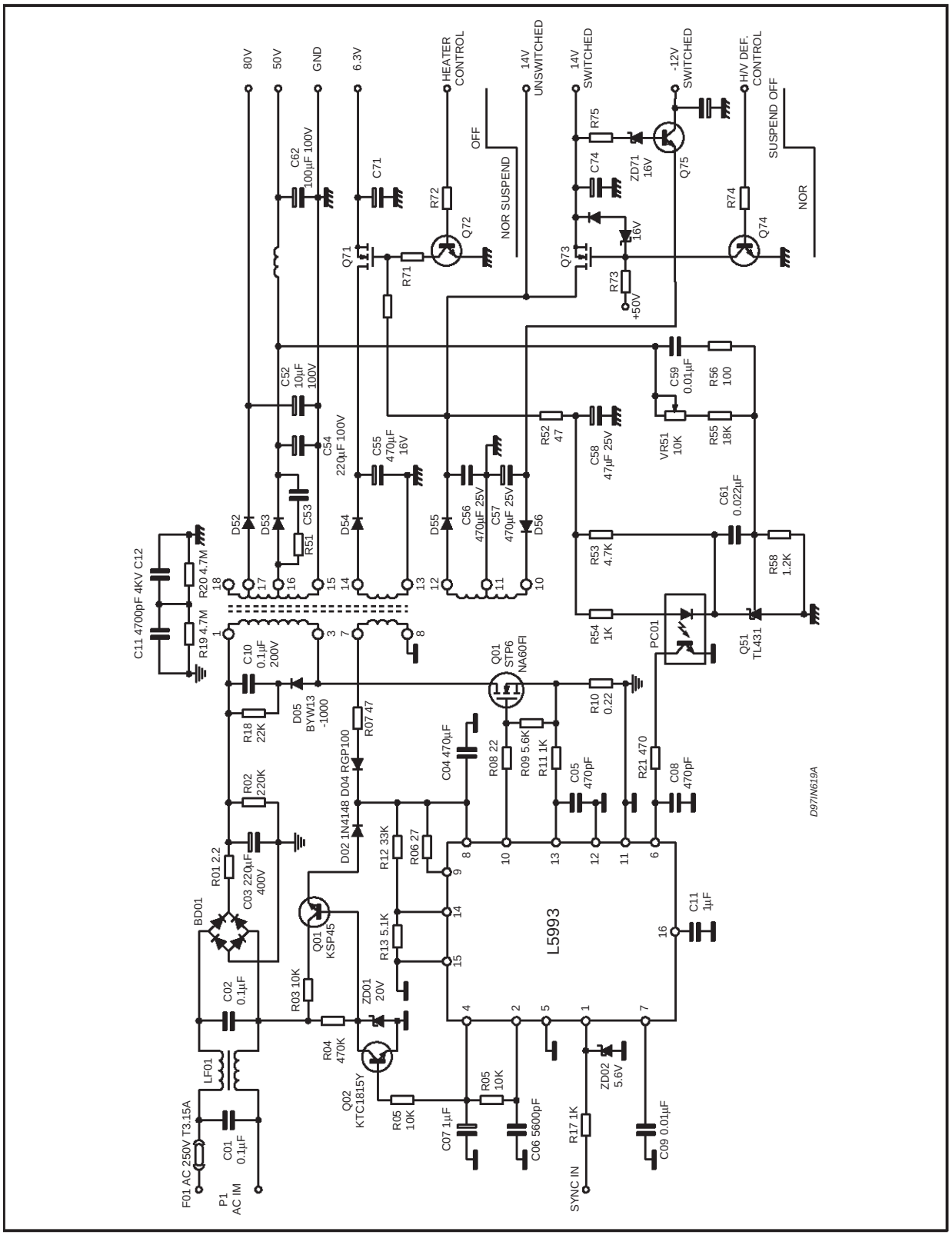


Figure 32. Isolated MOSFET Drive & Current Transformer Sensing in 2-switch Topologies

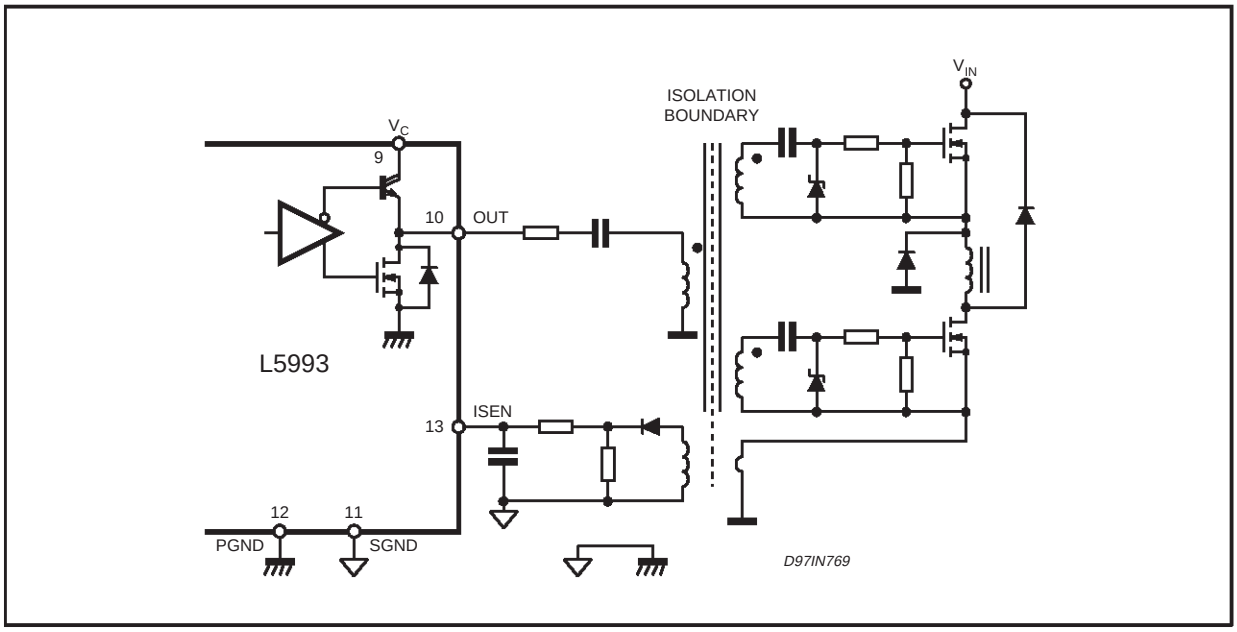


Figure 33. Low consumption start-up

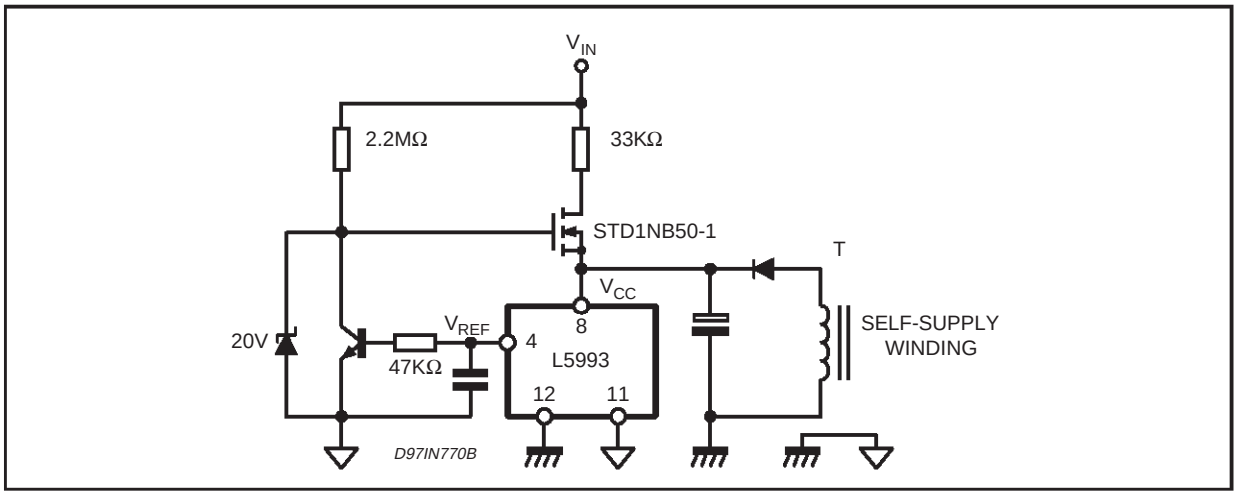


Figure 34. Bipolar Transistor Drive

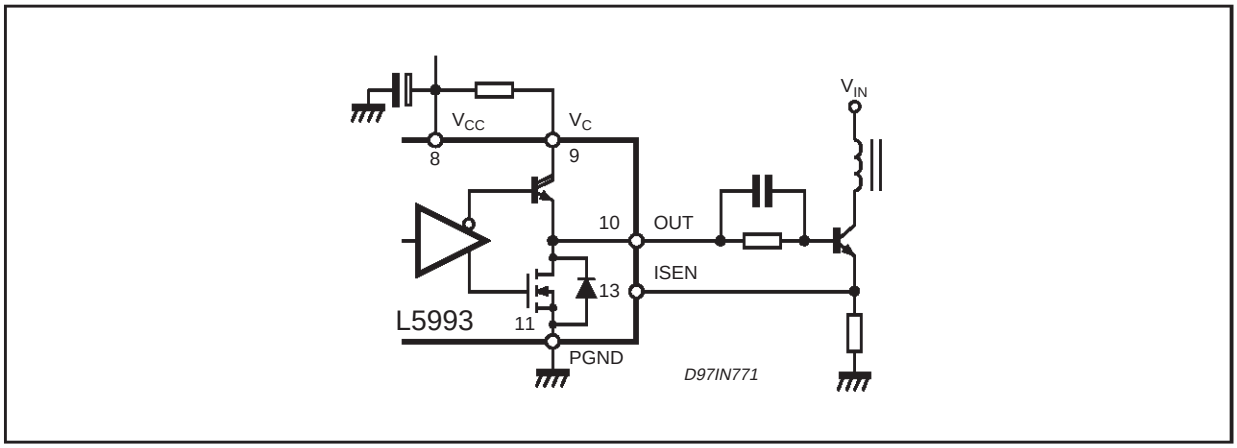
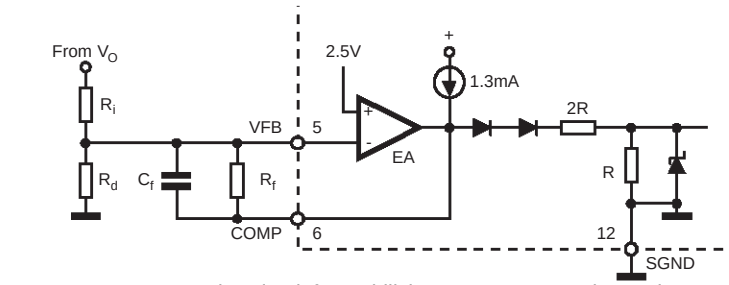
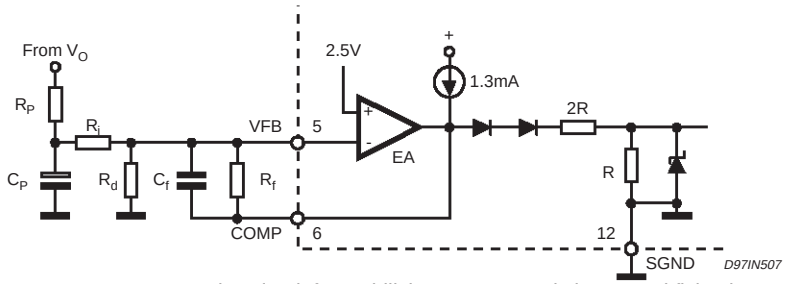


Figure 35. Typical E/A compensation networks.



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 36. Feedback with optocoupler

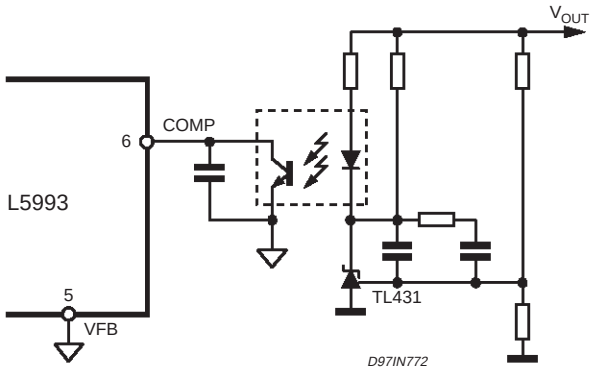


Figure 37. Slope compensation techniques

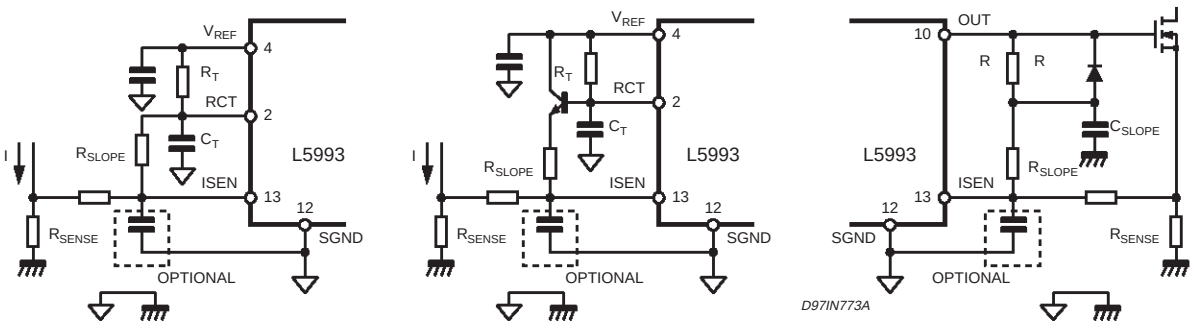


Figure 38. Protection against overvoltage/feedback disconnection (latched)

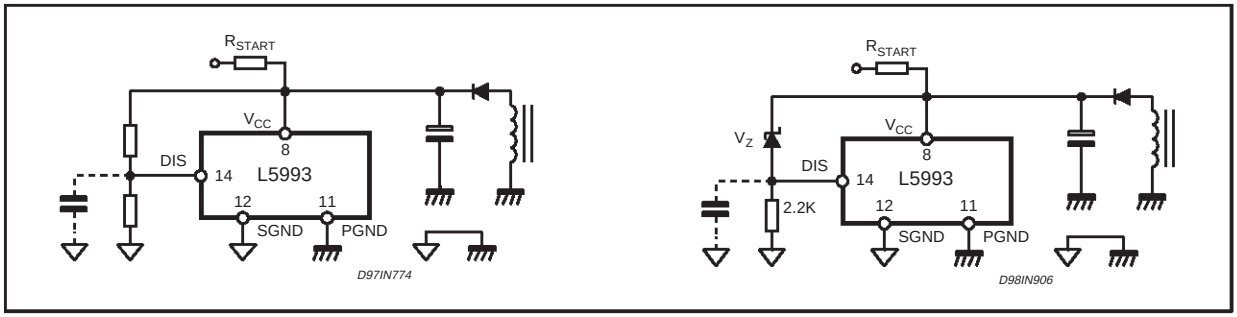


Figure 39. Protection against overvoltage/feedback disconnection (not latched)

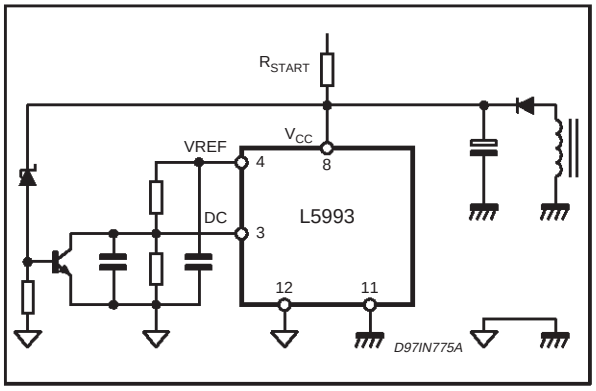


Figure 40. Device shutdown on overcurrent

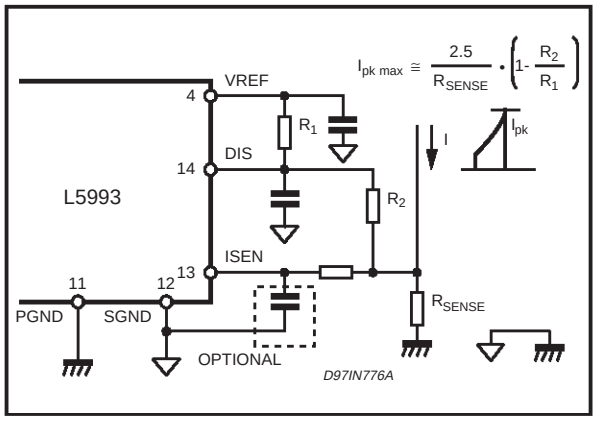


Figure 41. Constant power in pulse-by-pulse current limitation (flyback discontinuous)

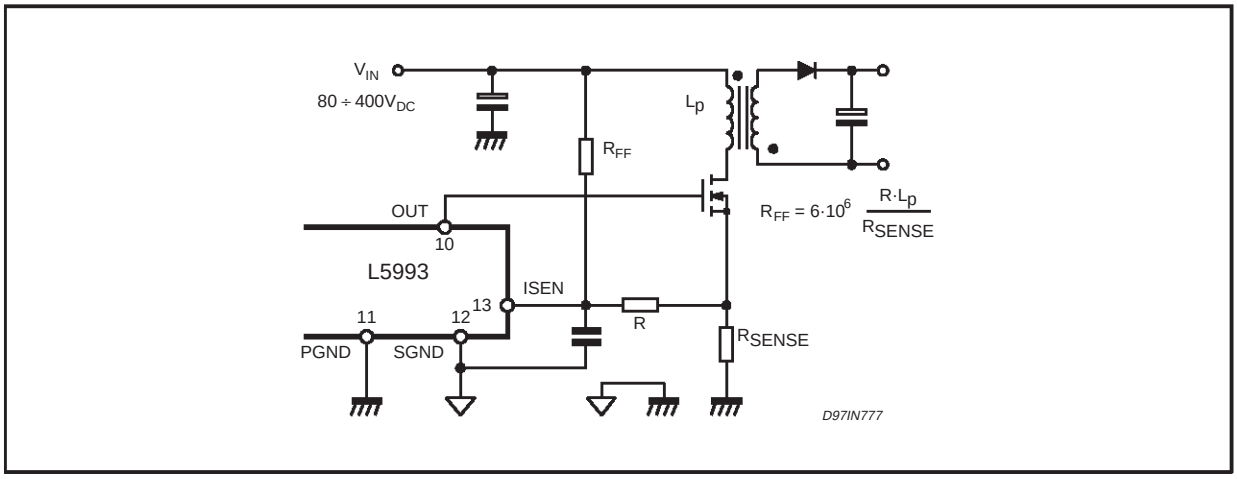


Figure 42. Voltage mode operation.

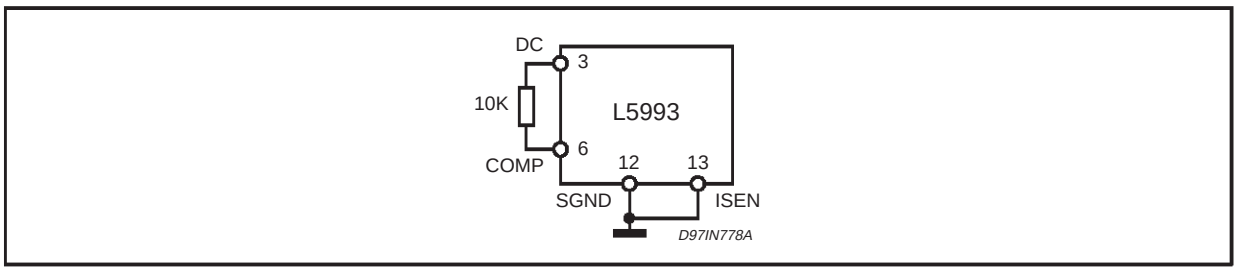


Figure 43. Device shutdown on mains undervoltage.

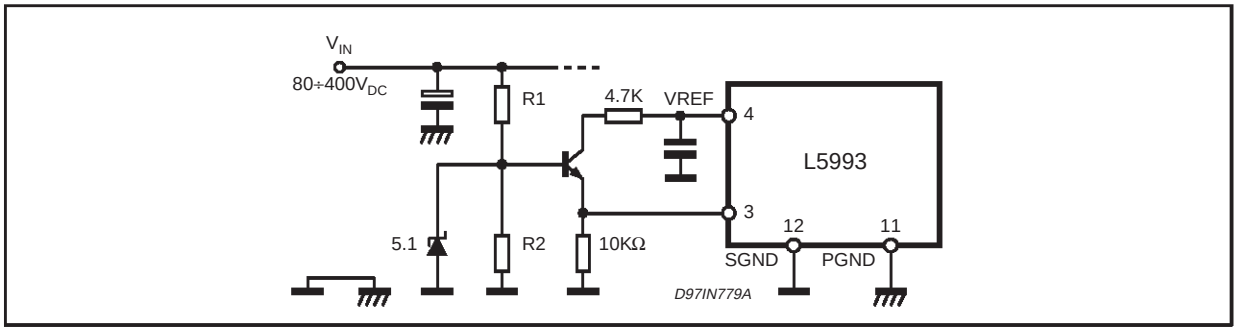


Figure 44. Constant power "Fine Tuning".

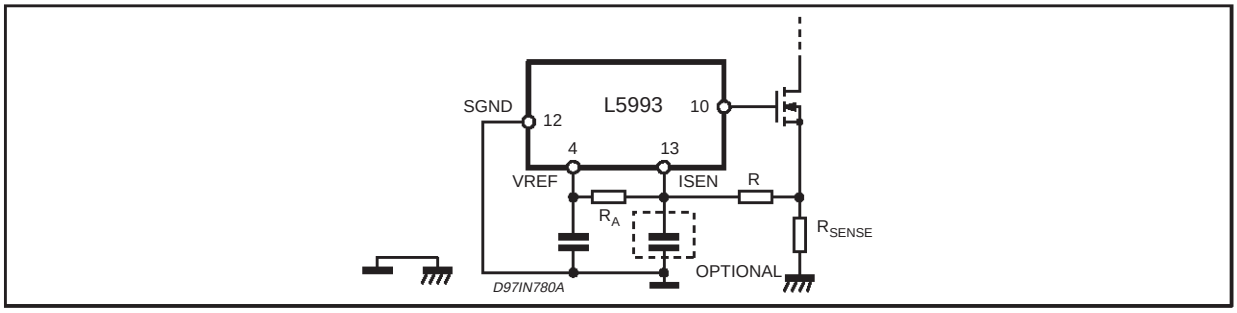


Figure 45. Synchronization to flyback pulses (for monitors).

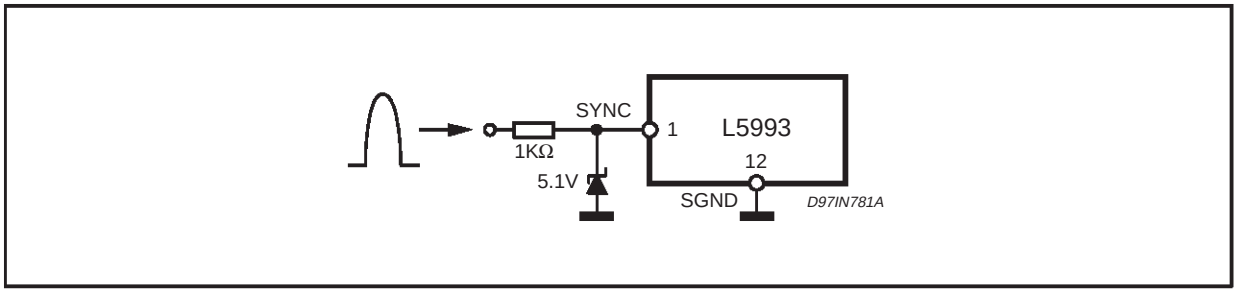
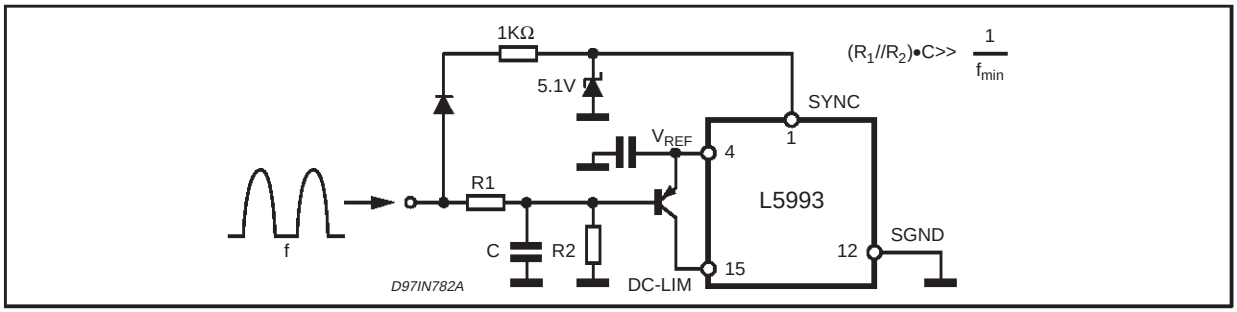
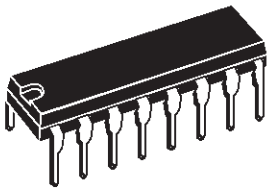


Figure 46. Switching frequency halving on absence of sync. signal (for monitor).

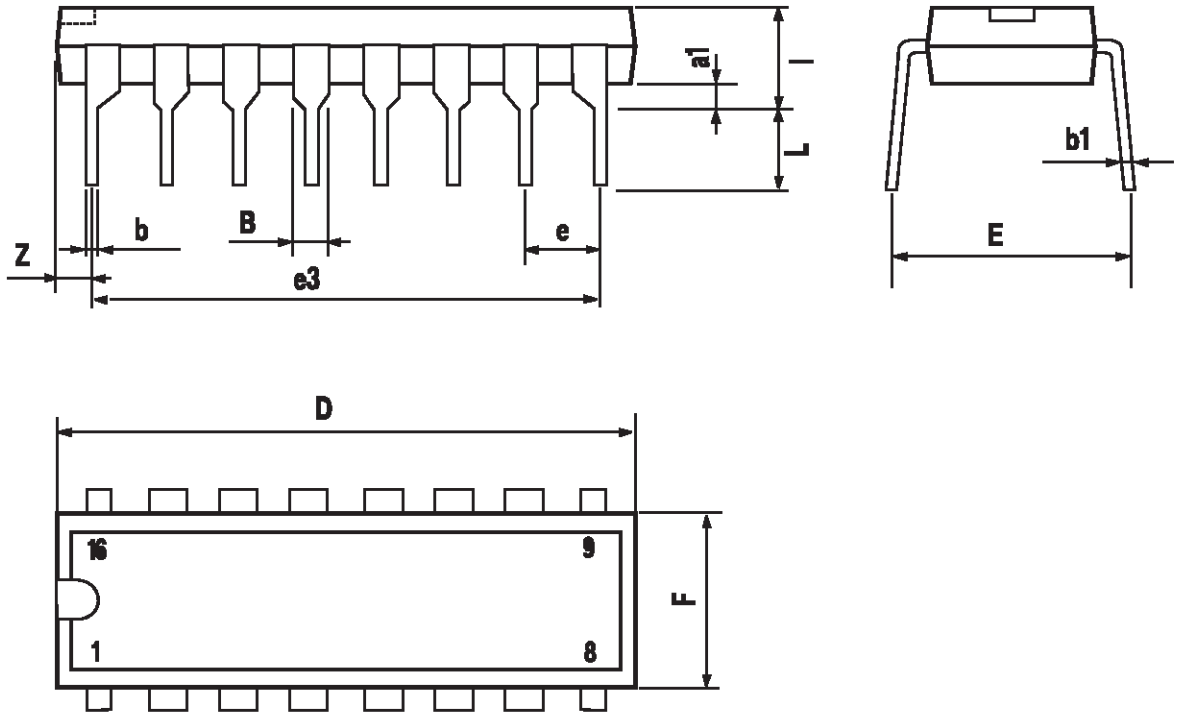


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA

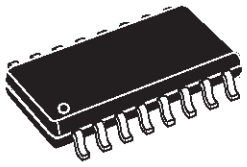


DIP16



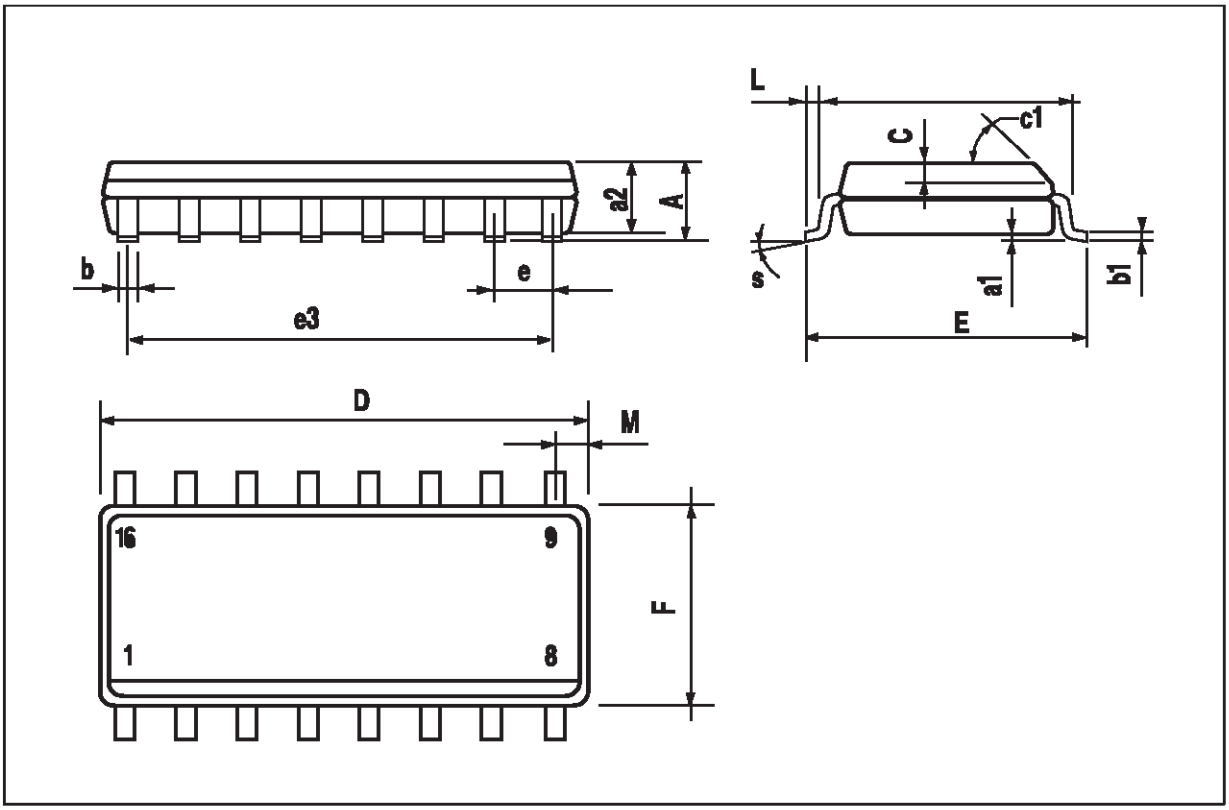
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F (1)	3.8		4	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.4		1.27	0.016		0.050
M			0.62			0.024
S	8°(max.)					

OUTLINE AND MECHANICAL DATA



SO16 Narrow

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).



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