Ordering number:ENN3245A

Monolithic Linear IC

LA5317M

Variable Divided Voltage Generator for LCD Use

Overview

The LA5317M is a variable divided voltage generator IC for multiple drive of LCD matrix.

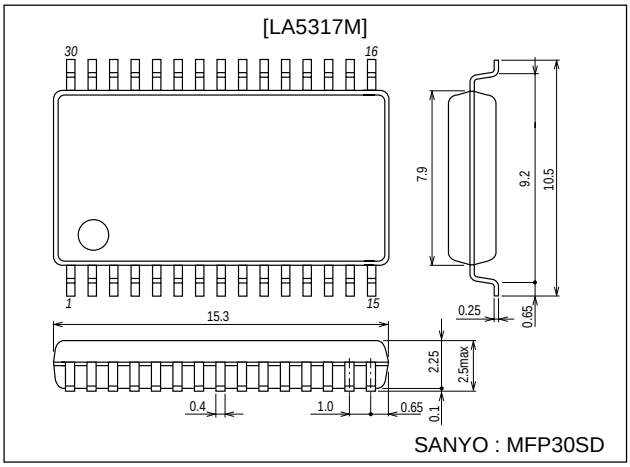
Features

- Power supply for variable bias LCD drive (1/5 to 1/20 bias available by on-chip resistances).
- 5 operational amplifiers to deliver 5 voltage outputs.
- Low current drain (1.6mA typ).
- Miniflat package.

Package Dimensions

unit:mm

3073A-MFP30SD



Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{EE} max	V_{CC}-V_{EE}	–38 to 0	V
Maximum output current	I_{OUT} max	V_1 to V_5	*±25	mA
Allowable power dissipation	Pd max		800	mW
Operating temperature	Topr		–20 to +75	˚C
Storage temperature	Tstg		–30 to +125	˚C

Note 1) Continuous operation (nonbreakdown) is guaranteed when operated at the maximum ratings shown above.

Note 2)* The maximum output current is a value specified under the conditions otherwise specified separately.

Operating Conditions at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{EE}	V_{CC}-V_{EE}	–35 to –10	V
Output current	I_{OUT1}	V_1	–0.5 to +10	mA
	$I_{OUT2, 3}$	V_2, V_3	–10 to +10	mA
	$I_{OUT4, 5}$	V_4, V_5	–15 to +0.5	mA

Note 3) Set V_{CC}, V_{EE} so that $|V_1|$, $|V_5-V_4|$ become 1V or greater.

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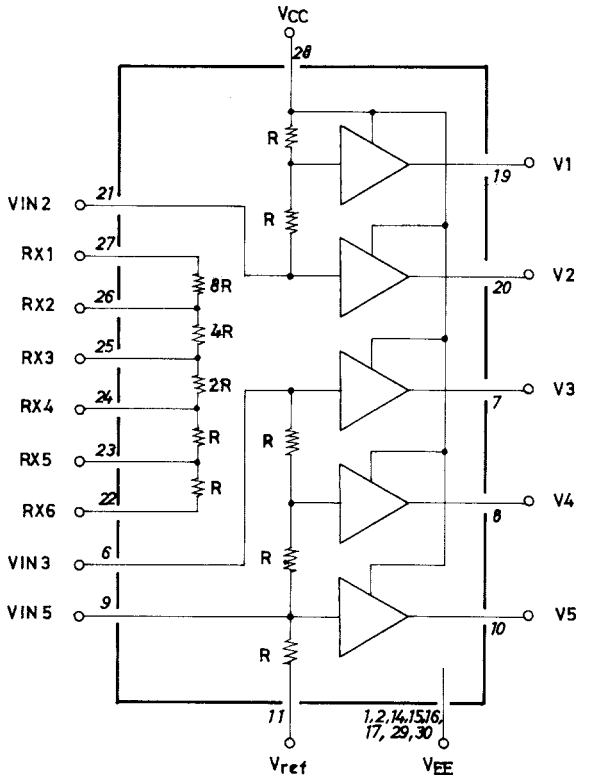
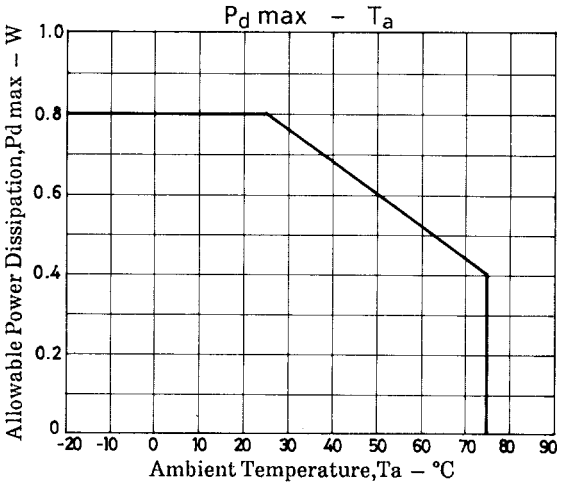
Operating Characteristics at Ta = 25˚C, V_{CC}–V_{EE}=20V, V_{REF}=V_{EE}, R_X=8R

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}, I_{EE}	V_{CC}, V_{EE} : V_{CC}=V_{EE}=20V, R_X=8R		1.6	3	mA
Output voltage ratio 1	Ra1	V_2/V_1	1.96	2.00	2.04	
Output voltage ratio 2	Ra2	$(V_5-V_3)/(V_5-V_4)$	1.96	2.00	2.04	
Output voltage ratio 3	Rb1	V_5/V_1	11.64	12.00	12.36	
Output voltage ratio 4	Rb2	V_5/V_2	5.82	6.00	6.18	
Output voltage ratio 5	Rb3	$V_5/(V_5-V_3)$	5.82	6.00	6.18	
Output voltage ratio 6	Rb4	$V_5/(V_5-V_4)$	11.64	12.00	12.36	
Internal resistance ratio 1	8R	R_X1-R_X2, Resistance ratio referenced to R across R_X5 and R_X6		8		
Internal resistance ratio 2	12R	R_X1-R_X3, Resistance ratio referenced to R across R_X5 and R_X6		12		
Internal resistance ratio 3	14R	R_X1-R_X4, Resistance ratio referenced to R across R_X5 and R_X6		14		
Internal resistance ratio 4	15R	R_X1-R_X5, Resistance ratio referenced to R across R_X5 and R_X6		15		
Internal resistance ratio 5	16R	R_X1-R_X6, Resistance ratio referenced to R across R_X5 and R_X6		16		
Resistance	R	R value when 0.5V is applied across R_X5 and R_X6		20		kΩ
Load regulation 1	ΔV_1	V_1 : –0.2mA<I_{OUT1}<+10.0mA			±20	mV
Load regulation 2	ΔV_2	V_2 : –0.2mA<I_{OUT2}<+10.0mA			±20	mV
Load regulation 3	ΔV_3	V_3 : –0.2mA<I_{OUT3}<+10.0mA			±20	mV
Load regulation –2	$-\Delta V_2$	V_2 : –10.0mA<I_{OUT2}<+0.2mA			±20	mV
Load regulation –3	$-\Delta V_3$	V_3 : –10.0mA<I_{OUT3}<+0.2mA			±20	mV
Load regulation –4	$-\Delta V_4$	V_4 : –10.0mA<I_{OUT4}<+0.2mA			±20	mV
Load regulation –5	$-\Delta V_5$	V_5 : –10.0mA<I_{OUT5}<+0.2mA			±20	mV

Equivalent Circuit Block Diagram





Note : Use the IC so that $V_{RX1} \geq V_{RX2} \geq V_{RX3} \geq V_{RX4} \geq V_{RX5} \geq V_{RX6}$ is obtained.

Pin Assingment