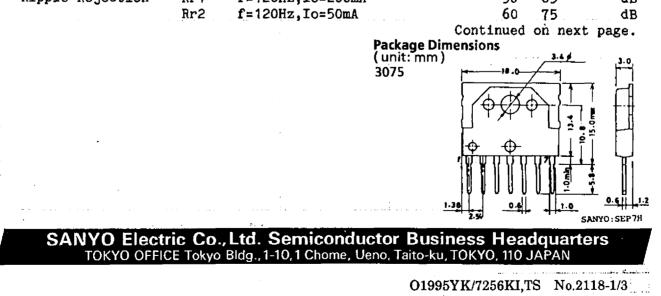
Ordering number: EN 2118A

				Monol	lithic Linear	C
NO	.2118A				LA566	6
SANYO		N	Aultifunction N	Aultiple Voltag	e Regulato	or
Use						
. Especially suit preamps and the		use in mic	orcomputer-c	controlled tun	ers, recei	ivers,
Functions and Feature	es					
. Two independent		ators con	tained in a	single chip	(13.0V/3	50mA,
5.6V/100mA) . Reset circuit wh	dah dal	twong the	meset stans]	on the needti	tro trong	1+1-00
negative transit:				on the postu	ive transi	LUION,
. Muting circuit w				reset output	to delive	r the
muting signal			-	-		
(We have the LAS			on function fo	or reset, muti	ing is pro	vided
on the output vo.	ltage si	de.)	a ser e e			• • •
Maximum Ratings at Ta	a=25 ⁰ C				unit	
Input Voltage		V_IN1,2		36	V	
Output Current		IQUT1.2	Internal	20	•	
Allowable Power Dis	ssipatio	n Pdmax'	IC only	1.6	W	
Operating Temperati	ure	Topr	·	-30 to +80		
Storage Temperature	е	Tstg		-40 to +125	°C	
Operating Conditions	at Ta=2	5 ⁰ C			unit	
Input Voltage		V _{IN1}	$I_{OUT1} = 200 \text{mA}$	16.2 to 35	v	
		VIN2	I _{OUT2} =50mA	8.7 to 35	V	
Operating Characteri	stics at	$Ta=25^{\circ}c$. V		IOV min	typ max	unit
Quiescent Current	IN1		IN1	1.8	2.8 3.8	mA
• • • • • • • • • • • • • • • • • • • •				3.8	5.8 7.8	mA
Output Voltage		$I_{OUT1} = 200$	mA		13.0 13.7	v
:	V02	$I_{\text{OUT}} = 50 \text{m}$	A	5.2	5.6 6.0	v
Line Regulation	Voli	VTNO=19 C	5 27V		6 20	mV
	*012	$V_{\rm IN2}=9$ to	18V		2 20	mV
Load Regulation	'old1	Io=0 to 3	50mA		10 30	mV
	_old2	Io=0 to 10			2 20	mV
Ripple Rejection	U T. 1	f=120Hz,I		56	65 75	dB
	Rr2	f=120Hz,I		60 Continued	75 on next p	dB



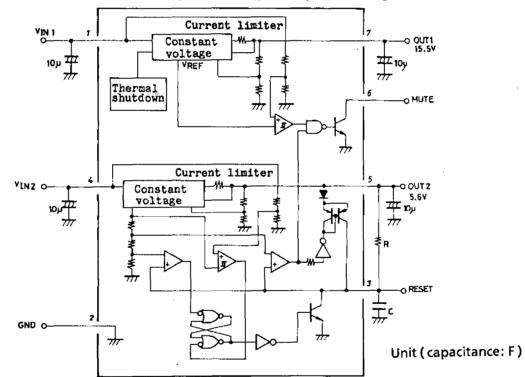
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Continued from preceding page.

•		min	typ	max	unit
Input-Output Voltage Drop	Vdr1 Io=200mA		1.6	2.5	· V
	Vdr2 Io=50mA	(Note1)	1.5	2.5	v
Reset Detect Voltage	$\triangle V_{R} \triangle V_{R} = V_{R} - Vo2$	Io2=50mA 1.65	1.9	2.2	v
Reset Detect Hysteresis Voltage	$\Delta v_{\rm H}^{\rm A}$ K K	50	75	110	mV
Timer Compare Voltage	V _{C1}	1.0	1.2	1.4	v
	V _{C2}	0.06	0.13	0.18	v
Timer Input Bias Current	ITB (Note	2)	-	250	nA
Muting Detect Voltage	$\triangle V_M = V_M - V_0 1$	Ío1=200mA 1.0	1.5	2.0	v
Muting Output Voltage	V _{OMUTE} I _{OMUTE} =51	nA	0.1	0.15	v
Muting Detect Hysteresis Voltage	△V _{MH}	110	160	210	mν

Note 1: V_R is the voltage of V_{IN2} at the time reset is turned OFF. Note 2: V_M is the voltage of V_{IN1} at the time muting is turned OFF.

Equivalent Circuit Block Diagram, Pin Assignment, and Peripheral Circuit

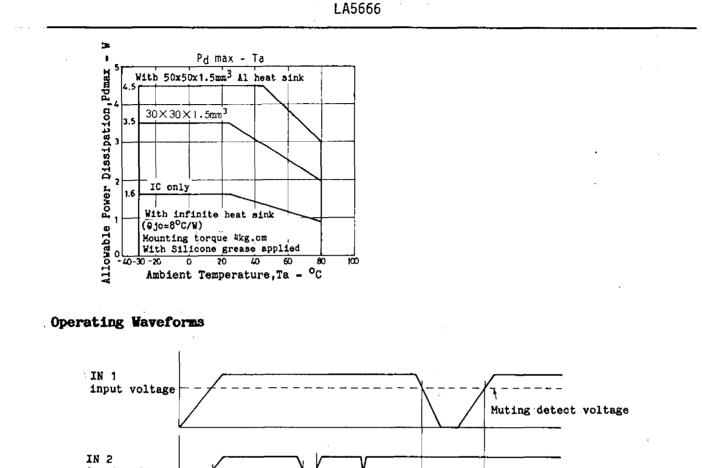


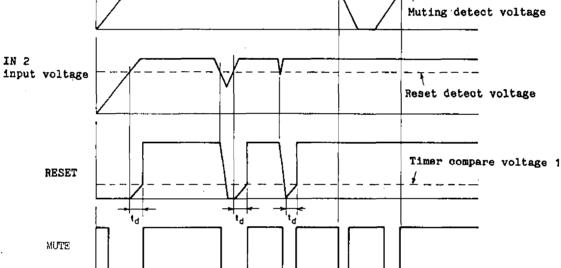
Pin No.	Name	Description
1	<u>V</u> IN1 GND	Input pin for 13.0V output line
2	GND '	Ground
3	RESET	Reset delay tine and output pin
4		Input pin for 5.6V output line
5	OUT2	5.6V output pin
6	MUTE	Muting signal output pin
7	OUT 1	13.0V output pin

.

(Note) The reset delay time is set by R. C.







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