Ordering number:EN3804B

Monolithic Linear IC

LA7217, 7217M

Synchronizing Signal Separator with AFC and Sync Detector

Overview

The LA7217 and 7217M are synchronizing signal separator ICs with AFC and AFC Lock detector designed to be used in video equipments such as VCR and TV sets. VCO with ceramic oscillator and PLL horizontal sync detector provide an adjust-free, percision sync detection system.

Functions

- Horizontal sync separation.
- Vertical sync separation.
- VCO ($32f_H$).
- AFC.
- Sync signal detection.

Features

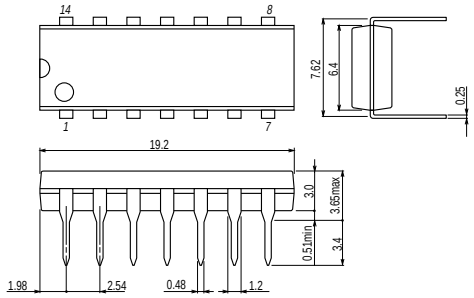
- Use of a ceramic oscillator requiers no adjustment.
- Negative polarity output.
- High impedance video signal input pin.
- 5V supply voltage.

Package Dimensions

unit:mm

3003A-DIP14

[LA7217]

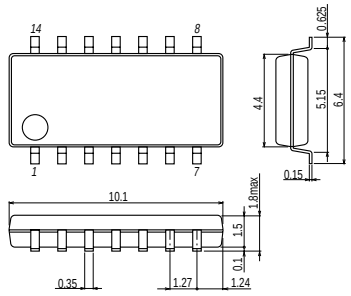


SANYO : DIP14

unit:mm

3034A-MFP14

[LA7217M]



SANYO : MFP14

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SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquaters

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Specifications

Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7	V
Allowable power dissipation	Pd max		150	mW
Operating temperature	Topr		–15 to +65	˚C
Storage temperature	Tstg		–40 to +125	˚C

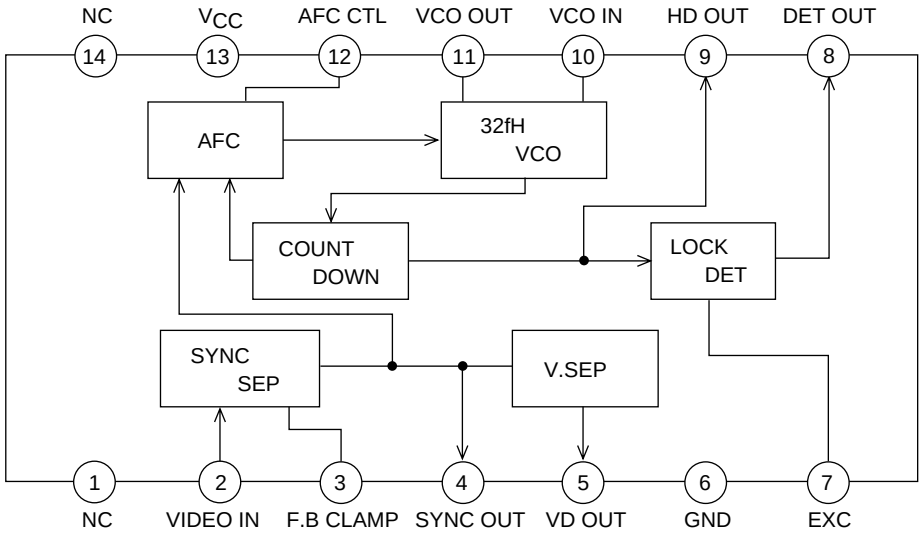
Operating Conditons at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5.0	V
Operating voltage range	V_{CC} op		4.5 to 5.5	V

Operating Characteristics at Ta = 25˚C, V_{CC}=5V

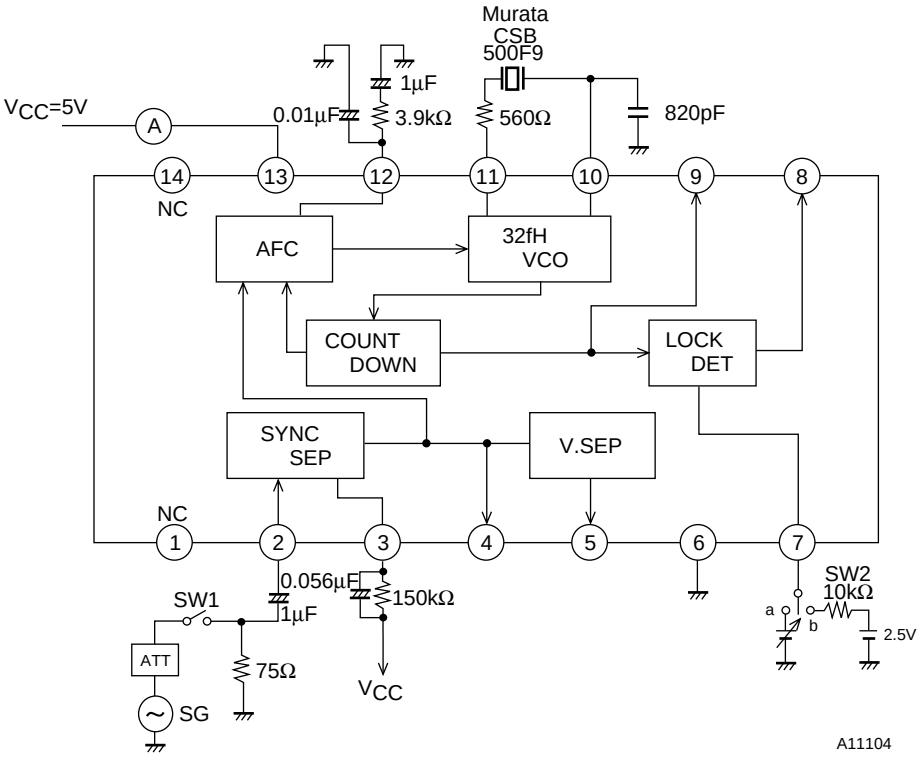
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	Standard color bar input	4.9	7	9.1	mA
Sync separation minimum input level	V_{IN} min		–15	–11	–8	dB
HD output delay time	t_{HD}	From pin 2 to pin 9	0.1	0.5	0.9	µs
HD output pulse width	t_{HW}		3.6	4.0	4.4	µs
VD output delay time	t_{VD}	From pin 2 to pin 5	9	13	17	µs
VD output pulse width	t_{VW}		0.16	0.21	0.26	ms
Free-running frequency	f_O	SW1 off	15.4	15.75	16.1	kHz
Capture Range 1	f_{CH}	Judgment by comparison of pin 9 with pin 2	300	500		Hz
Capture Range 2	f_{CL}	Judgment by comparison of pin 9 with pin 2	1000	1500		Hz
SYNC out, high level voltage	V_{SH}	Level on pin 4	3.9	4.2		V
SYNC out, low level voltage	V_{SL}	Level on pin 4		0.8	1.0	V
HD out, high level voltage	V_{HH}	Level on pin 9	3.9	4.2		V
HD out, low level voltage	V_{HL}	Level on pin 9		0.8	1.0	V
VD out, high level voltage	V_{VH}	Level on pin 5	3.9	4.2		V
VD out, low level voltage	V_{VL}	Level on pin 5		0.8	1.0	V
DET out, high level voltage	V_{DH}		4.8	5.0		V
DET out, low level voltage	V_{DL}	SW1 off		0.1	0.3	V
Comparator threshold high level voltage	V_{TH}	SW2–a	2.7	2.95	3.2	V
Comparator threshold low level voltage	V_{TL}	SW2–a	2.4	2.7	3.0	V
Threshold width	V_{TW}	V_{TH}–V_{TL}	0.10	0.22	0.40	V
DET operating current, high level	I_{DH}	SW2–b	40	65	90	µA
DET operating current, low level	I_{DL}	SW2–b	40	65	90	µA

Block Diagram

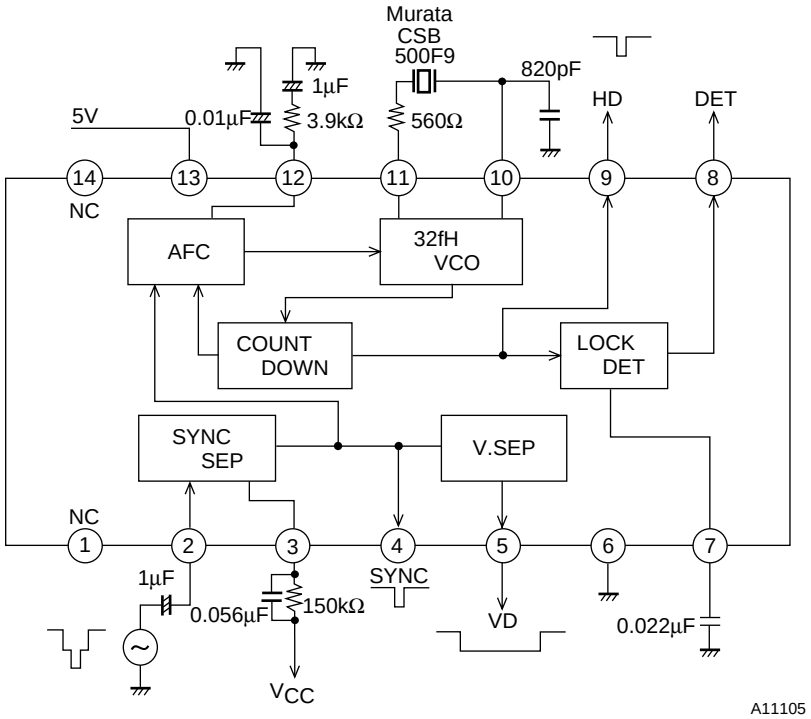


A11103

Test Circuit



Sample Application Circuit



- DET OUT becomes high upon lock.
- When feeding video signal to the input pin directly, keep DC level between 2 and 3.5 volts.
- Standard video input is 1 Vp-p.

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