

SANYO Semiconductors DATA SHEET

LB11620T

Monolithic Digital IC Brushless Motor Driver

Overview

The LB11620T is a direct PWM drive predriver IC that is optimal for three-phase power brushless motors. A motor driver circuit with the desired output capability (voltage and current) can be implemented by adding discrete transistors or other power devices to the outputs of this IC. Since the LB11620T is provided in a miniature package, it is also appropriate for use with miniature motors as well.

Features

- Three-phase bipolar drive
- Direct PWM drive (input of either a control voltage or a variable-duty PWM signal)
- Built-in forward/reverse switching circuit
- Full complement of protection circuits (current limiter, low-voltage, and automatic recovery lock (motor constraint) protection circuits)
- Selectable Hall sensor signal pulse output

Specifications

Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V _{CC} max	V _{CC} pin	18	V
Output current	I _O max	UL, VL, WL, UH, VH, WH pins	30	mA
Allowable power dissipation	Pd max	*Mounted on a circuit board.	0.8	W
Operating temperature	Topr		-20 to +100	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a circuit board : 114.3mm×76.1mm×1.6mm, glass epoxy board.

Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

> SANYO Semiconductor Co., Ltd. www.semiconductor-sanyo.com/network

Recommended Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1-1	V _{CC} 1-1	V _{CC} pin	8 to 17	V
Supply voltage range 1-2	V _{CC} 1-2	$V_{\mbox{CC}}$ pin, with $V_{\mbox{CC}}$ shorted to VREG	4.5 to 5.5	V
Output current	IO	UL, VL, WL, UH, VH, WH pins	25	mA
5 V constant voltage output current	IREG		-30	mA
HP pin voltage	VHP		0 to 17	V
HP pin output current	IHP		0 to 15	mA
RD pin voltage	VRD		0 to 17	V
RD pin output current	IRD		0 to 15	mA

Electrical Characteristics at $Ta = 25^{\circ}C$, $V_{CC} = 12V$

Decomptor	Symbol	Conditions	Ratings			Linit
Parameter			min	typ	max	Unit
Supply voltage 1	ICC1			12	16	mA
5V constant voltage output (VREG pi	n)					
Output voltage	VREG		4.7	5.0	5.3	V
Line regulation	∆VREG1	V _{CC} = 8 to 17V		40	100	mV
Load regulation	∆VREG2	I _O = -5 to -20mA		10	30	mV
Temperature coefficient	∆VREG3	Design target		0		mV/°C
Low-voltage protection circuit (VREC	G pin)					
Operating voltage	VSDL		3.5	3.7	3.9	V
Clear voltage	VSDH		3.95	4.15	4.35	V
Hysteresis	ΔVSD		0.3	0.45	0.6	V
Output Block						
Output voltage 1-1	VOUT1-1	Low level $I_{O} = 400 \mu A$		0.2	0.5	V
Output voltage 1-2	V _{OUT} 1-2	Low level I _O = 10mA		0.9	1.2	V
Output voltage 2	V _{OUT} 2	High level I _O = -20mA	V _{CC} -1.1	V _{CC} -0.9		V
Output leakage current	lOleak				10	μΑ
Hall Amplifier Block						
Input bias current	IHB (HA)		-2	-0.5		μΑ
Common-mode input voltage range 1	VICM1	When a Hall effect sensor is used	0.5		V _{CC} -2.0	V
Common-mode input voltage range 2	VICM2	For single-sided input bias (Hall IC application)	0		V _{CC}	V
Hall input sensitivity			80			mVp-p
Hysteresis	ΔV _{IN} (HA)		15	24	40	mV
Input voltage low \rightarrow high	VSLH (HA)		5	12	20	mV
Input voltage high \rightarrow low	VSHL (HA)		-20	-12	-5	mV
PWM Oscillator (PWM pin)						
High-level output voltage	V _{OH} (PWM)		2.75	3.0	3.25	V
Low-level output voltage	V _{OL} (PWM)		1.2	1.35	1.5	V
External capacitor charge current	ICHG	VPWM = 2.1V	-120	-90	-65	μΑ
Oscillator frequency	f (PWM)	C = 2000pF		22		kHz
Amplitude	V (PWM)		1.4	1.6	1.9	Vp-р

Continued on next page

Parameter Symbol Conditions jumit type max type E1+ pin Input isok current IB (C1) Input web isok current Input solutage ange VCR Input solutage ange VCR Input solutage ange VCR Input solutage ange VCR	Continued from preceding page.						
Lep in min by max Exp in Input bias current IB (CTL) 1 1 1 μ A Common-mode input voltage range VCR4 Output duty 100% 0 3.0 V V Input voltage 1 VCTL1 Output duty 00% 1.8 0 V Input voltage 1L VCTL2 Output duty 00% 1.8 0 V Input voltage 1L VCTL1 Design target value. 1.28 0 V Input voltage 2L VCTL2L Design target value. 1.12 0 V Input voltage 2H VCTL2L Design target value. 1.14 V V Input voltage 2H VCTL2H Design target value. 1.14 V V Input voltage 2H VCTL2H Design target value. 1.14 V V Input voltage 2H VCTL2H Design target value. 1.14 V V Output staration voltage VPTL Log and target value. 1.14 V V	Parameter	Symbol	Conditions		Ratings		
Et pin Input bias current B (CTL) -1 -1 V REG-17 V Common-mode input voltage range VICM 0.0 VREG-17 V Input voltage 1 VCTL1 Output duly 100% 1.0 1.38 V Input voltage 2 VCTL2 Output duly 00% 1.28 V V Input voltage 2L VCTL1 Design target value. 2.22 V V Input voltage 2L VCTL1H Design target value. 1.29 V V Input voltage 2L VCTL2H Design target value. 1.29 V V Input voltage 2H VCTL2H Design target value. 1.44 Incut voltage V Mythen VREG = 5.3V, 00% Intervelow Intervelow Intervelow V V CAD tastardian voltage VHL Iog intarget value. Intervelow Intervelow V CAD tastardian voltage VHL Iog intarget value. Intervelow Intervelow V CAD tastardinacabotine voltage		,		min	typ	max	
Input isourientIB (CTL)Imput ontege and the second s	El+ pin						
Common-mode input voltage range VCM 0 VKE0-1.7 V input voltage 1 VCTL1 Output duity 0% 1.38 V input voltage 1 VCTL2 Output duity 0% 1.38 V input voltage 1 VCTL2 Design target value. 2.82 V V input voltage 1 VCTL2 Design target value. 1.29 V V input voltage 2 VCTL2 Design target value. 3.318 V V input voltage 2H VCTL1 Design target value. 3.318 V V input voltage 2H VCTL2H Design target value. 1.44 V V input voltage 2H VCTL2H Design target value. 1.44 V V input voltage 2 VCTL2H Design target value. 1.44 V V input voltage 2 VCTL2H Design target value. 1.41 2.5 V input voltage 2 VPCL2 Iop = 10mA 0.2 0.5 V Cup-setoriot	Input bias current	IB (CTL)		-1		1	μΑ
Input voltage 1 VCTL 1 Output duty 100% I 3.0 V Input voltage 2 VCTL 2 Output duty 0% I 1.35 V Input voltage 1. VCTL 1. Design target value. When VREG 4.7V, 100% I 2.82 V Input voltage 1. VCTL 1. Design target value. When VREG 4.7V, 100% I 1.81 V Input voltage 1. VCTL 1. Design target value. When VREG 5.3V, 100% I 1.81 V Input voltage 1. VCTL 2. Design target value. When VREG 5.3V, 100% I 1.44 V Input voltage 2. VCTL 2. Design target value. When VREG 5.3V, 100% I 1.44 V Input voltage 2. VCTL 2. Design target value. When VREG 5.3V, 100% I 1.44 V Cottoge 2. VCTL 2. Design target value. When VREG 5.3V, 100% I 0.14 V Cottoge 2. VCTL 2. Design target value. When VREG 5.3V, 100% I 0.14 V Cottoge 2. VCTL 2. VCTL 2. VC 1.05 1.05	Common-mode input voltage range	VICM		0		VREG-1.7	V
Input voltage 2VCTL 2Output duly 0%1.35VInput voltage 1LVCTL 1LDesign target value. When VREG = 4.7V, 100%2.82VInput voltage 2LVCTL 2LDesign target value. When VREG = 5.47V, 06%1.29VInput voltage 2HVCTL 2HDesign target value. When VREG = 5.3V, 00%1.44VInput voltage 2HVCTL 2HDesign target value. When VREG = 5.3V, 00%1.44VInput voltage 2HVCTL 2HDesign target value. When VREG = 5.3V, 00%1.44VOutput saturation voltageVHPLIp = 10mA0.00.020.5VOutput saturation voltageVHPLIp = 10mA0.00.00.00.00.0Output saturation voltageVHPLVp = 18V0.00.00.00.00.00.0CBO scillator (CSD pin)VOL (CSD)VCSD = 2V3.152.251.185µALaw-level output voltageVOL (CSD)VCSD = 2V3.152.251.185µAExternal capacitor discharge currentICHG 1VCSD = 2V0.11.011.3VCharge discharge currentILCHG 1VCSD = 2V0.11.011.0µAExternal capacitor discharge currentILCHG 1VCSD = 2V0.11.011.04µACharge discharge currentILCHG 1VCSD = 2V0.11.011.011.04µAExternal capacitor discharge currentILCHG 1VC = 1.02VCSDVC	Input voltage 1	VCTL1	Output duty 100%		3.0		V
Input voltage 1. VCTL1L Design target value. 2.82 V Input voltage 2L VCTL2L Design target value. 1.29 V Input voltage 2L VCTL2L Design target value. 3.18 V Input voltage 1H VCTL2H Design target value. 3.18 V Input voltage 2H VCTL2H Design target value. 1.44 V Input voltage 2H VCTL2H Design target value. 1.44 V Output saturation voltage VIPPL IQ = 10mA 0.2 0.5 V Output saturation voltage VOHCSD 10 1.44 V V External capacitor (CSD pin) VIPL IQ = 10mA 0.2 0.5 V External capacitor charge current ICHG1 VCSD = 2V -3.15 -2.5 1.48 piA External capacitor charge current ICHG2 VCSD = 2V -3.15 -2.5 1.48 piA Chargedischarge current tatio RCSD Charge current //discharge current 1.6 1.0	Input voltage 2	VCTL2	Output duty 0%		1.35		V
Imput voltage 2L VCTL2L Design rarget value. 1.29 V Input voltage 1H VCTL1H Design rarget value. 1.29 V Input voltage 1H VCTL1H Design rarget value. 1.44 V Input voltage 2H VCTL2H Design rarget value. 1.44 V Input voltage 2H VCTL2H Design rarget value. 1.44 V Mem VRG 5 = 5.3V, 100% 1.44 V V HP pin V 0.02 0.5 V Output saturation voltage VHPL Vo = 18V 0.0 10 μ A CSD oscillator (CSD pin) 0.7 1.0 1.3 V Low-level output voltage Vo_U (CSD) 0.7 1.0 1.3 V External capacitor discharge current ICHG1 VCSD = 2V 0.1 0.14 0.18 μ A Chargedischarge current ratio RCSD Charge current /discharge current 15 18 2.1 Times RD jn 0.2 0.25	Input voltage 1L	VCTL1L	Design target value.		2.82		V
Input voltage 2. Vert2.t Design target value. When VREG = 4.7V, 0% Imput voltage 1H V Input voltage 1H VCTL1H Design target value. When VREG = 5.3V, 00% 3.18 V Input voltage 2H VCTL2H Design target value. When VREG = 5.3V, 0% 1.44 V P pin 0 0.2 0.5 V Output leakage current IHPleak Vg = 18V 0 10 μ A CSD oscillator (CSD pin) 0.7 3.0 3.3 V External capacitor charge current ICHG1 VCSD = 2V 0.7 1.0 1.3 V External capacitor charge current ICHG2 VCSD = 2V 0.1 0.14 0.18 μ A Charge discharge current value RCSD Charge current / discharge current / dis	Input veltage 2		When VREG = 4.7V, 100%		1 20		V
Input voltage 1H VCTL1H Design target value. When VREG = 5.3V, 100% 3.18 V Input voltage 2H VCTL2H Design target value. When VREG = 5.3V, 00% 1.44 V Input voltage 2H VCTL2H Design target value. When VREG = 5.3V, 00% 1.44 V Output saturation voltage VHPL Io = 10mA 0.2 0.5 V Output saturation voltage VHPL Io = 10mA 0.2 0.5 V CSD oscillator (CSD pin) 1.0 μ A V 2.7 3.0 3.3 V Low-level output voltage VOL (CSD) 0.7 1.0 1.3 V External capacitor charge current ICHG2 VCSD = 2V -3.15 -2.5 -1.85 μ A Charge/discharge current ratio RCSD Charge current //discharge current 108 μ A Charge/discharge current ratio RCSD V Output leakage current ratio μ A Charge/discharge current ratio μ A Charge/discharge current ratio μ A Charge/discharge current ratio μ A Charge/d	Input voltage 2L	VOIL2L	When VREG = $4.7V_{-}0\%$		1.29		v
Input voltage 2H VCTL2H Design target value. When VREG = 5.3V, 0% In.44 Int.44 HP pin Output saturation voltage VHPL $l_0 = 10mA$ 0.2 0.5 V Output saturation voltage VHPL $l_0 = 10mA$ 0.2 0.05 V Output leakage current IHPleak $V_0 = 18V$ 0 1.0 μ A CSD oscillator (CSD pin) 0.7 1.0 1.3 V Low-level output voltage V_{OL} (CSD) 0.7 1.0 1.3 V External capacitor charge current ICHG1 VCSD = 2V -3.15 -2.5 1.1.8 μ A Charge/discharge current ICHG2 VCSD = 2V -0.1 0.1 0.14 μ A Charge/discharge current ICHG2 VCSD = 2V -0.1 0.1 μ A Charge/discharge current ICHG2 VCSD = 2V -0.1 0.1 μ A Current limet circuit (RF pin) Low-level output voltage VRDL $l_0 = 10mA$ 0.2	Input voltage 1H	VCTL1H	Design target value.		3.18		V
Input voltage 2H VCTL2H Design target value. When VREG 5.3V, 0% 1.44 Iv V HP pin Output saturation voltage VHPL I ₀ = 10mA 0.2 0.5 V Output saturation voltage current IHPleak V ₀ = 18V 0.1 1.0 µA CSD occillator (CSD pin) 0.7 1.0 1.3 V External capacitor charge current ICHG1 VCSD = 2V -3.15 -2.5 -1.85 µA External capacitor discharge current ICHG2 VCSD = 2V -0.1 0.14 0.18 µA Charge/discharge current ichCHG1 VCSD = 2V -3.15 -2.5 -1.85 µA Charge/discharge current ichCHG2 VCSD = 2V -0.1 0.14 0.18 µA Charge/discharge current ichCB2 VCBC Corrent //discharge current /			When VREG = 5.3V, 100%				
P pin VHPL $l_{O} = 10mA$ 0.2 0.2 0.5 V Output saturation voltage VHPL $l_{O} = 10mA$ 0.2 0.5 V Output saturation voltage VHPL $V_{O} = 18V$ 0.1 100 μA CSD oscillator (CSD pin) 2.7 3.0 3.3 V Low-level output voltage V_{OL} (CSD) 0.7 1.0 1.3 V External capacitor discharge current ICHG1 VCSD $= 2V$ 0.1 0.14 0.18 μA Charge/discharge current in ICHG1 VCSD $= 2V$ 0.1 0.14 0.18 μA Charge/discharge current in ICHG1 VCSD $= 2V$ 0.1 0.14 0.18 μA Charge/discharge current in ICPG1 VCSD $= 2V$ 0.1 0.14 0.16 μA Charge/discharge current in ICPG1 VCD VCD VCD VCD VCD VO VO VO VO VO <	Input voltage 2H	VCTL2H	Design target value.		1.44		V
HP pin Output saturation voltage VHPL $l_0 = 10mA$ 0 0.2 0.5 V Output leakage current IHPleak $V_0 = 18V$ 0 10 μA CSD oscillator (CSD pin) 2.7 3.0 3.3 V Low-level output voltage V_{OL} (CSD) 0.7 1.0 1.3 V External capacitor charge current ICHG1 VCSD = 2V -3.15 -2.25 -1.85 μA Charge/discharge current ICHG2 VCSD = 2V -3.15 1.0 1.8 2.1 Times RD pin Charge/discharge current ratio RCS 0.1 0.1 0.2 0.5 V Uow-level output voltage VRDL $l_0 = 10mA$ 0.0 0.25 0.25 V Output leakage current IL (RD) V_0 = 18V 0.25 0.25 0.25 V Output leakage current imiter circuit (RF pin) Imiter voltage VIP Pin 10 10 pin Input frequency f			When VREG = 5.3V, 0%				
Output saturation voltage VHL IQ = 10mA 0.2 0.2 0.5 V Output leakage current IHPleak VQ = 18V In In μ A CSD oscillator (CSD pin) 2.7 3.0 3.3 V Low-level output voltage VQL (CSD) 0.7 1.0 1.1.3 V External capacitor charge current ICHG1 VCSD = 2V -3.15 -2.5 -1.85 μ A Charge/discharge current ICHG2 VCSD = 2V -0.1 0.14 0.18 μ A Charge/discharge current tatio RCSD Charge current //discharge current 115 18 2.1 Times RD pin Low-level output voltage VRDL Io_ = 10mA 0.2 0.5 V Output lakage current IL (RD) Vo_ = 18V 10 μ A Current limiter circuit (RF pin) Limiter voltage VIR (PI) 0.225 0.25 V PWMN pin Low-level input voltage VIL (PI) 0 </td <td>HP pin</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	HP pin						
Output leakage current IHPleak V _O = 18V Image contract Image contract <thimage cont<="" td=""><td>Output saturation voltage</td><td>VHPL</td><td>I_O = 10mA</td><td></td><td>0.2</td><td>0.5</td><td>V</td></thimage>	Output saturation voltage	VHPL	I _O = 10mA		0.2	0.5	V
CSD oscillator (CSD pin) Image: CSD oscillator (CSD pin) Image: CSD obscillator (CSD pin) Image: CSD obscillator (CSD pin) Image: CSD obscillator (CSD pin) Image: CSD pin) Low-level output voltage VOL (CSD VCSD = 2V 0.1 1.0 1.3 V External capacitor charge current ICHG1 VCSD = 2V 0.1 0.14 0.18 μ A Charge/discharge current ICHG2 VCSD = 2V 0.1 1.01 1.8 2.1 Times RD pin Image: CSD Charge current /discharge current 0.2 0.5 V Output leakage current IL (RD) VO = 18V Image: COSD 0.225 0.25 0.25 V PWMIN pin VIL VIP RF-GND 0.225 0.25 0.25 V Input requency f (PI) Image: CSD (CSD (PI) VIP VIP VIP VIP Input requency f (PI) Image: CSD (CSD (PI) VIP	Output leakage current	IHPleak	V _O = 18V			10	μΑ
High-level output voltage V_{OH} (CSD)2.73.03.3VLow-level output voltage V_{OL} (CSD)0.71.01.3VExternal capacitor charge currentICHG1VCSD = 2V-3.15-2.5-1.85 μ AExternal capacitor discharge currentICHG2VCSD = 2V0.10.140.18 μ ACharge/discharge current ratioRCSDCharge current /discharge current151821Times RD pin Low-level output voltageVRDL $I_O = 10mA$ 0.20.5VOutput leakage currentIL (RD) $V_O = 18V$ 0.250.250.275VCurrent limiter circuit (RF pin)RF-GND0.2250.250.275VPWMIN pinInput frequencyf (PI)RF-GND2.0VREGVVInput open voltage V_{IL} (PI)001.0VVInput open voltage V_{IL} (PI)VREG01.0VVHigh-level input current I_{IL} (PI)VPWIN = VREG1.0000 μ AFR pinVIL (FR)VPWIN = VREG1.001.0 μ AVInput open voltage V_{IL} (FR)Current01.0 μ AVHigh-level input current I_{IL} (PI)VPWIN = VREG1.0000 μ AFR pinHigh-level input current I_{IL} (FR)Current0.250.4V <t< td=""><td>CSD oscillator (CSD pin)</td><td></td><td></td><td></td><td>1</td><td></td><td></td></t<>	CSD oscillator (CSD pin)				1		
Low-level output voltage V_{OL} (CSD) 0.7 1.0 1.3 V External capacitor charge current ICHG1 VCSD = 2V -3.15 -2.5 -1.85 μ A External capacitor charge current ICHG2 VCSD = 2V 0.1 0.14 0.18 μ A Charge/discharge current ratio RCSD Charge current /discharge current 15 18 21 Times RD pin Low-level output voltage VRDL I_Q = 10mA 0.2 0.5 V Output leakage current IL (RD) V_Q = 18V 10 0 0.25 0.25 0.275 V Current limiter circuit (RF pin) Limiter voltage VIF RF-GND 0.225 0.25 0.275 V PWMIN pin Input frequency f (PI) Input frequency VIE (PI) VIE	High-level output voltage	V _{OH} (CSD)		2.7	3.0	3.3	V
External capacitor charge current ICHG1 VCSD = 2V -3.15 -2.5 -1.85 μ A External capacitor discharge current ICHG2 VCSD = 2V 0.1 0.14 0.18 μ A Charge/discharge current ratio RCSD Charge current/discharge current 15 18 21 Times RD pin 0.2 0.5 V Output leakage current IL (RD) V_O = 18V 0.2 0.2 0.5 V Output leakage current IL (RD) V_O = 18V 0.25 0.25 0.25 V Current limiter circuit (RF pin) Limiter voltage VRF RF-GND 0.25 0.25 0.25 V PWMIN pin 6.0 1.0 V	Low-level output voltage	V _{OL} (CSD)		0.7	1.0	1.3	V
External capacitor discharge current ICHG2 VCSD = 2V 0.1 0.14 0.18 μ A Charge/discharge current ratio RCSD Charge current /discharge current 15 18 21 Times RD pin 0.2 0.5 V Output leakage current IL (RD) V_O = 18V 0.2 0.2 0.5 V Output leakage current (RF pin) 0.25 0.25 0.27 V Imiter voltage VRF RF-GND 0.225 0.25 0.275 V PWMIN pin 50 kHz Input requency f (PI) 0.0 1.0 V Input open voltage V _{IL} (PI) 0.0 1.0 V Input open voltage V _{ID} (PI) 0.25 0.4 V High-level input voltage V _{IL} (PI) V V V V V V	External capacitor charge current	ICHG1	VCSD = 2V	-3.15	-2.5	-1.85	μΑ
Charge/discharge current ratio RCSD Charge current /discharge current 15 18 21 Times RD pin Low-level output voltage VRDL I_O = 10mA 0.2 0.5 V Output leakage current IL (RD) V_O = 18V 0 10 μ A Current limiter circuit (RF pin) 0.25 0.25 0.27 V PWMIN pin 0 10 YREG V	External capacitor discharge current	ICHG2	VCSD = 2V	0.1	0.14	0.18	μΑ
RD pin Low-level output voltage VRDL I_O = 10mA 0.0 0.0.2 0.0.5 V Output leakage current IL (RD) V _O = 18V 0 10 µA Current limiter circuit (RF pin) 0.225 0.25 0.25 V Limiter voltage VRF RF-GND 0.225 0.25 0.25 V PWMIN pin 0.225 0.25 0.275 V Input frequency f(PI) 2.0 VREG V Low-level input voltage VI _I (PI) 2.0 VREG V Input open voltage VI _I (PI) 0.2 0.25 0.4 V High-level input current I _{IH} (PI) VPWMIN = VREG 0.0 1.0 V High-level input current I _{IL} (PI) VPWMIN = VREG -10 0 1.0 µA Low-level input current I _{IL} (PI) VPWMIN = VREG -10 0 1.0 µA Low-level input	Charge/discharge current ratio	RCSD	Charge current /discharge current	15	18	21	Times
Low-level output voltage VRDL $I_O = 10mA$ Output leakage current 0.2 0.0 V Output leakage current IL (RD) $V_O = 18V$ Image construction 100 μA Current limiter circuit (RF pin) VRF RF-GND 0.225 0.25 0.275 V PWMIN pin 0.225 0.26 VRF V	RD pin						
Output leakage current IL (RD) $V_{O} = 18V$ Image 10 μA Current limiter circuit (RF pin) Imiter voltage VRF RF-GND 0.225 0.25 0.275 V PWMIN pin Input frequency f (Pl) Image 20 VRFG VRFG High-level input voltage VI _{II} (Pl) Image 2.0 VRFG VRFG Low-level input voltage VI _{II} (Pl) Image VIII VRFG VIIII VRFG VIIIII Input open voltage VI _{II} (Pl) Image VIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Low-level output voltage	VRDL	I _O = 10mA		0.2	0.5	V
Current limiter circuit (RF pin) Limiter voltage VRF RF-GND 0.225 0.25 0.275 V PWMIN pin Input frequency f (PI) Input second	Output leakage current	IL (RD)	V _O = 18V			10	μΑ
Limiter voltage VRF RF-GND 0.225 0.255 0.275 V PWMIN pin Input frequency f (P) Input frequency 0.250 0.250 0.275 VRE High-level input voltage f (P) Input frequency f (P) 0.200 0.200 VRE 0.2000 VRE $0.200000000000000000000000000000000000$	Current limiter circuit (RF pin)						
PWMIN pin Input frequency f (PI) Input optimized or state of the st	Limiter voltage	VRF	RF-GND	0.225	0.25	0.275	V
$\begin{array}{ c c c c c c } Input frequency & f(Pl) & & & & & & & & & & $	PWMIN pin						
High-level input voltage V_{IH} (PI) 2.0 VREG V Low-level input voltage V_{IL} (PI) 0 1.0 V Input open voltage V_{IO} (PI) VREG-0.5 VREG V Hysteresis V_{IS} (PI) 0.2 0.25 0.4 V High-level input current I_{IH} (PI) VPWMIN = VREG -10 0 10 μ A Low-level input current I_{IL} (PI) VPWMIN = 0V -130 -90 μ A High-level input current I_{IL} (PI) VPWMIN = 0V -130 -90 μ A Ecw-level input voltage V_{IL} (FR) 0 1.0 μ A High-level input voltage V_{IL} (FR) 2.0 VREG V Low-level input voltage V_{IL} (FR) 0 1.0 V Input open voltage V_{IL} (FR) 0.2 0.25 0.4 V Hysteresis V_{IS} (FR) 0.2 0.25 0.4 V High-	Input frequency	f (PI)				50	kHz
Low-level input voltage V _{IL} (PI) 0 1.0 V Input open voltage V _{IO} (PI) VREG-0.5 VREG V Hysteresis V _{IS} (PI) 0.2 0.25 0.4 V High-level input current I _{IH} (PI) VPWMIN = VREG -10 0 10 μA Low-level input current I _{IL} (PI) VPWMIN = 0V -130 -90 μA F/R pin -90 1.0 V High-level input voltage V _{IH} (FR) 2.0 VREG V Low-level input voltage V _{IH} (FR) 0 1.0 V High-level input voltage V _{IH} (FR) 2.0 VREG V Low-level input voltage V _{IL} (FR) 0 1.0 V Input open voltage V _{IL} (FR) 0.2 0.25 0.4 V Hysteresis V _{IS} (FR) 0.2 0.25 0.4 V High-level input current I _{IH} (FR) -10 0 10	High-level input voltage	V _{IH} (PI)		2.0		VREG	V
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Low-level input voltage	V _{IL} (PI)		0		1.0	V
Hysteresis VIS (PI) 0.2 0.25 0.4 V High-level input current IIH (PI) VPWMIN = VREG -10 0 10 μ A Low-level input current IIL (PI) VPWMIN = 0V -130 -90 μ A F/R pin F/R pin 2.0 VREG V Low-level input voltage VIL (FR) 0 1.0 V Input open voltage VIL (FR) 0 1.0 V Hysteresis VIO (FR) VREG V V V High-level input current IIH (FR) 0.2 0.25 0.4 V	Input open voltage	V _{IO} (PI)		VREG-0.5		VREG	V
High-level input currentIIH (PI)VPWMIN = VREG-10010 μ ALow-level input currentIIL (PI)VPWMIN = 0V-130-90 μ AF/R pinHigh-level input voltageVIH (FR)2.0VREGVLow-level input voltageVIL (FR)01.0VInput open voltageVIO (FR)VREGVVREGVHysteresisVIS (FR)0.20.250.4VHigh-level input currentIIH (FR)01010 μ A	Hysteresis	V _{IS} (PI)		0.2	0.25	0.4	V
Low-level input currentIIL (PI)VPWMIN = 0V-130-90 μ AF/R pinHigh-level input voltageVIH (FR)2.0VREGVLow-level input voltageVIL (FR)01.0VInput open voltageVIO (FR)VREGVREGVHysteresisVIS (FR)0.20.250.4VHigh-level input currentIIH (FR)-10010 μ A	High-level input current	I _{IH} (PI)	VPWMIN = VREG	-10	0	10	μA
F/R pin Low-level input voltage V _{IH} (FR) 2.0 VREG V Low-level input voltage V _{IL} (FR) 0 1.0 V Input open voltage V _{IO} (FR) VREG-0.5 VREG V Hysteresis V _{IS} (FR) 0.2 0.25 0.4 V High-level input current I _{IH} (FR) -10 0 10 μA	Low-level input current	I _{IL} (PI)	VPWMIN = 0V	-130	-90		μA
High-level input voltage V _{IH} (FR) 2.0 VREG V Low-level input voltage V _{IL} (FR) 0 1.0 V Input open voltage V _{IO} (FR) VREG-0.5 VREG V Hysteresis V _{IS} (FR) 0.2 0.25 0.4 V High-level input current I _{IH} (FR) -10 0 10 μA	F/R pin	_1				1	
Low-level input voltage V _{IL} (FR) 0 1.0 V Input open voltage V _{IO} (FR) VREG-0.5 VREG V Hysteresis V _{IS} (FR) 0.2 0.25 0.4 V High-level input current I _{IH} (FR) -10 0 10 μA	High-level input voltage	V _{IH} (FR)		2.0		VREG	V
Input open voltage VIO (FR) VREG-0.5 VREG V Hysteresis VIS (FR) 0.2 0.25 0.4 V High-level input current II _H (FR) -10 0 10 µA	Low-level input voltage	V _{IL} (FR)		0		1.0	V
Hysteresis V _{IS} (FR) 0.2 0.25 0.4 V High-level input current I _{IH} (FR) -10 0 10 μA	Input open voltage	VIO (FR)		VREG-0.5		VREG	V
High-level input current II _H (FR) -10 0 10 μA	Hysteresis	V _{IS} (FR)		0.2	0.25	0.4	V
	High-level input current	I _{IH} (FR)		-10	0	10	μA
Low-level input current I _{IL} (FR) -130 -90 μA	Low-level input current	I _{IL} (FR)		-130	-90		μA
N1 pin							
High-level input voltage V _{IH} (N1) 2.0 VREG V							
Low-level input voltage VII (N1) 0 1.0 V	Low-level input voltage	VII (N1)		0		1.0	V
Input open voltage VIO (N1) VREG-0.5 VREG V	Input open voltage			VREG-0.5		VREG	V
High-level input current Image: Note of the second se	High-level input current		VN1 = VREG	-10	0	10	цА
Low-level input current III (N1) VN1 = 0V -130 -100 IIIA	Low-level input current	lμ (N1)	VN1 = 0V	-130	-100		μA

Package Dimensions

unit : mm (typ) 3260A



Pin Assignment



• Three-Phase Logic Truth	Table ($IN = "H"$ indicates	the state where $IN^+ > IN^-$)
Thee Thuse Bogle Hude	1 fuble (11) = 11 mateutes	the state where $\mathbf{n} \neq \mathbf{n} \neq \mathbf{n}$

	F/R = "L"		F/R="H"			Output		
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	
1	Н	L	Н	L	Н	L	VH	UL
2	Н	L	L	L	Н	Н	WH	UL
3	Н	Н	L	L	L	Н	WH	VL
4	L	Н	L	Н	L	Н	UH	VL
5	L	Н	Н	Н	L	L	UH	WL
6	L	L	Н	Н	Н	L	VH	WL

• PWMIN pin

Input state	State
High or open	Output off
Low	Output on

If the PWM pin is not used, the input must be held at the low level.

• <u>N1</u> pin

Input state	HP output
High or open	Three Hall sensor synthesized output
Low	Single Hall sensor output

Pin Functions

Pin No.	Pin	Description
1	GND	Ground
2	RF	Output current detection. The current detection resistor (Rf) voltage is sensed by the RF pin to implement current detection.
		The maximum output current is set by RF to be IOUT = 0.25/Rf.
7	UH	Outputs (PWM outputs).
5	VH	These are push-pull outputs.
3	WH	
8	UL	Outputs
6	VL	These are push-pull outputs.
4	WL	
10, 9	IN1+, IN1-	Hall sensor inputs from each motor phase.
12, 11	IN2+, IN2-	The logic high state indicates that $IN^+ > IN^-$.
14, 13	IN3+, IN3 ⁻	If inputs are provided by a Hall effect sensor IC, the common-mode input range is expanded by biasing either the + or -
		input.
15	PWM	Functions as both the PWM oscillator frequency setting pin and the initial reset pulse setting pin. Connect a capacitor
		between this pin and ground.
16	RD	Lock (motor constrained) detection state output. This output is turned on when the motor is turning and off when the lock
		protection function detects that the motor has been stopped. This is an open collector output.
17	CSD	Sets the operating time for the lock protection circuit.
		Connect a capacitor between this pin and ground. Connect this pin to ground if the lock protection function is not used.
18	PWMIN	PWM pulse signal input. The output goes to the drive state when this pin is low, and to the off state when this pin is high
		or open. To use this pin for control, a CTL amplifier input such that the TOC pin voltage goes to the 100% duty state
		must be provided.
19	F/R	Forward/reverse control input
20	HP	Hall signal output (HP output). This provides either a single Hall sensor output or a synthesized 3-sensor output.
21	N1	Hall signal output (HP output) selection
22	El+	CTL amplifier + (noninverting) input. The PWMIN pin must be held at the low level to use this input for motor control
23	VREG	5V regulator output (Used as the control circuit power supply. A low-voltage protection circuit is built in.)
		Connect a capacitor between this pin and ground for stabilization.
24	Vcc	Power supply. Connect a capacitor between this pin and ground to prevent noise and other disturbances from affecting
		this IC.

Hall Sensor Signal Input/Output Timing Chart



Block Diagram and Application Example 1

Bipolar transistor drive (high side PWM) using a 5V power supply



Application Example 2

54 MOS transistor drive (low side PWM) using a 12V single-voltage power supply



Application Example 3

MOS transistor drive (low side PWM)

using a $V_{CC} = 12V$, VM = 24V power supply system



Application Example 4

MOS transistor drive (low side PWM) using a 24V single-voltage power supply



LB11620T Functional Description

1. Output Drive Circuit

The LB11620T adopts direct PWM drive to minimize power loss in the outputs. The output transistors are always saturated when on, and the motor drive power is adjusted by changing the on duty of the output. The output PWM switching is performed on the UH, VH, and WH outputs. Since the UL to WL and UH to WH outputs have the same output form, applications can select either low side PWM or high side PWM drive by changing the way the external output transistors are connected. Since the reverse recovery time of the diodes connected to the non-PWM side of the outputs is a problem, these devices must be selected with care. (This is because through currents will flow at the instant the PWM side transistors turn on if diodes with a short reverse recovery time are not used.)

2. Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation I = VFR/Rf (VRF = 0.25V typical, Rf: current detection resistor). This circuit suppresses the output current by reducing the output on duty.



The current limiter circuit includes an internal filter circuit to prevent incorrect current limiter circuit operation due to detecting the output diode

reverse recovery current due to PWM operation. Although there should be no problems with the internal filter circuit in normal applications, applications should add an external filter circuit (such as an RC low-pass filter) if incorrect operation occurs (if the diode reverse recovery current flows for longer than 1µs).

3. Notes on the PWM Frequency

The PWM frequency is determined by the capacitor C (F) connected to the PWM pin.

 $f_{PWM} \approx 1/(22500 \times C)$

If a 2000pF capacitor is used, the circuit will oscillate at about 22kHz. If the PWM frequency is too low, switching noise will be audible from the motor, and if it is too high, the output power loss will increase. Thus a frequency in the range 15k to 50kHz must be used. The capacitor's ground terminal must be placed as close as possible to the IC's ground pin to minimize the influence of output noise and other noise sources.

4. Control Methods

The output duty can be controlled by either of the following methods

 \cdot Control based on comparing the EI+ pin voltage to the PWM oscillator waveform

The low side output transistor duty is determined according to the result of comparing the EI+ pin voltage to the PWM oscillator waveform. When the EI+ pin voltage is 1.35V or lower, the duty will be 0%, and when it is 3.0V or higher, the duty will be 100%.

When EI+ pin voltage control is used, a low-level input must be applied to the PWMIN pin or that pin connected to ground.

• Pulse Control Using the PWMIN Pin

A pulse signal can be input to the PWMIN pin, and the output can be controlled based on the duty of that signal. Note that the output is on when a low level is input to the PWMIN pin, and off when a high level is input. When the

PWMIN pin is open it goes to the high level and the output is turned off. If inverted input logic is required, this can be implemented with an external

transistor (npn).

When controlling motor operation from the PWMIN pin, the EI+ pin must be connected to the VREG pin.

Note that since the PWM oscillator is also used as the clock for internal circuits, a capacitor (about 2000pF) must be connected to the PWM pin even if the PWMIN pin is used for motor control.



5. Hall Input Signals

A signal input with an amplitude in excess of the hysteresis (80mV maximum) is required for the Hall inputs. Considering the possibility of noise and phase displacement, an even larger amplitude is desirable.

If disruptions to the output waveforms (during phase switching) or to the HP output (Hall signal output) occur due to noise, this must be prevented by inserting capacitors across the inputs. The constraint protection circuit uses the Hall inputs to discriminate the motor constraint state. Although the circuit is designed to tolerate a certain amount of noise, care is required when using the constraint protection circuit.

If all three phases of the Hall input signal system go to the same input state, the outputs are all set to the off state (the UL, VL, WL, UH, VH, and WH outputs all go to the low level).

If the outputs from a Hall IC are used, fixing one side of the inputs (either the + or - side) at a voltage within the common-mode input voltage range allows the other input side to be used as an input over the 0V to V_{CC} range.

6. Under-voltage Protection Circuit

The under-voltage protection circuit turns one side of the outputs (UH, VH, and WH) off when the VREG pin voltage falls below the minimum operation voltage (see the Electrical Characteristics). To prevent this circuit from repeatedly turning the outputs on and off in the vicinity of the protection operating voltage, this circuit is designed with hysteresis. Thus the output will not recover until the operating voltage rises 0.5V (typical).

7. Constraint Protection Circuit

When the motor is physically constrained (held stopped), the CSD pin external capacitor is charged (to about 3.0 V) by a constant current of about 2.25μ A and is then discharged (to about 1.0V) by a constant current of about 0.15μ A. This process is repeated, generating a saw-tooth waveform. The constraint protection circuit turns motor drive on and off repeatedly based on this saw-tooth waveform. (The UH, VH, and WH side outputs are turned on and off.) Motor drive is on during the period the CSD pin external capacitor is being charged from about 1.0V to about 3.0V, and motor drive is off during the period the CSD pin external capacitor is being discharged from about 3.0V to about 1.0V. The IC and the motor are protected by this repeated drive on/off operation when the motor is physically constrained.

The motor drive on and off times are determined by the value of the connected capacitor C (in μ F).

TCSD1 (drive on period) $\approx 0.89 \times C$ (seconds)

TCSD2 (drive off period) $\approx 13.3 \times C$ (seconds)

When a 0.47μ F capacitor is connected externally to the CSD pin, this iterated operation will have a drive on period of about 0.4 seconds and a drive off period of about 6.3 seconds.

While the motor is turning, the discharge pulse signal (generated once for each Hall input period) that is created by combining the Hall inputs internally in the IC discharges the CSD pin external capacitor. Since the CSD pin voltage does not rise, the constraint protection circuit does not operate.

When the motor is physically constrained, the Hall inputs do not change and the discharge pulses are not generated. As a result, the CSD pin external capacitor is charged by a constant current of 2.5μ A to about 3.0V, at which point the constraint protection circuit operates. When the constraint on the motor is released, the constraint protection function is released.

Connect the CSD pin to ground if the constraint protection circuit is not used.

8. Forward/Reverse Direction Switching

This IC is designed so that through currents (due to the output transistor off delay time when switching) do not flow in the output when switching directions when the motor is turning. However, if the direction is switched when the motor is turning, current levels in excess of the current limiter value may flow in the output transistors due to the motor coil resistance and the motor back EMF state when switching. Therefore, designers must consider selecting external output transistors that are not destroyed by those current levels or only switching directions after the speed has fallen below a certain speed.

9. Handling Different Power Supply Types

When this IC is operated from an externally supplied 5V power supply (4.5 to 5.5V), short the V_{CC} pin to the VREG pin and connect them to the external power supply.

When this IC is operated from an externally supplied 12V power supply (8 to 17 V), connect the V_{CC} pin to the power supply. (The VREG pin will generate a 5V level to function as the control circuit power supply.)

11. Power Supply Stabilization

Since this IC uses a switching drive technique, the power supply line level can be disturbed easily. Therefore capacitors with adequate capacitance to stabilize the power supply line must be inserted between V_{CC} and ground. If diodes are inserted in the power supply lines to prevent destruction if the power supply is connected with reverse polarity, the power supply lines are even more easily disrupted, and even larger capacitors are required. If the power supply is turned on and off by a switch, and if there is a significant distance between that switch and the stabilization capacitor, the supply voltage can be disrupted significantly by the line inductance and surge current into the capacitor. As a result, the withstand voltage of the device may be exceeded. In application such as this, the surge current must be suppressed and the voltage rise prevented by not using ceramic capacitors with a low series impedance, and by using electrolytic capacitors instead.

12. VREG Stabilization

To stabilize the VREG voltage, which is the control circuit power supply, a 0.1μ F or larger capacitor must be inserted between the VREG pin and ground. The ground side of this capacitor must connected to the IC ground pin with a line that is as short as possible.

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellctual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of October, 2008. Specifications and information herein are subject to change without notice.