LB11850VA

Single-phase Full-wave Pre-driver with Speed Control Function for Fan Motor

Monolithic Digital IC

Overview

The LB11850VA is a single-phase bipolar fan motor driver with speed control function that works with a speed feedback signal. A highly efficient, quiet and low power consumption motor driver circuit, with a high speed accuracy and large variable speed can be implemented by adding a small number of external components.

This pre-driver is optimal for driving large scale fan motors (with large air volume and large current) such as those used in servers and consumer products.

Functions and Features

- Pre-driver for Single-phase Full-wave Drive
  - PMOS-NMOS is Used as an External Power TR, Enabling High-efficiency and Low-power-consumption Drive by Means of the Low-saturation Output and Single-phase Full-wave Drive
- On-chip Speed Control Circuit
  - The Speed Control (Closed Loop Control) Using a Speed Feedback Signal Makes it Possible to Achieve Higher Speed Accuracy and Lower Speed Fluctuations when Supply Voltage Fluctuates or Load Fluctuates, Compared with an Open-loop Control System. Separately Excited Upper Direct PWM Control Method is Used as the Variable-speed Control System
- External PWM Input or Analog Voltage Input Enabling Variable Speed Control
  - The Speed Control Input Signal is Compatible with PWM Duty Ratio or Analog Voltages
- On-chip Soft Start Circuit
- Lowest Speed Setting Pin
  - The Lowest Speed can be Set with the External Resistor
- Current Limiter Circuit Incorporated
  - Chopper Type Current Limit at Start or Lock
- Reactive Current Cut Circuit Incorporated
  - Reactive Current before Phase Change is Cut to Enable Silent and Low-consumption Drive
- Constraint Protection and Automatic Reset Functions Incorporated
- FG (Speed Detection), RD (Lock Detection) Output
- Constant-voltage Output Pin for Hall Bias

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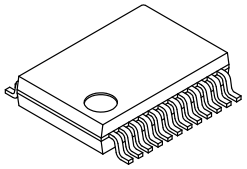

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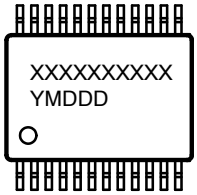
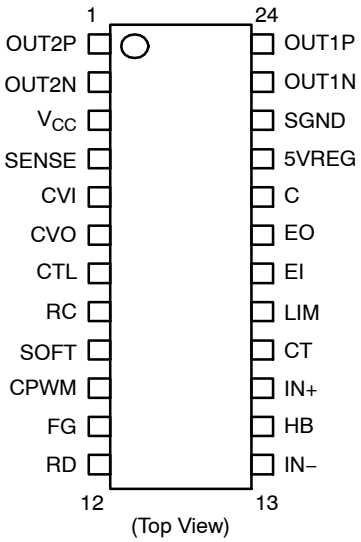
MARKING DIAGRAM



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC} max	V_{CC} Maximum Supply Voltage		18	V
I_{OUT}N max	OUTN Pin Maximum Output Current		20	mA
I_{OUT}P max	OUTP Pin Maximum Sink Current		20	mA
V_{OUT} max	OUT Pin Output Withstand Voltage		18	V
HB	HB Maximum Output Current		10	mA
CTL, C max	CTL, C Pin Withstand Voltage		7	V
CVI, LIM max	CVI, LIM Pin Withstand Voltage		7	V
FG max	RD/FD Output Pin Output Withstand Voltage		19	V
	RD/FG Output Current		10	mA
I5VREG max	5VREG Pin Maximum Output Current		10	mA
P_d max	Allowable Power Dissipation	Mounted on a specified board (Notes 1, 2)	0.9	W
T_{opr}	Operating Temperature Range		−30 to +95	°C
T_{stg}	Storage Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on a specified board: 114.3 mm × 76.1 mm × 1.6 mm, glass epoxy.
2. T_j max = 150°C. Use the device in a condition that the chip temperature does not exceed T_j = 150°C during operation.

RECOMMENDED OPERATING RANGES (T_A = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}1	V_{CC} Supply Voltage 1	V_{CC} pin	5.5 to 16	V
V_{CC}2	V_{CC} Supply Voltage 2	When V_{CC} − 5VREG shorted	4.5 to 5.5	V
VCTL	CTL Input Voltage Range		0 to 5VREG	V
VLIM	LIM Input Voltage Range		0 to 5VREG	V
VCVI	VCI Input Voltage Range		0 to 5VREG	V
VICM	Hall Input Common Phase Input Voltage Range		0.2 to 3	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}1	Circuit Current	During drive		12	15	mA
I_{CC}2		During lock protection		12	15	mA
5VREG	5VREG Voltage	I5VREG = 5 mA	4.8	5.0	5.2	V
VHB	HB Voltage	IHB = 5 mA	1.05	1.20	1.35	V
VLIM	Current Limiter Voltage		190	210	230	mV
VCRH	CPWM Pin H Level Voltage		2.8	3.0	3.2	V
VCRL	CPWM Pin L level Voltage		0.9	1.1	1.3	V
ICPWM1	CPWM Pin Charge Current	VCPWM = 0.5 V	24	30	36	μA
ICPWM2	CPWM Pin Discharge Current	VCPWM = 3.5 V	21	27	33	μA
FPWM	CPWM Oscillation Frequency	C = 220 pF		30		kHz

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V, unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCTH	CT Pin H Level Voltage		2.8	3.0	3.2	V
VCTL	CT Pin L Level Voltage		0.9	1.1	1.3	V
ICT1	CT Pin Charge Current	VCT = 2 V	1.6	2.0	2.5	μA
ICT2	CT Pin Discharge Current	VCT = 2 V	0.16	0.20	0.25	μA
RCT	CT Pin Charge/Discharge Current Ratio	ICT1/ICT2	8	10	12	times
VONH	OUTN Pin Output H Voltage	I_O = 10 mA	–	V_{CC}–0.85	V_{CC}–1.0	V
VONL	OUTN Pin Output L Voltage	I_O = 10 mA	–	0.9	1.0	V
VOPL	OUTP Pin Output L Voltage	I_O = 10 mA	–	0.5	0.65	V
VHN	Hall Input Sensitivity	IN+, IN− difference voltage (including offset and hysteresis)	–	±15	±25	mV
VFGL	FG Output L Voltage	IFG = 5 mA	–	0.15	030	μA
IFGL	FG Pin Leak Current	VFG = 19 V	–	–	30	μA
VRDL	RD Output L Voltage	IRD = 5 mA	–	0.15	0.30	V
IRDL	RD Pin Leak Current	VRD = 19 V	–	–	30	μA
VEOH	EO Pin Output H Voltage	IEO1 = −0.2 mA	VREG−1.2	VREG−0.8	–	V
VEOL	EO Pin Output L Voltage	IEO1 = 0.2 mA	–	0.8	1.1	V
VRCH	RC Pin Output H Voltage		3.2	3.45	3.7	V
VRCL	RC Pin Output L Voltage		0.7	0.8	1.05	V
VRCCLP	RC Pin Clamp Voltage		1.3	1.5	1.7	V
VCTLH	CTL Pin Input H Voltage		2.0	–	VREG	V
VCTLL	CTL Pin Input L Voltage		0	–	1.0	V
VCTLO	CTL Pin Input Open Voltage		VREG−0.5	–	VREG	V
ICTLH	CTL Pin H Input H Current	VFGIN = 5VREG	−10	0	10	μA
ICTLL	CTL Pin L Input L Current	VFGIN = 0 V	−120	−90	–	μA
VCH	C Pin Output H Voltage		VREG−0.3	VREG−0.1	–	V
VCL	C Pin Output L Voltage		1.8	2.0	2.2	V
IBLIM	LIM Pin Input Bias Current		−1	–	1	μA
VILIM	LIM Pin Common Phase Input Voltage Range		2.0	–	VREG	V
ICSOFT	SOFT Pin Charge Current		1.0	1.3	1.6	μA
VISOFT	SOFT Pin Operating Voltage Range		2.0	–	VREG	V
IB(VCI)	CVI Pin Input Bias Current		−1	–	2	μA
VIVCI	CVI Pin Common Phase Input Voltage Range		2.0	–	VREG	V
V_{OH}(VCO)	CVO Pin Output H Level Voltage		VREG−0.35	VREG−0.2	–	V
V_{OL}(VCO)	Output L Level Voltage		1.8	2.0	2.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Design target value and si not measured.

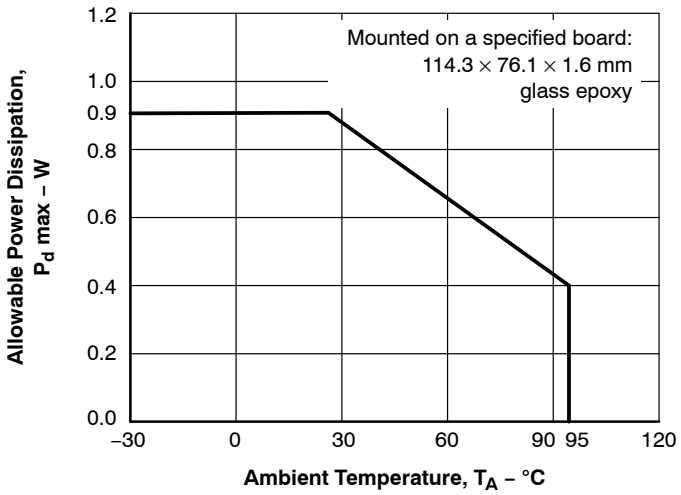


Figure 1. P_d max – T_A

TRUTH TABLE – LOCK PROTECTION CPWM = H

IN–	IN+	CT	OUT1P	OUT1N	OUT2P	OUT2N	FG	Mode
H	L	L	L	L	OFF	H	L	OUT1 → 2 drive
L	H		OFF	H	L	L	OFF	OUT2 → 1 drive
H	L	H	OFF	L	OFF	H	L	Lock protection
L	H		OFF	H	OFF	L	OFF	

TRUTH TABLE – SPEED CONTROL CT = L

EO	CPWM	IN–	IN+	OUT1P	OUT1N	OUT2P	OUT2N	Mode
L	H	H	L	L	L	OFF	H	OUT1 → 2 drive
		L	H	OFF	H	L	L	OUT2 → 1 drive
H	L	H	L	OFF	L	OFF	H	Regeneration mode
		L	H	OFF	H	OFF	L	

BLOCK DIAGRAM

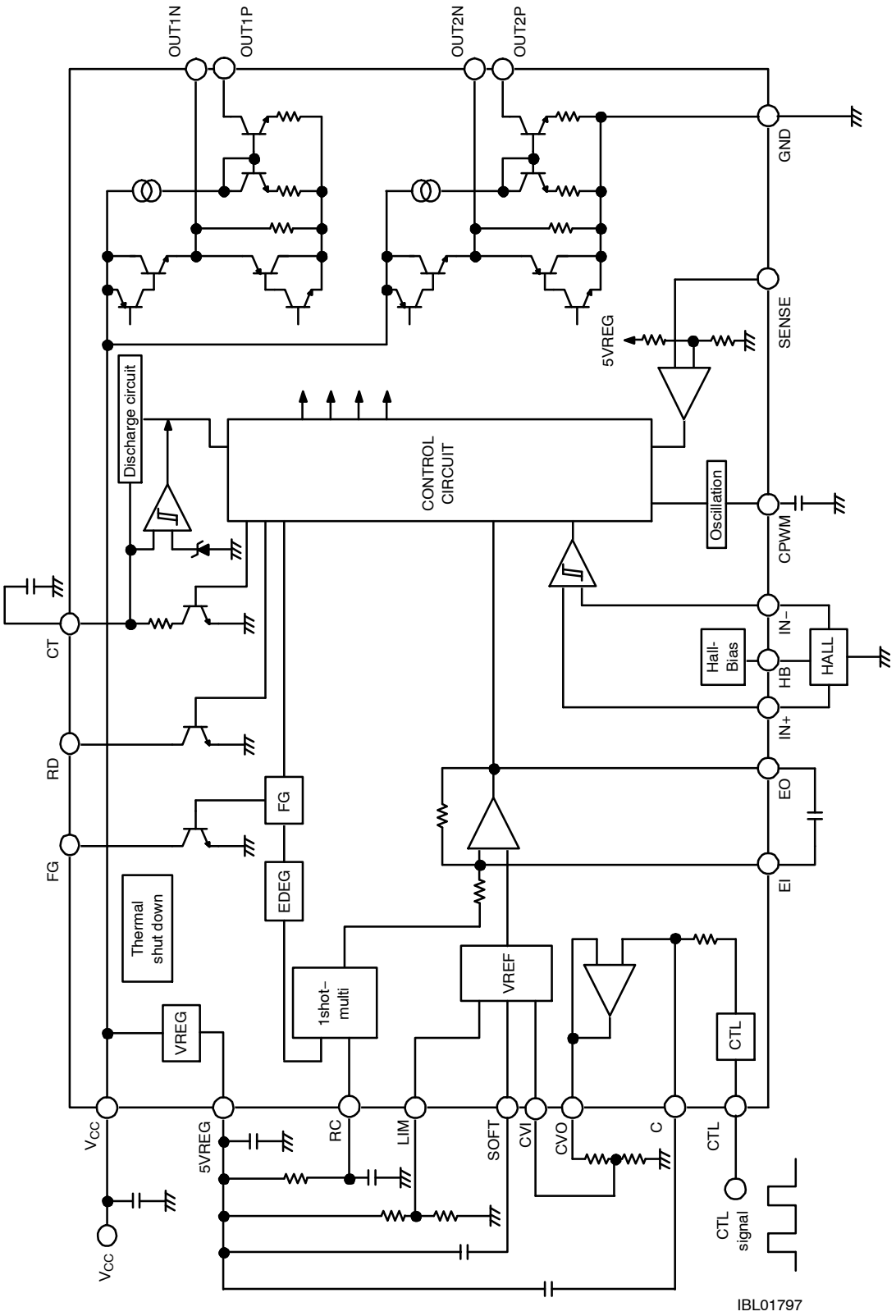


Figure 2. Block Diagram

APPLICATION CIRCUIT

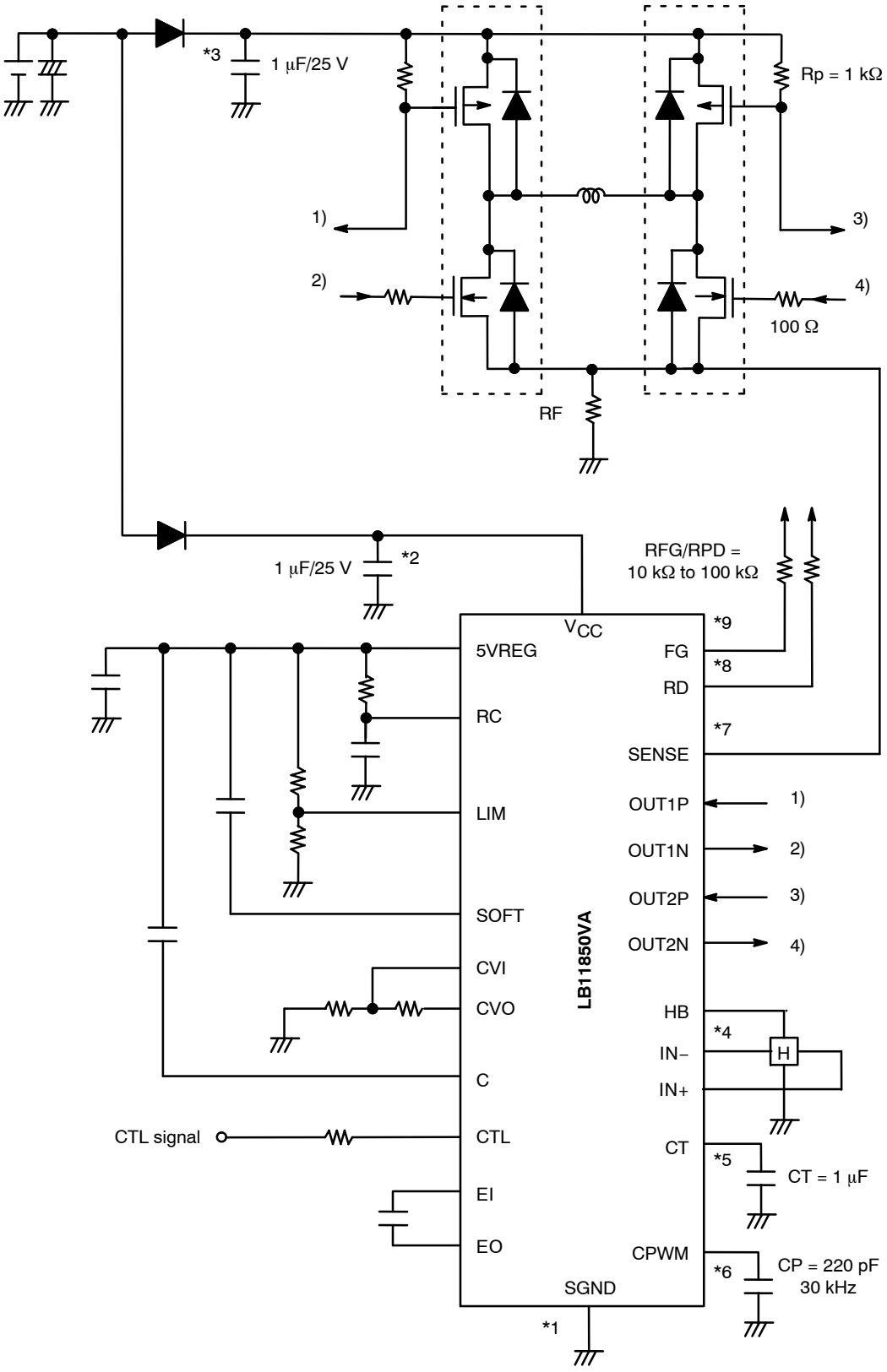


Figure 3. Sample Application Circuit

DESCRIPTION OF PRE-DRIVER BLOCK

*1: <Power Supply-GND Wiring>
SGND is connected to the control circuit power supply system.

*2: <Power Stabilization Capacitor>
For the signal-side power stabilization capacitor, the capacitance of more than 0.1 μF is used.
Connect the capacitor between V_{CC} and GND with the thick pattern and along the shortest route.

*3: <Power-side Power Stabilization Capacitor>
For the power-side power stabilization capacitor, the capacitance of more than 0.1 μF is used.
Connect the capacitor between power-side power supply and GND with the thick pattern and along the shortest route.

*4: <IN^+, IN^- Pins>
Hall signal input pins.
Wiring needs to be short to prevent carrying noise. If noise is carried, insert a capacitor between IN^+ and IN^-. The Hall input circuit is a comparator having a hysteresis of 15 mV.
It has a ±30 mV (input signal difference voltage) soft switch zone.
It is recommended that the Hall input level is 100 mV (p−p) at the minimum.

*5: <CPWM Pin>
This is the pin to connect capacitor for generating the PWM basic frequency.
Use of CP = 220 pF produces oscillation at the frequency of 30 kHz which serves as the PWM basic frequency.
Since this pin is also used for the current limiter reset signal, the capacitor must be connected without fail even when no speed control is implemented.

*6: <CT Pin>
This is the pin to connect capacitor for lock detection.
Constant-current charging and constant-current discharging circuits are incorporated. When the pin voltage becomes 3.0 V, the safety lock is applied, and when it lowers to 1.0 V, the lock protection is reset.
Connect this pin to GND when it is not in use (when lock protection is not required).

*7: <SENSE Pin>
This is the pin for current limiter detection.
When the pin voltage exceeds 0.21 V, current limiting is applied, and the low-side regeneration mode is established.
Connect this pin to GND when it is not in use.

*8: <RD Pin>
Lock detection pin.
This is the open collector output, which outputs “L” during rotation and “H” at stop. This pin is left open when it is not in use.

*9: <FG Pin>
Speed detection pin.
This is the open collector output, which can detect the rotation speed using the FG output according to the phase change. This pin is left open when it is not in use.

DESCRIPTION OF SPEED CONTROL BLOCK

1. Speed Control Diagram

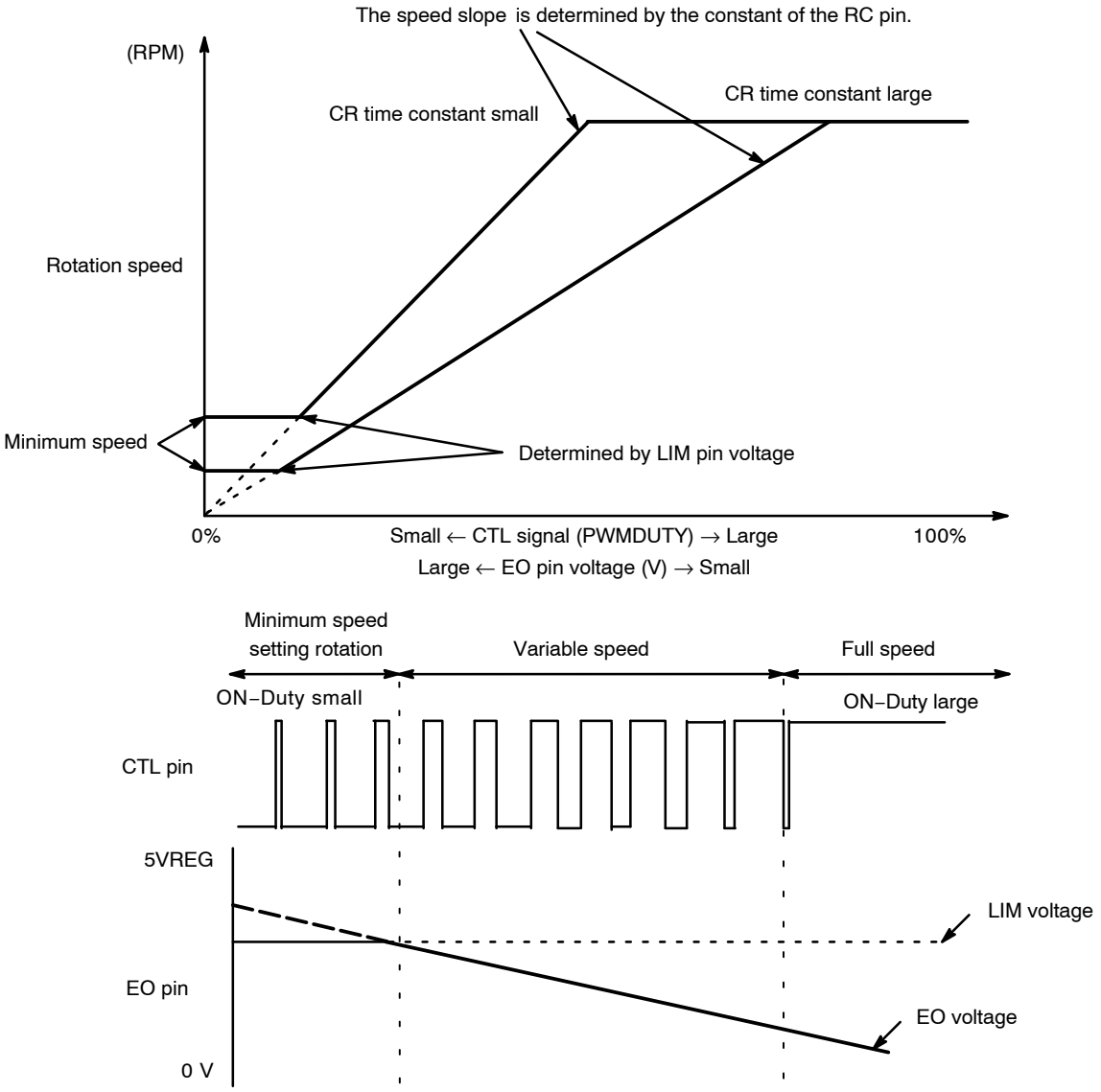


Figure 4. Speed Control Diagram

2. Timing at Startup (Soft Start)

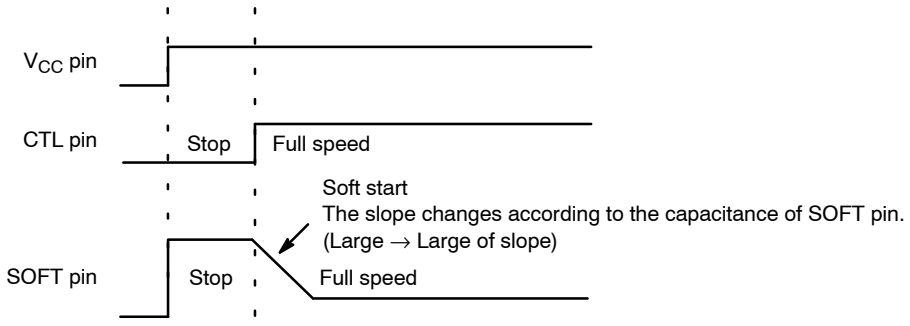


Figure 5. Timing at Startup (Soft Start)

3. Additional Description of Operations:
   The LB11850 forms a feedback loop inside the IC so that the FG period (motor speed) corresponding to the control voltage is established by inputting the duty pulse.

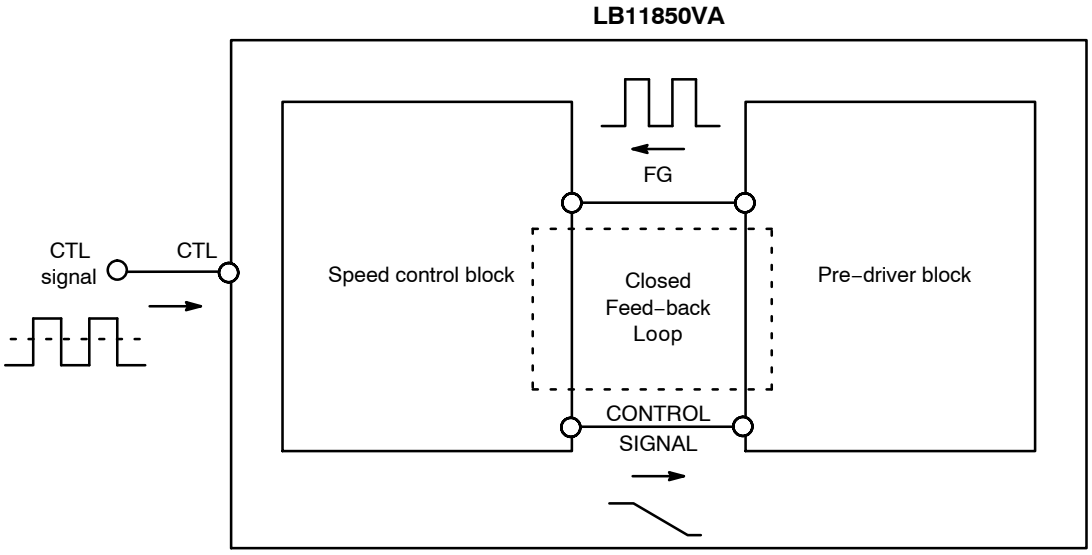


Figure 6. Additional Description of Operations

The operation inside the IC is as follows. Pulse signals are created from the edges of the FG signals as shown in the figure below, and a waveform with a pulse width which is determined by the CR time constants and which uses these edges as a reference is generated by a one-shot multivibrator.

These pulse waveforms are integrated and the duty ratio of the pre-driver output is controlled as a control voltage.

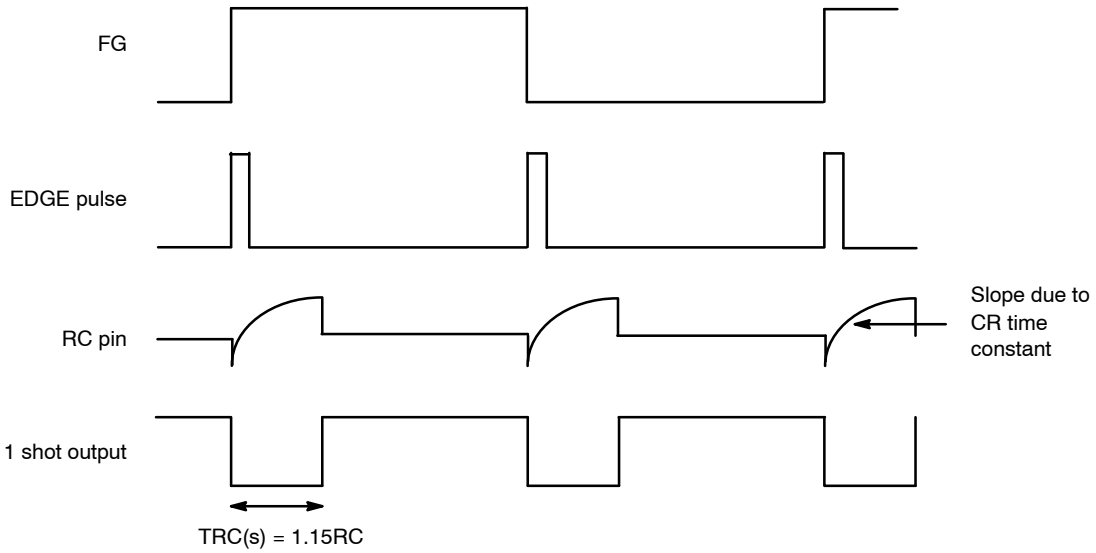


Figure 7. Pulse Waveforms

Furthermore, by changing the pulse width as determined by the CR time constant, the VCTL versus speed slope can be changed as shown in the speed control diagram of the previous section.

However, since the pulses used are determined by the CR time constant, the variations in CR are output as-is as the speed control error.

4. Procedure for Calculating Constants:
<RC Pin>
The slope shown in the speed control diagram is determined by the constant of the RC pin.

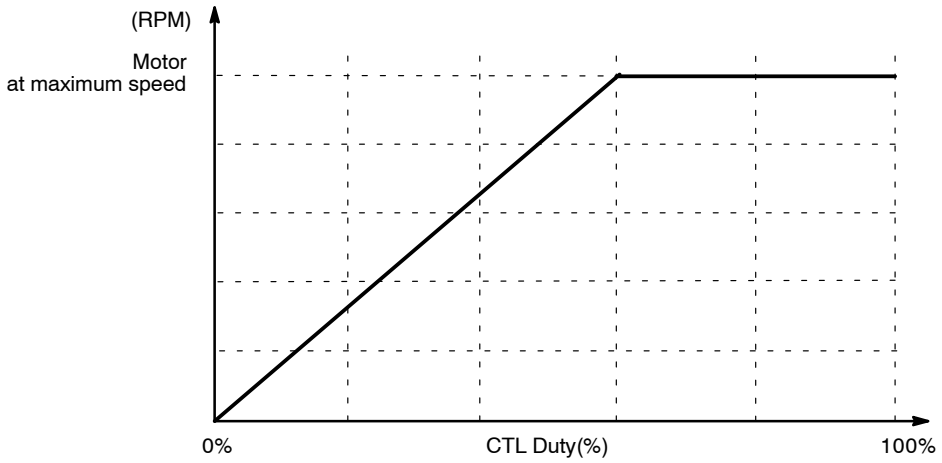


Figure 8.

1) Obtain FG signal frequency f_{FG} (Hz) of the maximum speed of the motor.
(With FG2 pulses per rotation)
f_{FG} (Hz) = 2 rpm / 60 .... <1>
2) Obtain the time constant which is connected to the RC pin.
(Have "DUTY" (example: 100% = 1.0, 60% = 0.6) serve as the CTL duty ratio at which the maximum speed is to be obtained.)
$R \times C = DUTY / (3.3 \times 1.1 \times f_{FG})$ .... <2>
3) Obtain the resistance and capacitance of the capacitor.
Based on the discharge capacity of the RC pin, the capacitance of the capacitor which can be used is 0.01 to 0.015 μF. Therefore, find the appropriate resistance using equation <3> or <4> below from the result of <2> above.
$R = (R \times C) / 0.01$ μF .... <3>
$R = (R \times C) / 0.015$ μF .... <4>

The temperature characteristics of the curve are determined by the temperature characteristics of the capacitor of the RC pin. When temperature-caused fluctuations in the speed are to be minimized, use a capacitor with good temperature characteristics.

<CVO, CVI Pins>
These pins determine the position of the slope origin. (When the origin point is at (0%, 0 rpm), CVO and CVI are shorted.)
1) Movement along the X-axis (resistance divided between CVO and GND)

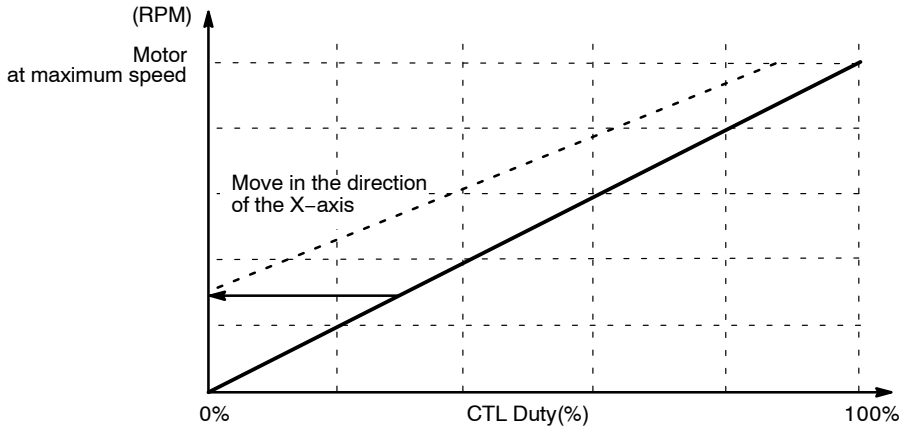


Figure 9.

(Example)
In the case where the characteristics change from ones with the origin point (0%, 0 rpm) to ones where the speed at a duty ratio of 30% becomes the speed at 0%:
First, obtain the input voltage of the CVI pin required at 0%.
CVI = 5 − (3 × duty ratio) = 5 − (3 × 0.3) = 5 − 0.9 = 4.1 V

Next, obtain the resistances at which the voltage becomes 4.1 V by dividing the resistance between CVO and GND when CVO is 5 V. The ratio of CVO−CVI: CVI−GND is 0.9 V : 4.1 V = 1 : 4.5.
Based on the above, the resistance is 20 kΩ between CVO and CVI and 91 kΩ between CVI and GND.
Furthermore, the slope changes. (In the case of the example given, since the resistance ratio is 1 : 4.5, the slope is now 4.5/5.5 = 0.8 times what it was originally.)
If necessary, change the resistance of the RC pin, and adjust the slope.

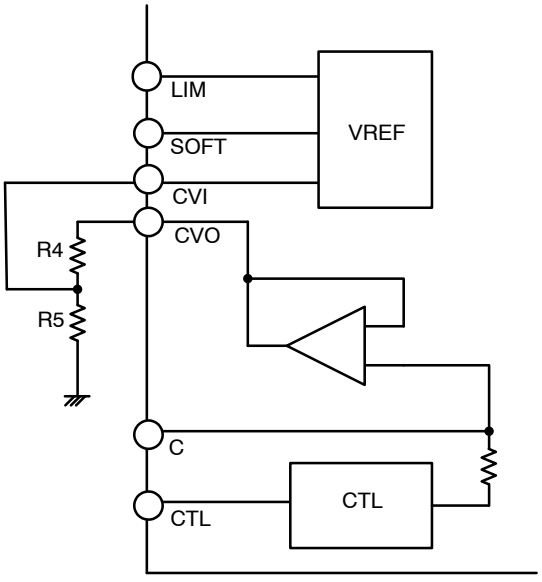


Figure 10.

2) Movement along the Y-axis (resistance divided between CVO and V_{CC})

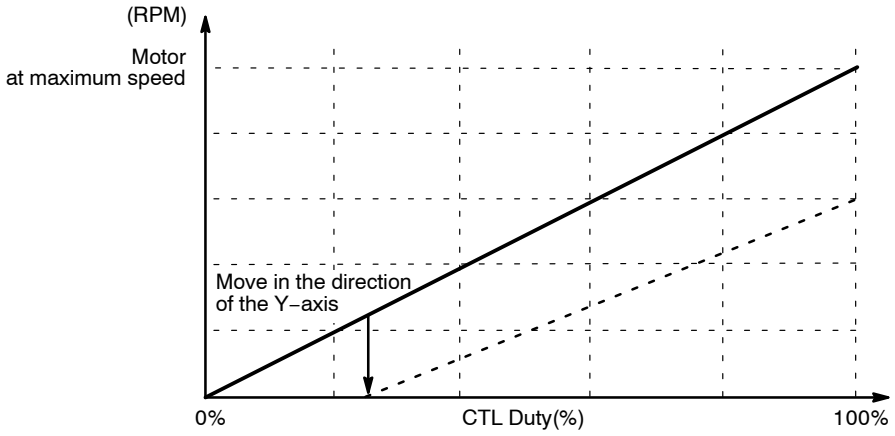


Figure 11.

(Example)
In the case where the characteristics change from ones with the origin point (0%, 0 rpm) to ones where the speed at a duty ratio of 25% becomes 0 rpm:
First, obtain the CVO pin voltage required for the CVI voltage to be 5 V at 25%.
CVO = 5 − (3 × duty ratio) = 5 − (3 × 0.25) = 5 − 0.75 = 4.25 V

With CVO = 4.25 V, find the resistances at which CVI = 5 V.
The ratio of CVO−CVI : CVI−GND is 0.75 V : 7 V = 1 : 9.3.
Based on the above, the resistance is 20 kΩ between CVO and CVI and 180 kΩ between CVI and V_{CC}.
(Due to the current capacity of the CVO pin, the total resistance must be set to 100 kΩ or more.)
Furthermore, the slope changes. (In the case of the example given, since the resistance ratio is 1 : 9.3, the slope is now 9.3/10.3 = 0.9 times what it was originally.)
If necessary, change the resistance of the RC pin, and adjust the slope.

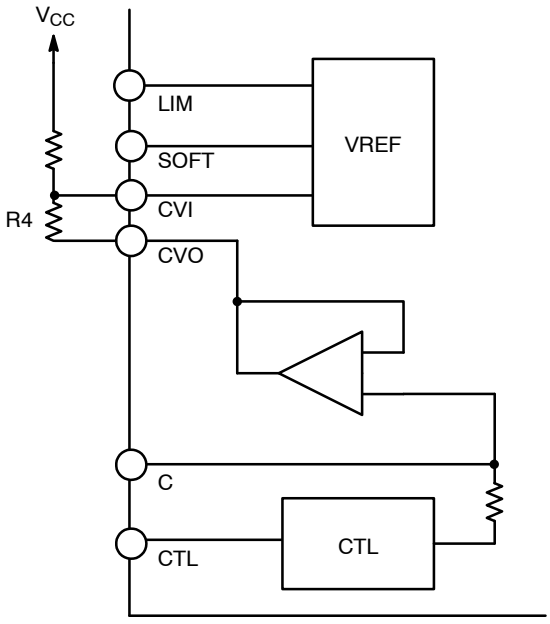


Figure 12.

<LIM Pin>
The minimum speed is determined by the voltage of the LIM pin.

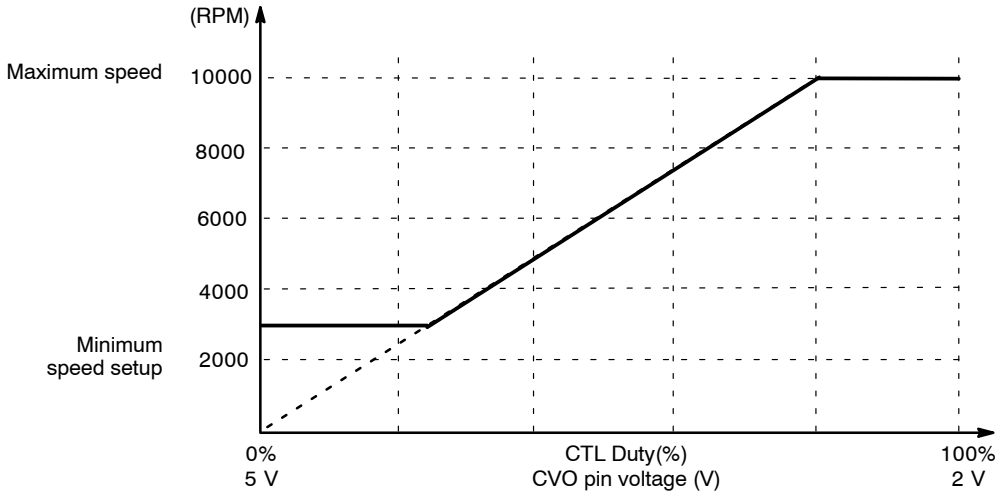


Figure 13.

1) Obtain the ratio of the minimum speed required to the maximum speed.
   Ra = Minimum speed/maximum speed .... <1>
   In the example shown in the figure above, Ra = minimum speed/maximum speed = 3000/10000 = 0.3.
2) Obtain the product of the duty ratio at which the maximum speed is obtained and the value in equation <1>.
   Ca = Duty ratio at maximum speed × Ra .... <2>
   In this example, Ca = duty ratio at maximum speed × Ra = 0.8 × 0.3 = 0.24.
3) Obtain the required LIM pin voltage.
   LIM = 5 − (3 × Ca) .... <3>
   In this example, LIM = 5 − (3 × Ca) = 5 − (3 × 0.24) ≈ 4.3 V.
4) Divide the resistance of 5VREG, and generate the LIM voltage.
   In this example, the voltage is 4.3 V so the resistance ratio is 1 : 6.
   The resistance is 10 kΩ between 5VREG and LIM and 62 kΩ between LIM and GND.

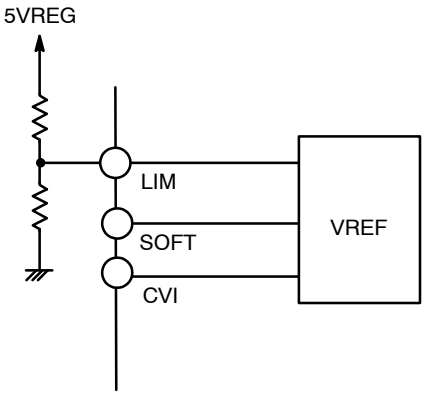


Figure 14.

<C Pin>
In order to connect a capacitor capable of smoothing the pin voltage to the C pin, the correlation given in the following equation must be satisfied when f (Hz) serves as the input signal frequency of the CTL pin. (R is contained inside the IC, and is 180 kΩ (typ.).)
$1/f = t < CR$
The higher the capacitance of the capacitor is, the slower the response to changes in the input signal is.

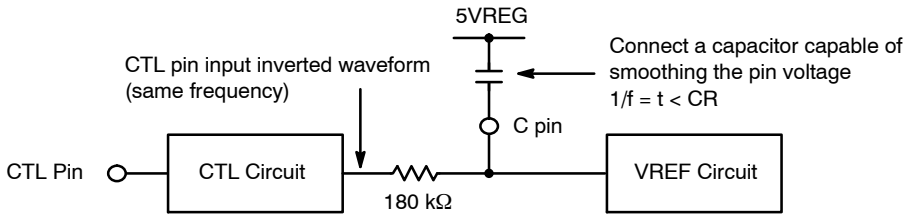


Figure 15.

ORDERING INFORMATION

Device	Package	Wire Bond	Shipping† (Qty / Packing)
LB11850VA−TLM−E	SSOP24 (225mil) (Pb−Free)	Au−wire	2,000 / Tape & Reel
LB11850VA−TLM−H	SSOP24 (225mil) (Pb−Free / Halogen Free)	Au−wire	2,000 / Tape & Reel
LB11850VA−W−AH	SSOP24 (225mil) (Pb−Free / Halogen Free)	Cu−wire	2,000 / Tape & Reel

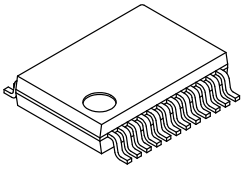
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

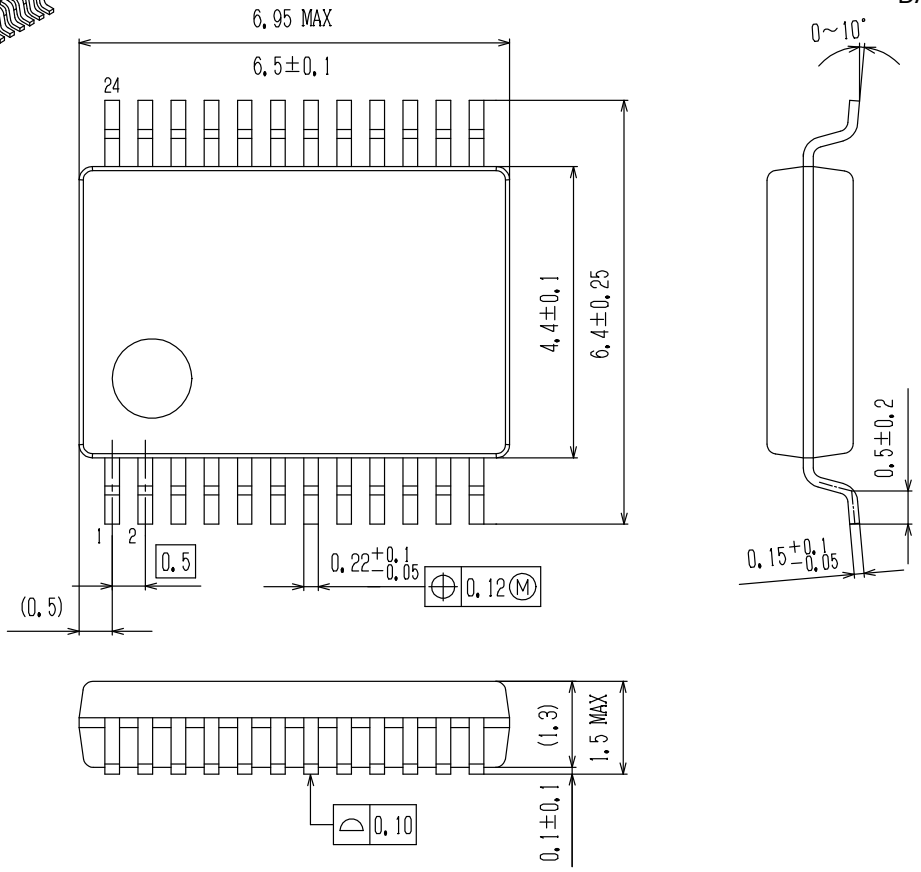
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

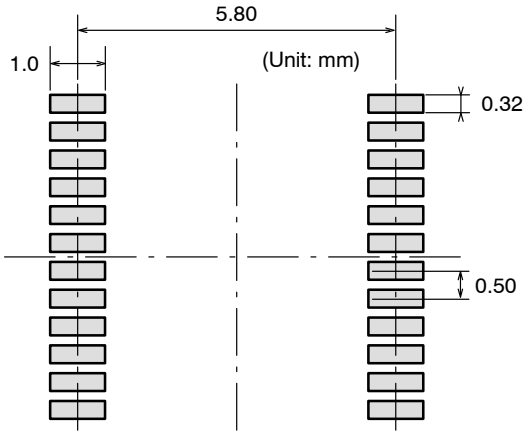
SSOP24 (225mil)
CASE 565AR
ISSUE A

DATE 23 OCT 2013





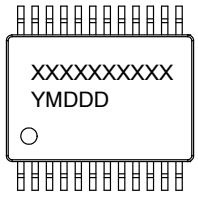
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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NEW STANDARD:			
DESCRIPTION:	**SSOP24 (225MIL)**		**PAGE 1 OF 2**

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