



LC4120NV

LCD Power Supply Switching IC

Overview

The LC4120NV is an LCD power supply switching IC that provides 3 input channels and 6 output channels. It is fabricated in an 80-V high-voltage CMOS process and features low power dissipation, high speed, and a low output impedance. This IC is optimal for switching the row driver LCD drive voltage in a wide range of LCD products.

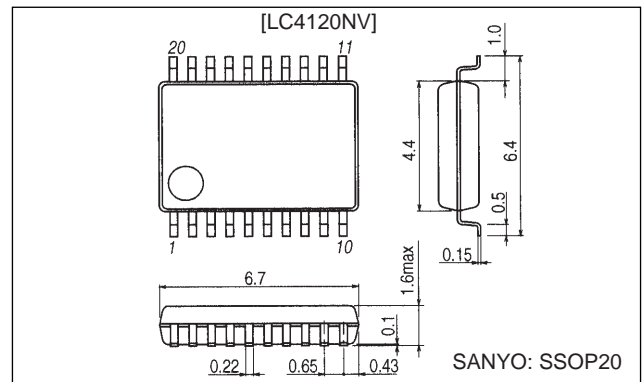
Features

- 3 input channels/6 output channels
- Logic voltage: 2.7 to 5.5 V
- Output voltage: 80 V (maximum)
- Output impedance: 110Ω (maximum)
(When $V_{HA} - V_{LA} = 60$ V)
- Output delay time: 0.5 μs (maximum)
- Operating temperature: -20 to 75°C
- Package: 20-pin SSOP

Package Dimensions

unit: mm

3179A-SSOP20



Specifications

Absolute Maximum Ratings (The following conditions must hold at all times: $V_{HA} \geq V_{HB} > V_{DD} > V_{SS} > V_{LB} \geq V_{LA}$)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD \text{ max}}$	V_{DD}	-0.3 to +7.0	V
	$V_{HA, B} - V_{LA, B}$	$V_{HA, B} / V_{LA, B}$	-0.3 to +85	V
	V_{HA} / V_{HB}	V_{HA} / V_{HB}	-0.3 to +45.0	V
	V_{LA} / V_{LB}	V_{LA} / V_{LB}	-40.0 to +0.3	V
Input voltage	V_{IN}	S1 to S3	-0.3 to $V_{DD} + 0.3$	V
Operating temperature	T_{opr}		-20 to +75	°C
Storage temperature	T_{stg}		-40 to +125	°C

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Electrical Characteristics

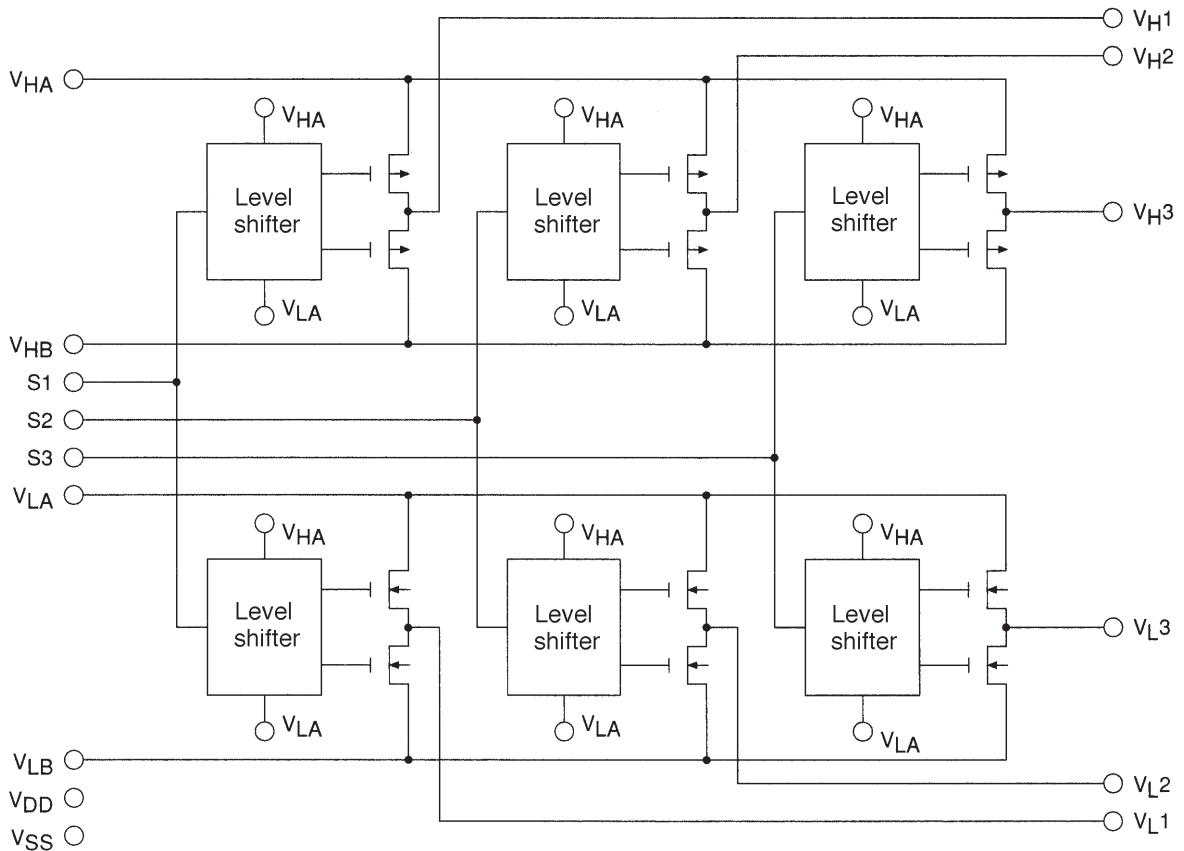
DC Characteristics at $T_a = -20$ to 75°C , $V_{SS} = 0\text{ V}$, $V_{DD} = 2.7$ to 5.5 V unless otherwise specified

(The following conditions must hold at all times: $V_{HA} \geq V_{HB} > V_{DD} > V_{SS} > V_{LB} \geq V_{LA}$.)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating voltage	V_{DD}	V_{DD}	2.7	5.0	5.5	V
	$V_{HA, B} - V_{LA, B}$	$V_{HA, B}, V_{LA, B}$	40.0		80.0	V
	V_{HA}, V_{HB}	V_{HA}, V_{HB}	20.0		42.5	V
	V_{LA}, V_{LB}	V_{LA}, V_{LB}	-37.5		-20.0	V
Potential difference	$V_{HA} - V_{HB}$	V_{HA}, V_{HB}	0		5.0	V
	$V_{LA} - V_{LB}$	V_{LA}, V_{LB}	0		5.0	V
Input high-level voltage	V_{IH}	S1 to S3	$V_{DD} \times 0.8$		V_{DD}	V
Input low-level voltage	V_{IL}	S1 to S3	0		$V_{DD} \times 0.2$	V
Output high-level voltage	R_{OHA}	$V_{OUT} = V_{HA} - 0.5 : V_{H1}$ to $V_{H3} *1$		70	110	Ω
	R_{OHB}	$V_{OUT} = V_{HB} - 0.5 : V_{H1}$ to $V_{H3} *1$		70	110	Ω
Output low-level voltage	R_{OLA}	$V_{OUT} = V_{LA} + 0.5 : V_{L1}$ to $V_{L3} *2$		70	110	Ω
	R_{OLB}	$V_{OUT} = V_{LB} + 0.5 : V_{L1}$ to $V_{L3} *2$		70	110	Ω
Current drain	I_{DDOPE}	$f = 40\text{ kHz}$, Input signals operating *3			80	μA
	I_{HOPE}	$f = 40\text{ kHz}$, Input signals operating *3			600	μA
	I_{HLEAK}	$f = 40\text{ kHz}$, Input signals stopped *3	-10		+10	μA

Notes: 1. $V_{HA} - V_{LA} = 60\text{ V}$, $V_{HA} - V_{HB} = 1.0\text{ V}$
 2. $V_{HA} - V_{LA} = 60\text{ V}$, $V_{LA} - V_{LB} = 1.0\text{ V}$
 3. $V_{HA} - V_{LA} = 60\text{ V}$, $V_{HA} - V_{HB} = V_{LA} - V_{LB} = 1.0\text{ V}$

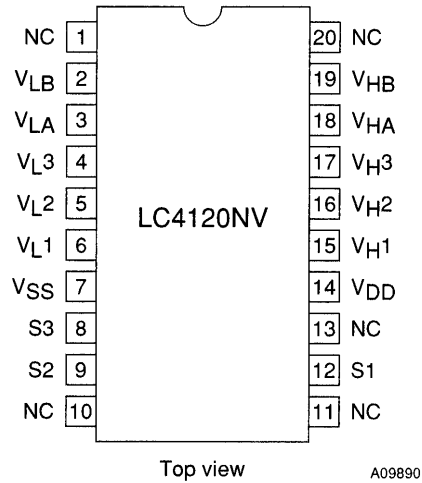
Block Diagram



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Pin Assignment



Pin Functions

Pin	I/O	Function	Signal voltage
V _{H1}	O	High-voltage output 1	V _{HA} /V _{HB}
V _{H2}	O	High-voltage output 2	V _{HA} /V _{HB}
V _{H3}	O	High-voltage output 3	V _{HA} /V _{HB}
V _{L1}	O	Low-voltage output 1	V _{LA} /V _{LB}
V _{L2}	O	Low-voltage output 2	V _{LA} /V _{LB}
V _{L3}	O	Low-voltage output 3	V _{LA} /V _{LB}
S1	I	Logic input 1	V _{DD} /V _{SS}
S2	I	Logic input 2	V _{DD} /V _{SS}
S3	I	Logic input 3	V _{DD} /V _{SS}
V _{HA}		High-voltage power supply A	
V _{HB}		High-voltage power supply B	
V _{LA}		Low-voltage power supply A	
V _{LB}		Low-voltage power supply B	
V _{DD}		Logic system power supply	
V _{SS}		Logic system ground	

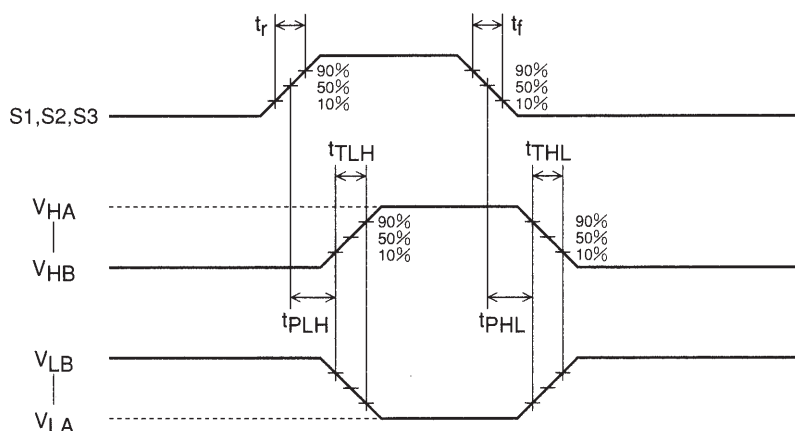
Truth Table

Input signal	Output	
	V _{Hn}	V _{Ln}
H	V _{HA}	V _{LA}
L	V _{HB}	V _{LB}

(n = 1, 2, 3)

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AC Characteristics



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Conditions 1 at $T_a = -20$ to 75°C , $V_{SS} = 0$ V, $V_{DD} = 2.7$ to 5.5 V, $V_{HA} = 42.5$ V, $V_{HB} = 37.5$ V, $V_{LA} = -37.5$ V, $V_{LB} = -32.5$ V, $C_L = 50$ pF, unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output rise time	t_{TLH}			80	160	ns
Output fall time	t_{THL}			80	160	ns
High-level transmission delay time	t_{PLH}			200	500	ns
Low-level transmission delay time	t_{PHL}			200	500	ns
Input rise and fall times	t_r/t_f				30	ns

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