Ordering number : EN*4247A

CMOS LSI

LC74730M

On-Screen Display Controller LSI

Preliminary

Overview

The LC74730M is a CMOS LSI for on-screen display, a function that displays characters and patterns on a TV screen under microprocessor control. (The LC74730M supports the S-VCR format.) The characters displayed have an 8 × 8 dots structure and a dot interpolation function is provided. The LC74730M display 10 lines of 24 characters each.

Features

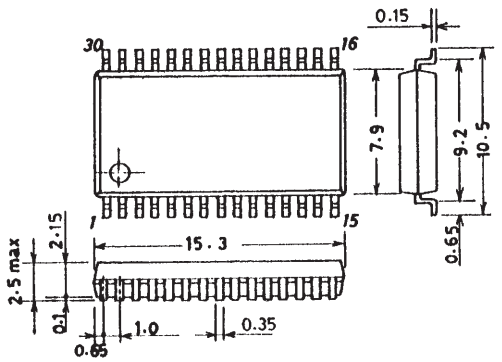
- Screen format: 10 lines × 24 characters (up to 240 characters)
- Character format: 8 (horizontal) × 8 (vertical) (interpolation function provided)
- Character sizes: Three horizontal sizes and 3 vertical sizes
- Number of characters in font: 64 characters
- Display start position
  - — Horizontal: 64 positions
  - — Vertical: 64 positions
- Blinking: In character units
- Types of blinking: Two types with approximately 1.0 sec. and 0.5 sec.
- Background color: Four background colors (in internal synchronization mode)
  (For the PAL-M format: 1 color; blue background)
- External control input: 8-bit serial data input format
- Built-in sync separator circuit
- Built-in synchronization recognition circuit: Recognizes whether or not external synchronizing signals are present
- Video output: NTSC and PAL-M format composite outputs, Y-C output

Package Dimensions

unit: mm

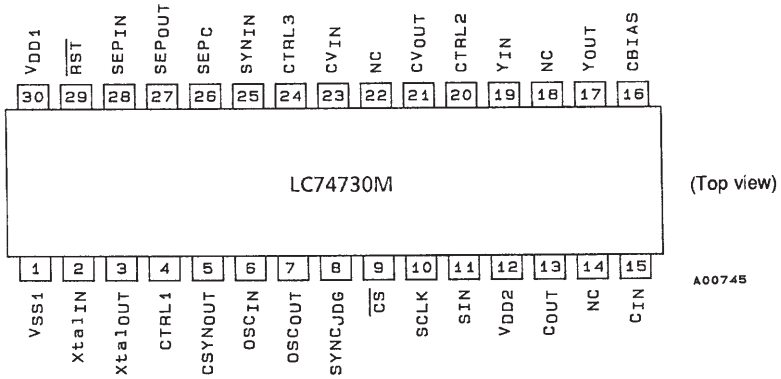
3073A-MFP30S

[LC74730M]



SANYO: MFP30S

Pin Assignment



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	$V_{DD}1$, $V_{DD}2$	V_{SS} – 0.3 to V_{SS} + 7.0	V
Maximum input voltage	V_{IN} max	All input pins	V_{SS} – 0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max	$CSYN_{OUT}$, $SYNC_{JDG}$, SEP_{OUT}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = –30 to +70°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}1$	$V_{DD}1$	4.5	5.0	5.5	V
	$V_{DD}2$	$V_{DD}2$	4.5	5.0	1.27 $V_{DD}1$	V
Input high-level voltage	$V_{IH}1$	$\overline{RST}$, $\overline{CS}$, SIN, SCLK	0.8 $V_{DD}1$		$V_{DD}1$ + 0.3	V
	$V_{IH}2$	CTRL1 to CTRL3, SEP_{IN}	0.7 $V_{DD}1$		$V_{DD}1$ + 0.3	V
Input low-level voltage	$V_{IL}1$	$\overline{RST}$, $\overline{CS}$, SIN, SCLK	V_{SS} – 0.3		0.2 $V_{DD}1$	V
	$V_{IL}2$	CTRL1 to CTRL3, SEP_{IN}	V_{SS} – 0.3		0.3 $V_{DD}1$	V
Composite video input voltage	$V_{IN}1$	CV_{IN}		2 Vp-p		V
	$V_{IN}2$	SYN_{IN}		2 Vp-p	2.5 Vp-p	V
Input voltage	$V_{IN}3$	The $Xtal_{IN}$ oscillator pin (in external clock input mode) Expected value (design target value)	140			mV
Oscillator frequency	$f_{OSC}1$	The $Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins ($2f_{sc}$)		7.159		MHz
	$f_{OSC}2$	The OSC_{IN} and OSC_{OUT} oscillator pins (LC oscillator)	5	8	12	MHz

Electrical Characteristics at Ta = –30 to +70°C, unless otherwise specified $V_{DD}1$ = 5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Output off leakage current	$I_{leak}1$	C_{OUT}, Y_{OUT}, CV_{OUT}			10	µA
Input off leakage current	$I_{leak}2$	C_{IN}, Y_{IN}, CV_{IN}			10	µA
Output high-level voltage	$V_{OH}1$	$CSYN_{OUT}$, $SYNC_{JDG}$, SEP_{OUT}; $V_{DD}1$ = 4.5 V, I_{OH} = 1.0 mA	3.5			V
Output low-level voltage	$V_{OL}1$	$CSYN_{OUT}$, $SYNC_{JDG}$, SEP_{OUT}; $V_{DD}1$ = 4.5 V, I_{OL} = 1.0 mA			1.0	V
Input current	I_{IH}	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, CTRL1 to CTRL3, SEP_{IN}; V_{IN} = $V_{DD}1$			1	µA
	I_{IL}	CTRL1 to CTRL3, OSC_{IN}: V_{IN} = $V_{SS}1$	–1			µA
Operating current drain	$I_{DD}1$	$V_{DD}1$; all outputs open, crystal: 7.159 MHz, LC: 8 MHz			15	mA
	$I_{DD}2$	$V_{DD}2$; $V_{DD}2$ = 5 V			20	mA

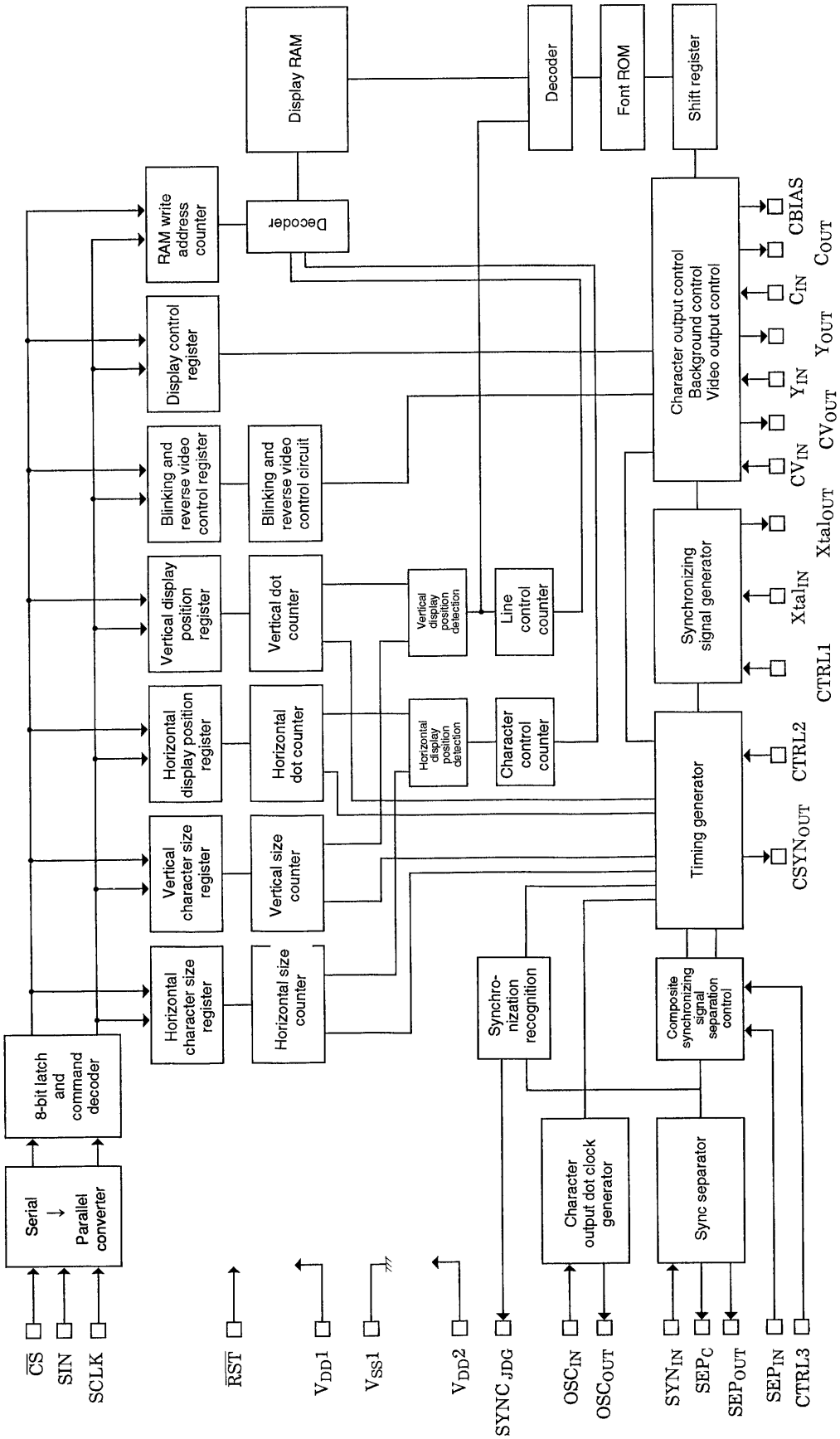
Timing Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 ± 0.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Minimum input pulse width	$t_{W\ (SCLK)}$	SCLK	200			ns
	$t_{W\ (CS)}$	$\overline{CS}$ pin (during the period that $\overline{CS}$ is high)	1			µs
Data setup time	$t_{SU\ (CS)}$	$\overline{CS}$	200			ns
	$t_{SU\ (SIN)}$	SIN	200			ns
Data hold time	$t_{h\ (CS)}$	$\overline{CS}$	2			µs
	$t_{h\ (SIN)}$	SIN	200			ns
One word write time	t_{word}	The 8-bit data write time	4.2			µs
	t_{wt}	The RAM data write time	1			µs

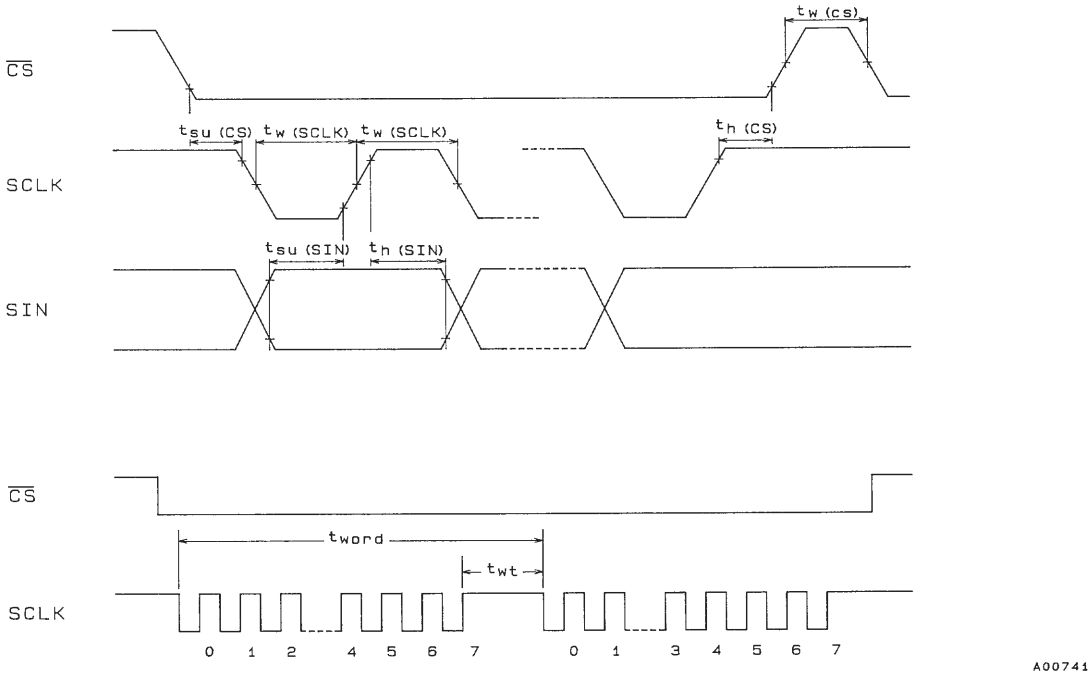
Pin Functions

Pin No.	Symbol	Function	Description
1	$V_{SS}1$	Ground	Ground connection
2	$Xtal_{IN}$	Crystal oscillator element connection	Used to connect the external crystal and capacitors for the crystal oscillator that generates the internal synchronizing signal. Also used for an external clock input. ($2f_{sc}$: 7.159 MHz)
3	$Xtal_{OUT}$		
4	CTRL1	Crystal oscillator input switching	Switches between the external $2f_{SC}$ clock input mode and the crystal resonator driving mode. Low: crystal oscillator, high: external clock input
5	$CSYN_{OUT}$	Composite synchronizing signal output	Outputs the composite synchronizing signal. Outputs the crystal oscillator clock on a reset due to a low level on the $\overline{RST}$ pin. Does not output any signal on a command reset.
6	OSC_{IN}	LC oscillator	Connections for the coil and capacitor that form the oscillator that generates the character output dot clock.
7	OSC_{OUT}		
8	$SYNC_{JDG}$	External synchronizing signal state judgment output	Outputs the judgment as to whether or not an external synchronizing signal is present. Outputs a high level when a synchronizing signal is present. Outputs the dot clock (LC oscillator) on a reset due to a low level on the $\overline{RST}$ pin. Does not output any signal on a command reset.
9	$\overline{CS}$	Enable input	Enable input for serial data input. Serial data input is enabled by a low level. A pull-up resistor is built in. (This input has hysteresis characteristics.)
10	SCLK	Clock input	Serial data input clock input. A pull-up resistor is built in. (This input has hysteresis characteristics.)
11	SIN	Data input	Serial data input. A pull-up resistor is built in. (This input has hysteresis characteristics.)
12	$V_{DD}2$	Power supply	Video signal level adjustment power supply. (Analog system power supply)
13	C_{OUT}	Color signal output	Color (C) signal output
14	NC		This pin must be level open or connected to ground.
15	C_{IN}	Color signal input	Color (C) signal input
16	CBIAS	Chrominance bias output	Chrominance signal bias level output
17	Y_{OUT}	Luminance signal output	Luminance signal (Y) output
18	NC		This pin must be level open or connected to ground.
19	Y_{IN}	Luminance signal input	Luminance signal (Y) input
20	CTRL2	NTSC/PAL-M switching input	Switches the synchronizing signal generator between NTSC and PAL-M formats. Low: NTSC, high: PAL-M
21	CV_{OUT}	Composite video signal output	Outputs a composite video signal.
22	NC		This pin must be level open or connected to ground.
23	CV_{IN}	Composite video signal input	Inputs a composite video signal.
24	CTRL3	SEP_{IN} input control	Controls whether the $\overline{VSYNC}$ signal is input to the SEP_{IN} input. Low: $\overline{VSYNC}$ is input, high: $\overline{VSYNC}$ is not input.
25	SYN_{IN}	Sync separator circuit input	Video signal input to the built-in sync separator circuit. (Input either a horizontal or composite synchronizing signal to this pin if the built-in sync separator circuit is not used.)
26	SEP_C	Sync separator circuit adjustment	Adjusts the built-in sync separator circuit. (Connect a capacitor to this pin.) (Leave this pin open if the built-in sync separator circuit is not used.)
27	SEP_{OUT}	Composite synchronizing signal output	Outputs the built-in sync separator circuit composite synchronizing signal. (Outputs the SYN_{IN} input signal if the built-in sync separator circuit is not used.)
28	SEP_{IN}	Vertical synchronizing signal input	Integrates the SEP_{OUT} output signal and inputs a vertical synchronizing signal. An integration circuit must be connected between this pin and the SEP_{OUT} pin. This pin must be tied to $V_{DD}1$ if it is not used.
29	$\overline{RST}$	Reset input	The system reset input. A pull-up resistor is built in. (This input has hysteresis characteristics.)
30	$V_{DD}1$	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

Block Diagram



Serial Data Input Timing



Display Control Commands

The display control commands have an 8-bit serial input format. Commands consist of a first byte, which includes the command identification code, and data in the second and following bytes. The LC74730M supports the following commands:

① COMMAND 0: Display memory (VRAM) write address setup command
② COMMAND 1: Display character data write command
③ COMMAND 2: Vertical display start position and vertical size setup command
④ COMMAND 3: Horizontal display start position and horizontal size setup command
⑤ COMMAND 4: Display control setup command
⑥ COMMAND 5: Synchronizing signal control setup command

Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND 0 Set write address	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND 1 Write character	1	0	0	1	0	0	0	0	at	0	c5	c4	c3	c2	c1	c0
COMMAND 2 Set vertical display start position and vertical character size	1	0	1	0	VS 21	VS 20	VS 11	VS 10	0	0	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND 3 Set horizontal display start position and horizontal character size	1	0	1	1	HS 21	HS 20	HS 11	HS 10	0	0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND 4 Display control	1	1	0	0	TST MOD	CB	OSC STP	SYS RST	0	0	NON	EG	BK 1	BK 0	RV	DSP ON
COMMAND 5 Synchronizing signal control	1	1	0	1	PH 1	PH 0	BCL	INT	0	0	0	0	SN 3	SN 2	SN 1	SN 0

The command identification code in a first byte is retained until the next first byte is written. However, if a display character data write command (COMMAND 1) is written, the LC74730M locks in display character data write mode, and the first byte cannot be overwritten.
The command state is reset to the COMMAND 0 state (display memory address setup mode) when the $\overline{CS}$ pin is set high.

① COMMAND 0 (Display memory write address setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 0 identification code Set the display memory write address.	
6	—	0		
5	—	0		
4	—	0		
3	V3	0	Display memory line address (0 to 9 hexadecimal)	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	H4	0	Display memory character address (0 to 17 hexadecimal)	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note: All these registers are set to 0 by a reset due to the $\overline{\text{RST}}$ pin.

② COMMAND 1 (Display character data write setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 1 identification code Sets up a display character data write operation	When this command is issued, the LC74730M is locked in display character data write mode until the $\overline{\text{CS}}$ pin goes high.
6	—	0		
5	—	0		
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	—	0		

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	at	0	Character attributes off	
		1	Character attributes on	
6	—	0		
5	c5	0	Character code (00 to 3F hexadecimal)	
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

Note: All these registers are set to 0 by a reset due to the $\overline{\text{RST}}$ pin.

③ COMMAND 2 (Vertical display start position and vertical size setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 2 identification code Sets up the vertical display position and the character size in the vertical direction.	
6	—	0		
5	—	1		
4	—	0		
3	VS21	0		
		1		
2	VS20	0		
		1		
1	VS11	0		
		1		
0	VS10	0		
		1		

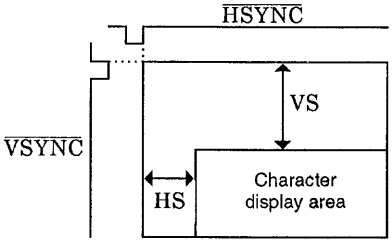
VS21 \ VS20	0	1
0	1 H per dot	2 H per dot
1	3 H per dot	1 H per dot

Vertical character size for the second line

VS11 \ VS10	0	1
0	1 H per dot	2 H per dot
1	3 H per dot	1 H per dot

Vertical character size for the first line

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	VP5 (MSB)	0	If VS is the vertical display start position then: $VS = H \times (2\sum_{n=0}^{5} 2^n VP_n)$ Where H is horizontal period pulse period.  	The vertical display start position is specified by the 6 bits VP0 to VP5. The weight of the low-order bit is 2 H.
		1		
4	VP4	0		
		1		
3	VP3	0		
		1		
2	VP2	0		
		1		
1	VP1	0		
		1		
0	VP0 (LSB)	0		
		1		

Note: All these registers are set to 0 by a reset due to the $\overline{RST}$ pin.

④ COMMAND 3 (Horizontal display start position and horizontal size setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 3 identification code Sets up the horizontal display position and the character size in the horizontal direction.	
6	—	0		
5	—	1		
4	—	1		
3	HS21	0	HS21 \ HS20: 0 / 1 0: 1 Tc per dot / 2 Tc per dot 1: 3 Tc per dot / 1 Tc per dot	Horizontal character size for the second line
		1		
2	HS20	0		
		1		
1	HS11	0	HS11 \ HS10: 0 / 1 0: 1 Tc per dot / 2 Tc per dot 1: 3 Tc per dot / 1 Tc per dot	Horizontal character size for the first line
		1		
0	HS10	0		
		1		

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	HP5 (MSB)	0	If HS is the horizontal start position then: $HS = Tc \times (2\sum_{n=0}^{5} 2^n HP_n)$ Where Tc is a single period of the LC oscillator connected the OSC_{IN} and OSC_{OUT} pins.	The horizontal display start position is specified by the 6 bits HP0 to HP5. The weight of the low-order bit is 2 Tc.
		1		
4	HP4	0		
		1		
3	HP3	0		
		1		
2	HP2	0		
		1		
1	HP1	0		
		1		
0	HP0 (LSB)	0		
		1		

Note: All these registers are set to 0 by a reset due to the $\overline{RST}$ pin.

⑤ COMMAND 4 (Display control setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 4 identification code Sets up the display control state.	
6	—	1		
5	—	0		
4	—	0		
3	TSTMOD	0	Normal operating mode	Must be set to 0.
		1	Test mode	
2	CB	0	Output the color burst signal.	Valid only when BCL is high.
		1	Stop color burst signal output.	
1	OSCSTP	0	Does not stop the crystal and LC oscillators.	Valid in external synchronization mode when character display is off.
		1	Stops the crystal and LC oscillators.	
0	SYSRST	0		Reset occurs when the $\overline{CS}$ pin is low, and the reset is cleared when $\overline{CS}$ goes high.
		1	Resets all registers and turns off display.	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification code	
6	—	0		
5	NON	0	Interlace (262.5 H per field)	Switches between interlaced and non-interlaced display
		1	Non-interlaced (263 H per field)	
4	EG	0	Border off	
		1	Border on	
3	BK1	0	Blinking period: about 0.5 s	Switches the blinking period
		1	Blinking period: about 1 s	
2	BK0	0	Blinking off	Blinking during reversed video character display switches the character display between normal display and reversed video display.
		1	Blinking on	
1	RV	0	Reverse video character display off	
		1	Reverse video character display on	
0	DSPON	0	Character display off	
		1	Character display on	

Note: All these registers are set to 0 by a reset due to the $\overline{RST}$ pin.

⑥ COMMAND 5 (Synchronizing signal control setup command)

First byte

<table>
<tr><th rowspan="2">DA0 to DA7</th><th rowspan="2">Register name</th><th colspan="2">Register content</th><th rowspan="2">Note</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>1</td><td rowspan="4">Command 5 identification code
Sets up control of the synchronizing signals</td><td rowspan="4"></td></tr>
<tr><td>6</td><td>—</td><td>1</td></tr>
<tr><td>5</td><td>—</td><td>0</td></tr>
<tr><td>4</td><td>—</td><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">PH1</td><td>0</td><td rowspan="4"><table><tr><th>PHASE1</th><th>PHASE0</th><th>Background color (phase)</th></tr><tr><td>0</td><td>0</td><td>π/2</td></tr><tr><td>0</td><td>1</td><td>π</td></tr><tr><td>1</td><td>0</td><td>3π/2</td></tr><tr><td>1</td><td>1</td><td>In phase</td></tr></table></td><td rowspan="4">Sets the background color
(one of 4 colors).
There is only one background color
(blue) in PAL-M mode.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">PH0</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">BCL</td><td>0</td><td>Background color displayed.</td><td rowspan="2">Valid only in internal synchronization mode</td></tr>
<tr><td>1</td><td>No background color (only the background level is set).</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">INT</td><td>0</td><td>External synchronization</td><td rowspan="2">Switches between internal and external synchronization.</td></tr>
<tr><td>1</td><td>Internal synchronization</td></tr>
</table>

Second byte

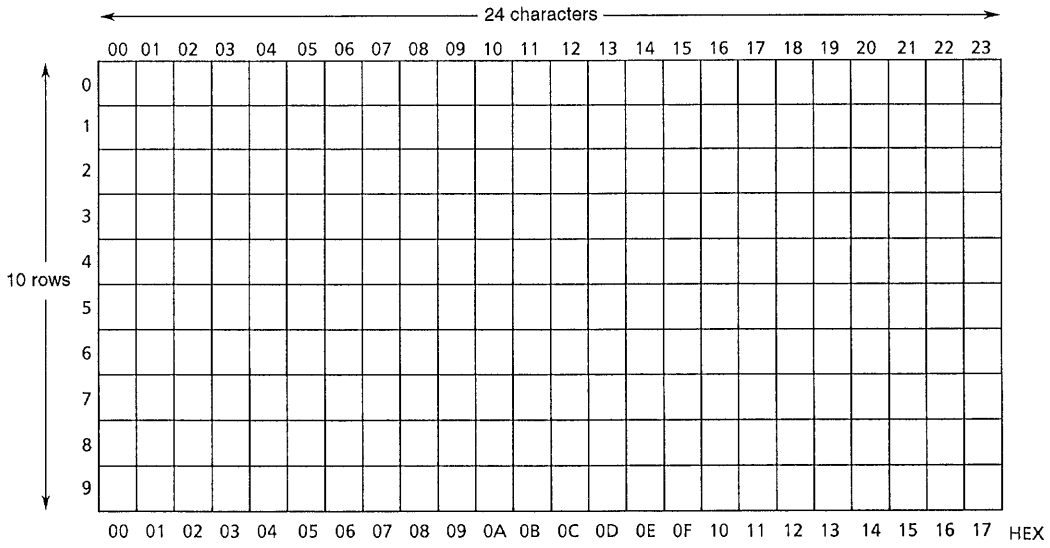
<table>
<tr><th rowspan="2">DA0 to DA7</th><th rowspan="2">Register name</th><th colspan="2">Register content</th><th rowspan="2">Note</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>0</td><td>Second byte identification bit</td><td></td></tr>
<tr><td>6</td><td>—</td><td>0</td><td></td><td></td></tr>
<tr><td>5</td><td>—</td><td>0</td><td></td><td></td></tr>
<tr><td>4</td><td>—</td><td>0</td><td></td><td></td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">SN3</td><td>0</td><td rowspan="8"><table><tr><th>SN3</th><th>SN2</th><th>SN1</th><th>SN0</th><th>Number of times HSYNC detected</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Not detected</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>16 times</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>32 times</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>64 times</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>128 times</td></tr></table></td><td rowspan="8">External synchronizing signal detection control</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">SN2</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">SN1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">SN0</td><td>0</td></tr>
<tr><td>1</td></tr>
</table>

Note: All these registers are set to 0 by a reset due to the $\overline{\text{RST}}$ pin.

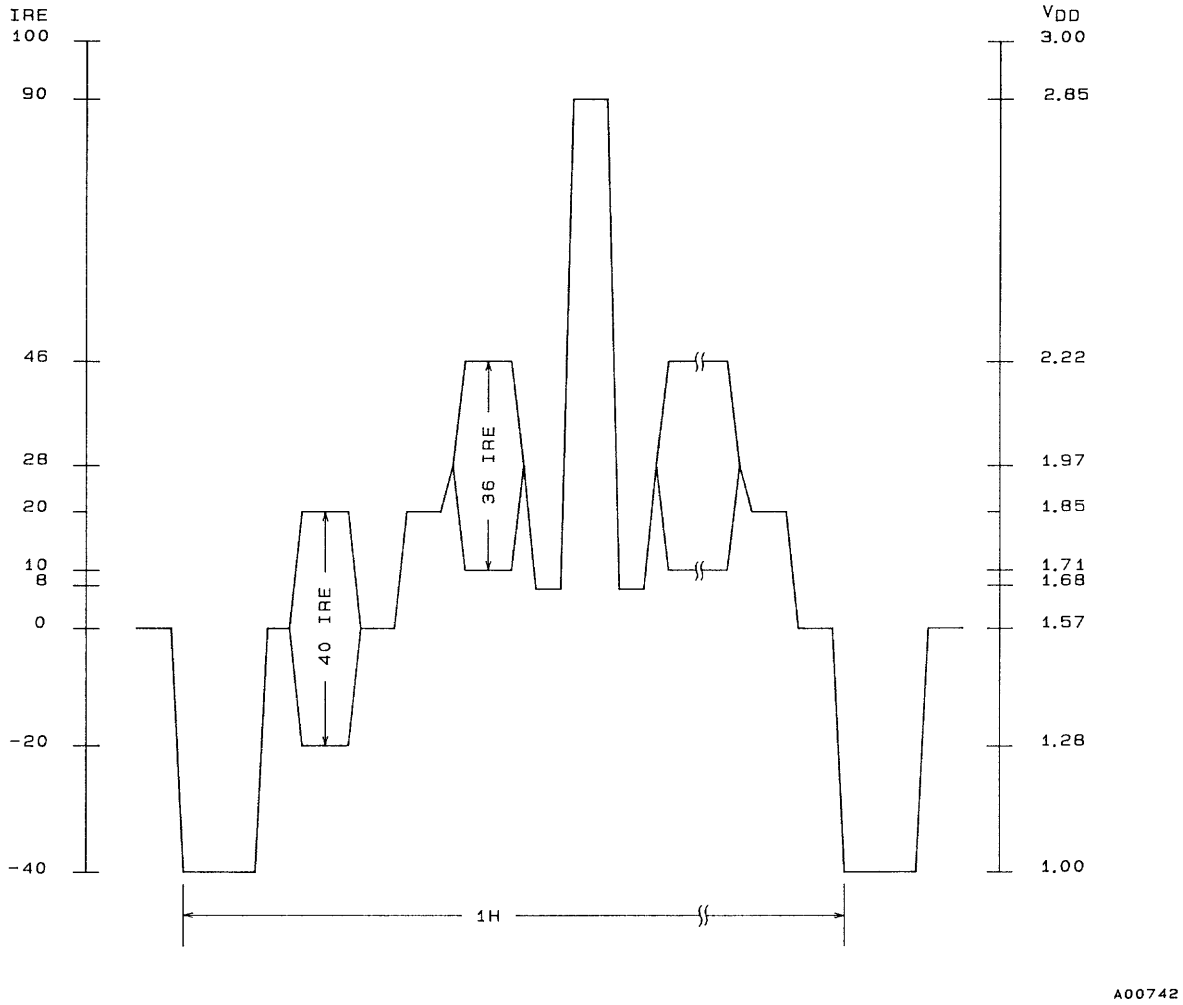
Display Screen Organization

The display screen consists of 10 lines of 24 characters each. Thus the maximum number of characters that can be displayed is 240 characters. However, the maximum number of characters that can be displayed may be fewer than 240 when characters are enlarged. The display memory address consists of a line address (with values from 0 to 9 decimal), and a column (character position) address (with values from 0 to 23 decimal).

Display Screen Organization (Display memory address)



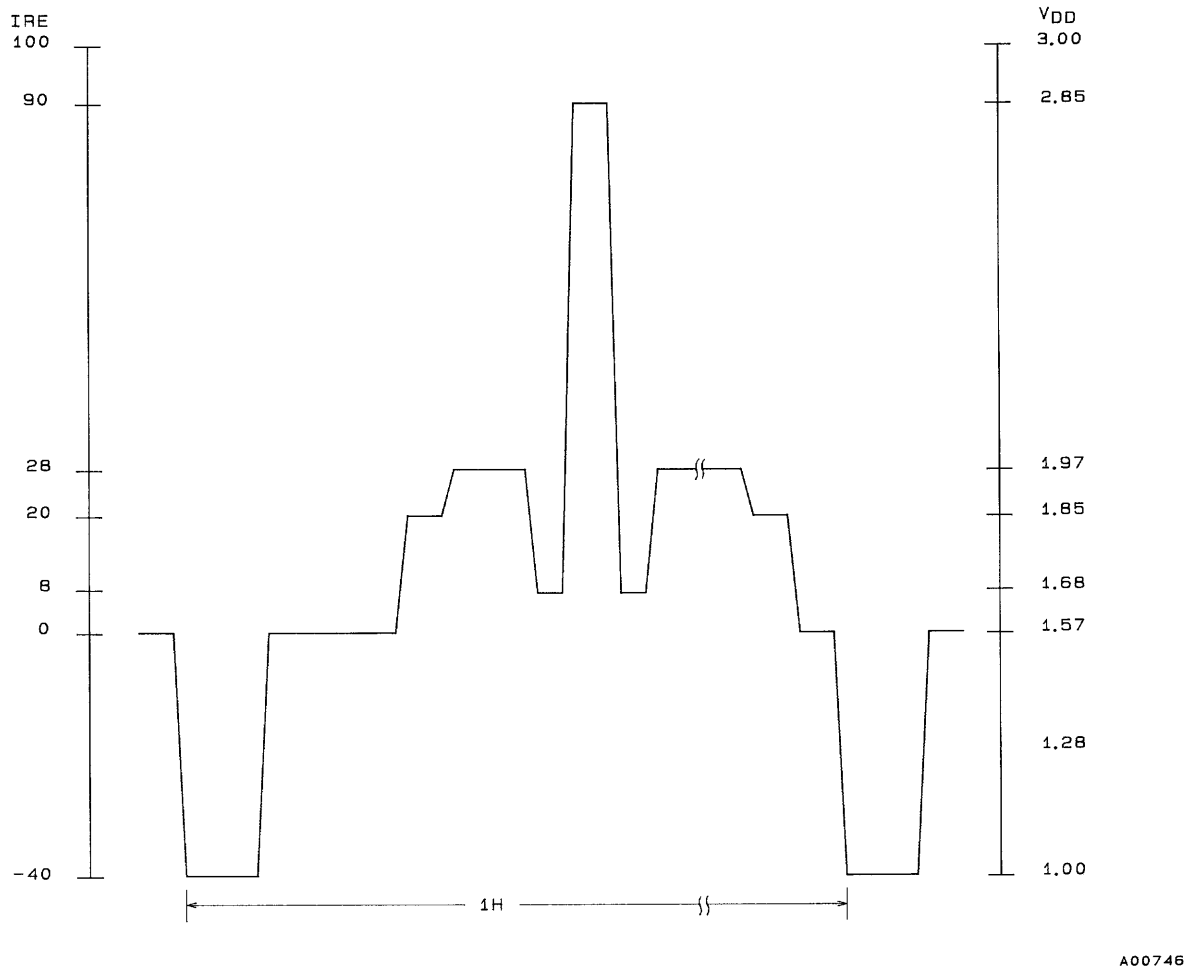
Composite Video Signal Output Levels (internally generated levels)



Output level (IRE)	Output voltage (V_{DC})
100	3.000
90	2.857
46	2.228
20	1.857
10	1.714
8	1.685
0	1.571
–20	1.285
–40	1.000

Note: $V_{DD}2 = 5.000\ V_{DC}$

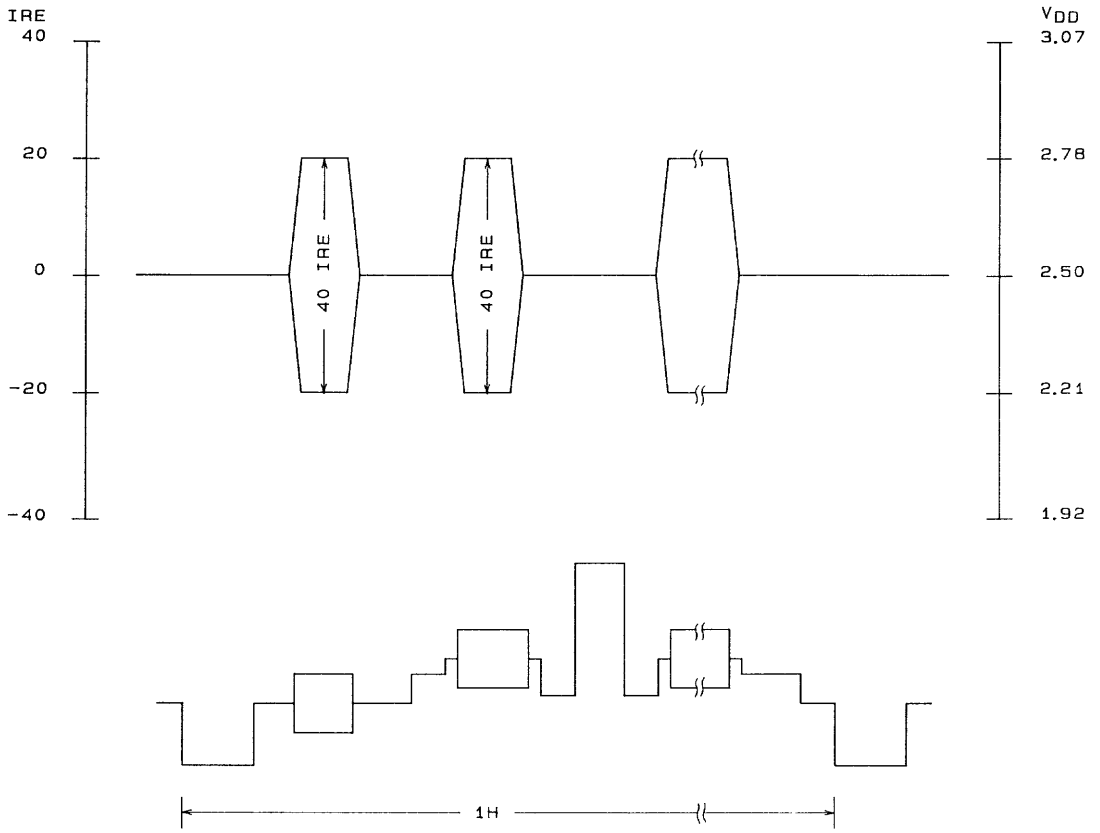
Video Signal Output Levels (Y (luminance) signal: internally generated levels)



Output level (IRE)	Output voltage (V_{DC})
100	3.000
90	2.857
28	1.971
20	1.857
8	1.685
0	1.571
–40	1.000

Note: $V_{DD}2 = 5.000\ V_{DC}$

Video Signal Output Levels (chrominance signal: internally generated levels)



Output level (IRE)	Output voltage (V_{DC})
40	3.071
20	2.786
0	2.500
–20	2.214
–40	1.928

Note: $V_{DD}2 = 5.000\ V_{DC}$