



# **On-Screen Display Controller LSI**

#### Overview

The LC74770M is a CMOS LSI that implements onscreen display, a function that displays characters and patterns on display screens such as camcorder viewfinder screens under microprocessor control. This LSI displays 12-dot by 18-dot characters.

#### **Features**

- Display format: 24 characters by 12 rows (up to 288 characters)
- Characters displayed: Up to 288 characters
- Character format: 12 (horizontal) × 18 (vertical)
- Characters in font: 128
- Character sizes: Normal and double
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Reverse video function: Characters can be displayed in reverse video specified in units of individual characters.
- Blinking types: In character units in one of two periods, 1.0 second and 0.5 second, with a 50% duty.
- Outputs: Character and blanking data, with two output systems for each
- External control input: 8-bit serial input format
- General-purpose output port: 4 bits (controlled from the serial input data)

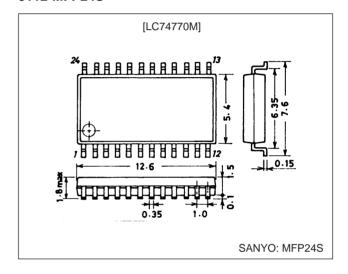
#### **Pin Assignment**

# LC74770M LC74770M LC74770M Top view

## **Package Dimensions**

unit: mm

#### 3112-MFP24S



# **Specifications**

# Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max	V <sub>DD</sub>	$V_{SS} - 0.3 \text{ to } V_{SS} + 7.0$	V
Maximum input voltage	V <sub>IN</sub> max	All input pins	$V_{SS} - 0.3 \text{ to } V_{DD} + 0.3$	V
Maximum output voltage	V <sub>OUT</sub> max	BLK1, BLK2, CHA1, CHA2, P0 to P3, CK <sub>OUT</sub>	$V_{SS} - 0.3 \text{ to } V_{DD} + 0.3$	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	Topr		-30 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

# Allowable Operating Ranges at $Ta = -30 \text{ to } +70^{\circ}\text{C}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V <sub>DD</sub>	$V_{DD}$	4.5	5.0	5.5	V
Input high-level voltage	V <sub>IH</sub>	RST, CS, SIN, SCLK, HSYNC, VSYNC	0.8 V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
Input low-level voltage	V <sub>IL</sub>	RST, CS, SIN, SCLK, HSYNC, VSYNC	V <sub>SS</sub> - 0.3		0.2 V <sub>DD</sub>	V
Oscillator frequency	fosc	OSC <sub>IN</sub> and OSC <sub>OUT</sub> oscillator pins	5	7	10	MHz

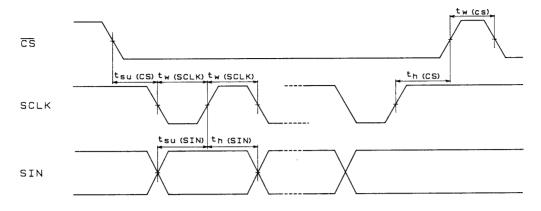
# Electrical Characteristics at Ta = -30 to $+70^{\circ}C$ , $V_{DD}$ = 5 V unless otherwise specified.

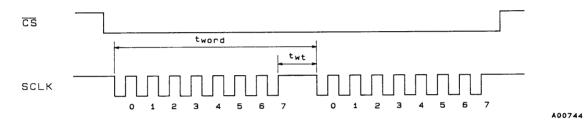
Parameter	Symbol	Conditions	min	typ	max	Unit
Output high-level voltage	V <sub>OH</sub>	BLK1, BLK2, CHA1, CHA2, P0 to P3: $V_{DD}$ = 5.0 V, $I_{OH}$ = -1.0 mA	4.5			V
Output low-level voltage	V <sub>OL</sub>	BLK1, BLK2, CHA1, CHA2, P0 to P3: $V_{DD}$ = 5.0 V, $I_{OL}$ = 1.0 mA			0.5	V
Input current	I <sub>IH</sub>	$\overline{\text{RST}}$ , $\overline{\text{CS}}$ , SIN, SCLK, $\overline{\text{HSYNC}}$ , $\overline{\text{VSYNC}}$ : $V_{\text{IN}} = V_{\text{DD}}$			1	μΑ
Input current	I <sub>IL</sub>	$\overline{\text{HSYNC}}$ , $\overline{\text{VSYNC}}$ : $V_{\text{IN}} = V_{\text{SS}}$	-1			μΑ
Operating current drain	I <sub>DD</sub>	V <sub>DD</sub> : all outputs open, LC = 7 MHz			10	mA

# Timing Characteristics at $Ta = -30~to~+70^{\circ}C,~V_{DD} = 5 \pm 0.5~V$

Parameter	Symbol	Conditions	min	typ	max	Unit
Minimum input pulse width	tw (SCLK)	SCLK	200			ns
wiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiii	t <sub>W</sub> (CS)	CS (the period that CS is high)	1			μs
Data setup time	t <sub>SU (CS)</sub>	<u>CS</u>	200			ns
Data Setup time	t <sub>SU (SIN)</sub>	SIN	200			ns
Data hold time	t <sub>h (CS)</sub>	CS	2			μs
Data fiold time	t <sub>h (SIN)</sub>	SIN	200			ns
Single word write time	t <sub>word</sub>	The time to write 8 bits of data	4.2			μs
Single word write time	t <sub>wt</sub>	The time to write RAM data	1			μs

# **Serial Data Input Timing**

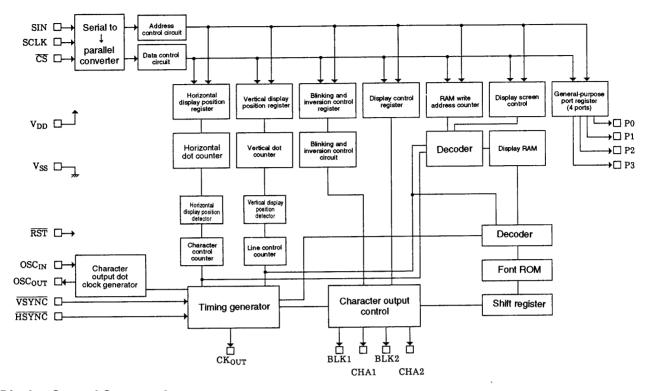




# **Pin Functions**

No.	Symbol	Pin	Function
1	V <sub>SS</sub>	Ground pin	Ground connection
2	OSC <sub>IN</sub>	LC oscillator pin	Connections for the coil and capacitor that form the oscillator that generates the character output
3	OSC <sub>OUT</sub>	LC oscillator pin	dot clock.
4	CK <sub>OUT</sub> /TEST	Clock output/test output pin	Provides the OSC <sub>OUT</sub> output (when $\overline{\text{RST}}$ is low) and the test mode output.
5	P0	General-purpose port 0 output pin	General-purpose port (PORT0) output
6	P1	General-purpose port 1 output pin	General-purpose port (PORT1) output
7	<del>CS</del>	Enable input pin	Enable input for the serial data input function. Serial data input is enabled when this pin is low. A pull-up resistor is built in, i.e., this is a hysteresis input.
8	SCLK	Clock input pin	Clock input for the serial data input function. A pull-up resistor is built in, i.e., this is a hysteresis input.
9	SIN	Data input pin	Serial data input. A pull-up resistor is built in, i.e., this is a hysteresis input.
10	V <sub>SS</sub>	Ground pin	Ground connection
11	NC	No connection	
12	NC	No connection	Unused pins.
13	NC	No connection	These pins must be left open or connected to ground.
14	NC	No connection	
15	CHA1	Character 1 output pin	System 1 character data output
16	BLK1	Blank 1 output pin	System 1 blank data output
17	CHA2	Character 2 output pin	System 2 character data output
18	BLK2	Blank 2 output pin	System 2 blank data output
19	P3	General-purpose port 3 output pin	General-purpose port (PORT3) output
20	P2	General-purpose port 2 output pin	General-purpose port (PORT2) output
21	VSYNC	Vertical synchronizing signal input pin	Input for the vertical synchronizing signal (active low)
22	HSYNC	Horizontal synchronizing signal input pin	Input for the horizontal synchronizing signal (active low)
23	RST	Reset input pin	System reset input (active low) A pull-up resistor is built in, i.e., this is a hysteresis input.
24	V <sub>DD</sub>	Power supply pin (+5 V)	Power supply (+5 V)

#### **Block Diagram**



#### **Display Control Commands**

Display control commands have an 8-bit format and are transferred using the serial input function. Commands consist of a command identification code in the first byte and command data in the following bytes. The following commands are supported.

- 1 COMMAND 0: Display memory (VRAM) write address setup command
- 2 COMMAND 1: Display character data write command
- 3 COMMAND 2: Vertical display start position and vertical character size setup command
- 4 COMMAND 3: Horizontal display start position and horizontal character size setup command
- 5 COMMAND 4: Display control setup command
- 6 COMMAND 5: System 2 (BLK2 and CHA2) output control (lines 1 to 6) and line size setting command
- 7 COMMAND 6: System 2 (BLK2 and CHA2) output control (lines 7 to 12) and general-purpose port setting command

## **Display Control Command Table**

				First	byte							Secon	d byte			
Command	Comm	and ide	ntificatio	n code		Da	ata					Da	ıta			
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND 0 Write address	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	НЗ	H2	H1	НО
COMMAND 1 Character write	1	0	0	1	0	0	0	0	at	c6	c5	c4	с3	c2	c1	c0
COMMAND 2 Vertical display position start position	1	0	1	0	0	0	0	0	0	0	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND 3 Horizontal display position start position	1	0	1	1	0	0	0	0	0	0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND 4 Display control	1	1	0	0	TST	RCL	osc	RST	0	MD1	MD0	EG	BK 1	BK 0	RV	DSP
COMMAND 5 BLK2 and CHA2 output control: lines 1 to 6, and line size control	1	1	0	1	0	0	0	LS	0	0	LN 6	LN 5	LN 4	LN 3	LN 2	LN 1
COMMAND 6 BLK2 and CHA2 output control: lines 7 to 12, and general-purpose port control	1	1	1	0	P3	P2	P1	P0	0	0	LN 12	LN 11	LN 10	LN 9	LN 8	LN 7

Once written, the command identification code in the first byte is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74770M locks into the display character data write mode, and another first byte cannot be written.

When a high level is input to the  $\overline{\text{CS}}$  pin, the LC74770M is set to COMMAND0 (display memory write address setup mode).

#### 1 COMMAND 0 (Display memory write address setup command)

#### First byte

DAG 1 DA 7	5		Register content	N .	
DAU to DA7	DA0 to DA7 Register name		Function	Note	
7	_	1			
6	_	0	Command 0 identification code		
5	_	0	Sets the display memory write address.		
4		0			
3	V3	V2 0			
3	V3	1			
2	V2	0			
2	VZ	1	Display memory address (0 to B hexadecimal)		
1	V1	0	Display memory address (o to b nexadecimal)		
'	V I	1			
0	VO	0			
0 0	1				

# Second byte

DAG: DA7	<b>D</b>		Register content	N.			
DA0 to DA7	Register name	State	Function	Note			
7	_	0	Second byte identification bit				
6	_	0					
5	_	0					
4	H4	0					
4	Π4	1					
3	H3	0					
3	пз	ПЗ	113	113	1		
2	110	H2	0	Display memory address (0 to 17 hexadecimal)			
2	112	1	Display memory address (0 to 17 nexadecimal)				
1	1 H1	0					
1		1					
0	H0	0					
0 Н0	1						

Note: All registers are set to 0 when the LC74770M is reset by the RST pin.

# 2 COMMAND 1 (Display character data write setup command)

# First byte

B40. B45	DAG ( DA7   D		Register content	
DA0 to DA7	Register name	State	Function	Note
7	_	1		When this command is input, the
6	_	0	Command 1 identification code	LC74770M locks into the display
5	_	0	Sets up display character data write.	character data write mode until the CS
4	_	1		pin goes high.
3	_	0		
2	_	0		
1	_	0		
0		0		

# Second byte

DAG ( DA7	5		Register content	N	
DA0 to DA7 Register name		State	Function	Note	
7	- t	0	Character attribute off		
,	at	1	Character attribute on		
6	-6	0			
6	c6	1			
5	c5	0			
5	Co	1			
4	c4	0			
4		C4	C4	1	
3	2 22	0	Character gode (00 to 75 heyodesimal)		
3	c3	1	Character code (00 to 7F hexadecimal)		
2	c2	0			
2	62	1			
1		0			
'	c1	1			
0	c0	0			
0		1			

Note: All registers are set to 0 when the LC74770M is reset by the  $\overline{\text{RST}}$  pin.

# 3 COMMAND 2 (Vertical display start position setup command)

## First byte

DAG / DA7	. 547		Register content	
DA0 to DA7	Register name	State	Function	Note
7	_	1		
6	_	0	Command 2 identification code	
5	_	1	Sets the vertical display start position.	
4	_	0		
3	_	0		
2	_	0		
1	_	0		
0	_	0		

## Second byte

DAG 1 DA 7	B		Register content	N.,
DA0 to DA7	Register name	State	Function	Note
7	_	0	Second byte identification bit	
6	_	0		
-	VP5	0	If VS is the vertical display start position then:	
5	(MSB)	1	$VS = H \times (5 \atop n = 0 \atop n = 0 \atop n = 0$	
4	VP4	0		
4	VF4	1	H: the horizontal synchronization pulse period	
3	VP3	0	HSYNC	
3	VP3	1		The vertical display start position is set by the 6 bits VP0 to VP5.
2	VP2	0	]	The weight of bit 1 is 1H.
2	VFZ	1	VS	The weight of bit 1 is 11.
1	VP1	0	VSYNC	
	VEI	1	Character	
0	VP0	0	HS display area	
	(LSB)	1		

Note: All registers are set to 0 when the LC74770M is reset by the RST pin.

# 4 COMMAND 3 (Horizontal display start position setup command)

# First byte

DAG ( DA7	Register name	Register content		
DA0 to DA7		State	Function	Note
7		1		
6		0	Command 3 identification code	
5	_	1	Sets the horizontal display start position.	
4	_	1		
3		0		
2		0		
1	_	0		
0	_	0		

# Second byte

	5	Register content		
DA0 to DA7	Register name	State	Function	Note
7	_	0	Second byte identification bit	
6	_	0		
5	HP5	0		
5	(MSB)	1		
4	HP4	0		
4	ПР4	1		
3	HP3	0	If HS is the horizontal start position then:	
3		1	HS = $Tc \times (\sum_{n=0}^{5} 2^{n}HP_{n})$	The horizontal display start position is set by the 6 bits HP0 to HP5.
2	HP2	0	Tc: Period of the oscillator connected to OSC <sub>IN</sub> /OSC <sub>OLIT</sub> in	The weight of bit 1 is 1Tc.
2		1	operating mode.	The weight of bit 1 to 110.
1	HP1	0		
'	11121	1		
0	HP0	0		
U	(LSB)	1		

Note: All registers are set to 0 when the LC74770M is reset by the  $\overline{RST}$  pin.

# 5 COMMAND 4 (Display control setup command)

# First byte

DA0 4- DA7	Register name	Register content							
DA0 to DA7		State	Function	Note					
7	_	1							
6	_	1	Command 4 identification code						
5	_	0	Sets up display control.						
4	_	0							
3	TST	0	Normal operating mode	This bit must be zero.					
3	(TSTMOD)	1	Test mode	This bit must be zero.					
2	RCL	0		Valid when display is off					
2	(RAMCLR)	1	Erase display RAM (Data is set to 7F hexadecimal.)	Valid when display is off.					
4	OSC (OSCSTP)	OSC	OSC	OSC	OSC	OSC	0	Do not stop the LC oscillator circuit.	This bit must be zero.
'		1	Stop the LC oscillator circuit.	This bit must be zero.					
0	RST (SYSRST)	RST	RST 0	0		The LSI is reset when the $\overline{CS}$ pin is low, and the reset is cleared when that pin			
U		1	Reset all registers and turn the display off.	goes high.					

# Second byte

DA0 to DA7	Register name	Register content			
		State	Function	Note	
7	_	0	Second byte identification bit		
6		0	The blank output also outputs character data.	Plants sustaint soutral	
б	MD1	1	The blank output only outputs blank data.	Blank output control	
5	MDo	0	The system 1 output outputs all lines.	Output quaters 1 control	
5	MD0	1	The system 1 output only outputs lines not output by system 2.	Output system 1 control	
4	EG	0	Border off		
4	EG	1	Border on		
3	BK1	0	Blinking period set to about 0.5 second.	Plinking period switching	
3		1	Blinking period set to about 1 second.	Blinking period switching	
2	DICO	BK0	0	Blinking off	Blinking of reverse video characters consists of alternation between normal
2	BNU	1	Blinking on	and reverse video.	
4	RV	0	Reverse video off		
'		1	Reverse video on		
0	DSP (DSPON)	0	Character display off		
		1	Character display on		

Note: All registers are set to 0 when the LC74770M is reset by the RST pin.

# 6 COMMAND 5 (System 2 output control and line size setting command)

# First byte

DAG ( DA7	Register name	Register content		N	
DA0 to DA7		State	Function	Note	
7	_	1	Command 5 identification code Controls output system 2 and sets the line size. (Output control for CHA2 and BLK2)		
6	_	1			
5	_	0			
4	_	1	(Line size control)		
3	_	0			
2	_	0			
1	_	0			
0	LS	1.6	0 Output	Output line selection	The line is selected in the second byte.
		1	Character size selection (line units)	The line is selected in the second byte.	

# Second byte

DAG: DAZ   D ::		Register content				
DA0 to DA7	Register name	State	Function	Note		
7	_	0	Second byte identification bit			
6	_	0				
5	LN6	0	The sixth line of data is not output to CHA2 and BLK2.			
5	LINO	1	The sixth line of data is output to CHA2 and BLK2.			
4	LN5	0	The fifth line of data is not output to CHA2 and BLK2.			
4	LINO	1	The fifth line of data is output to CHA2 and BLK2.	Used for the line output setting when LS		
3	LN4	1.014	0	The fourth line of data is not output to CHA2 and BLK2.	is low. Used for the line size setting when LS is	
3		1	The fourth line of data is output to CHA2 and BLK2.	high.		
2	LN3	0	The third line of data is not output to CHA2 and BLK2.	Nata		
2	LINO	1	The third line of data is output to CHA2 and BLK2.	Note: LS = 1: Set the line size.		
4	1 LN2	LNO	LNO	0	The second line of data is not output to CHA2 and BLK2.	LS = 0: Specifies line output.
'		1	The second line of data is output to CHA2 and BLK2.			
0	LN1	0	The first line of data is not output to CHA2 and BLK2.			
0		1	The first line of data is output to CHA2 and BLK2.			

Note: All registers are set to 0 when the LC74770M is reset by the  $\overline{RST}$  pin.

# 7 COMMAND 6 (System 2 output control and general-purpose port setting command)

## First byte

DA0 to DA7	Register name	Register content			
		State	Function	Note	
7	_	1	Command 6 identification code		
6	_	1	Controls output system 2 output.		
5	_	1	(Output control for CHA2 and BLK2)		
4	_	0	(General-purpose port output control)		
3	P3	0	Sets the general-purpose port output (P3) to low.		
3		1	Sets the general-purpose port output (P3) to high.		
2	P2	0	Sets the general-purpose port output (P2) to low.		
2		1	Sets the general-purpose port output (P2) to high.		
1	P1	D4	0	Sets the general-purpose port output (P1) to low.	
'		1	Sets the general-purpose port output (P1) to high.		
0	P0	0	Sets the general-purpose port output (P0) to low.		
0		1	Sets the general-purpose port output (P0) to high.		

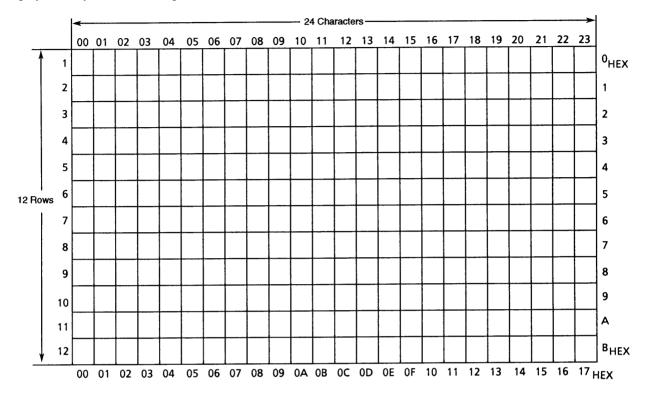
# Second byte

DAGE DATE DE LE		Register content							
DA0 to DA7	Register name	State	Function	Note					
7	_	0	Second byte identification bit						
6	_	0							
5	LN12	0	The twelfth line of data is not output to CHA2 and BLK2.						
5	LINIZ	1	The twelfth line of data is output to CHA2 and BLK2.						
4	LN11	0	The eleventh line of data is not output to CHA2 and BLK2.						
4	LINII	1	The eleventh line of data is output to CHA2 and BLK2.	Used for the line output setting when LS					
3	LN10	1.014.0	L N/4.0	1.0140	LNIIO	1 N40	0	The tenth line of data is not output to CHA2 and BLK2.	is low. Used for the line size setting when LS is
3		1	The tenth line of data is output to CHA2 and BLK2.	high.					
2	LN9	0	The ninth line of data is not output to CHA2 and BLK2.	Note:					
2	LIN9	1	The ninth line of data is output to CHA2 and BLK2.	LS = 1: Set the line size.					
4	1.10	1.010	LNIO	LNO	LN8	0	The eighth line of data is not output to CHA2 and BLK2.	LS = 0: Specifies line output.	
'	LINO	1	The eighth line of data is output to CHA2 and BLK2.						
0	LN7	0	The seventh line of data is not output to CHA2 and BLK2.						
0		1	The seventh line of data is output to CHA2 and BLK2.						

Note: All registers are set to 0 when the LC74770M is reset by the RST pin.

#### **Display Screen Structure**

The display consists of 12 lines of 24 characters each and thus up to 288 characters can be displayed. Display memory addresses are specified as row (0 to B hexadecimal) and column (0 to 17 hexadecimal) addresses.



**Display Screen Structure (display memory addresses)** 

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
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