Ordering number : EN4248A

CMOS LSI

# LC74770M

## On-Screen Display Controller LSI

## Overview

The LC74770M is a CMOS LSI that implements on-screen display, a function that displays characters and patterns on display screens such as camcorder viewfinder screens under microprocessor control. This LSI displays 12-dot by 18-dot characters.

## Features

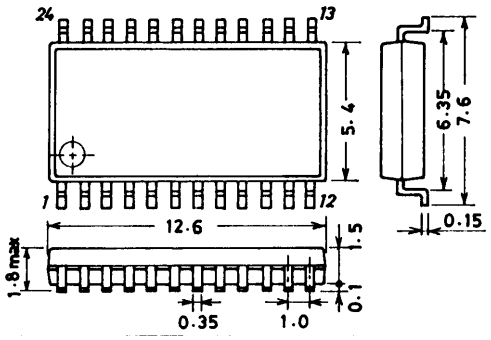
- Display format: 24 characters by 12 rows (up to 288 characters)
- Characters displayed: Up to 288 characters
- Character format: 12 (horizontal) × 18 (vertical)
- Characters in font: 128
- Character sizes: Normal and double
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Reverse video function: Characters can be displayed in reverse video specified in units of individual characters.
- Blinking types: In character units in one of two periods, 1.0 second and 0.5 second, with a 50% duty.
- Outputs: Character and blanking data, with two output systems for each
- External control input: 8-bit serial input format
- General-purpose output port: 4 bits (controlled from the serial input data)

## Package Dimensions

unit: mm

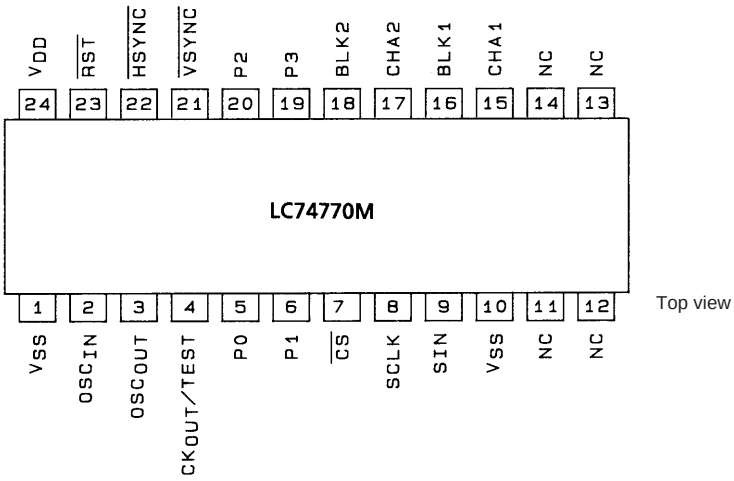
**3112-MFP24S**

[LC74770M]




SANYO: MFP24S

### Pin Assignment




Top view

# Specifications

## Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}$ | $V_{SS}$ – 0.3 to $V_{SS}$ + 7.0 | V |
| Maximum input voltage | $V_{IN}$ max | All input pins | $V_{SS}$ – 0.3 to $V_{DD}$ + 0.3 | V |
| Maximum output voltage | $V_{OUT}$ max | BLK1, BLK2, CHA1, CHA2, P0 to P3, $CK_{OUT}$ | $V_{SS}$ – 0.3 to $V_{DD}$ + 0.3 | V |
| Allowable power dissipation | Pd max | | 300 | mW |
| Operating temperature | Topr | | –30 to +70 | °C |
| Storage temperature | Tstg | | –40 to +125 | °C |

## Allowable Operating Ranges at Ta = –30 to +70°C

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ | 4.5 | 5.0 | 5.5 | V |
| Input high-level voltage | $V_{IH}$ | $\overline{RST}$, $\overline{CS}$, SIN, SCLK, $\overline{HSYNC}$, $\overline{VSYNC}$ | 0.8 $V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| Input low-level voltage | $V_{IL}$ | $\overline{RST}$, $\overline{CS}$, SIN, SCLK, $\overline{HSYNC}$, $\overline{VSYNC}$ | $V_{SS}$ – 0.3 | | 0.2 $V_{DD}$ | V |
| Oscillator frequency | $f_{OSC}$ | $OSC_{IN}$ and $OSC_{OUT}$ oscillator pins | 5 | 7 | 10 | MHz |

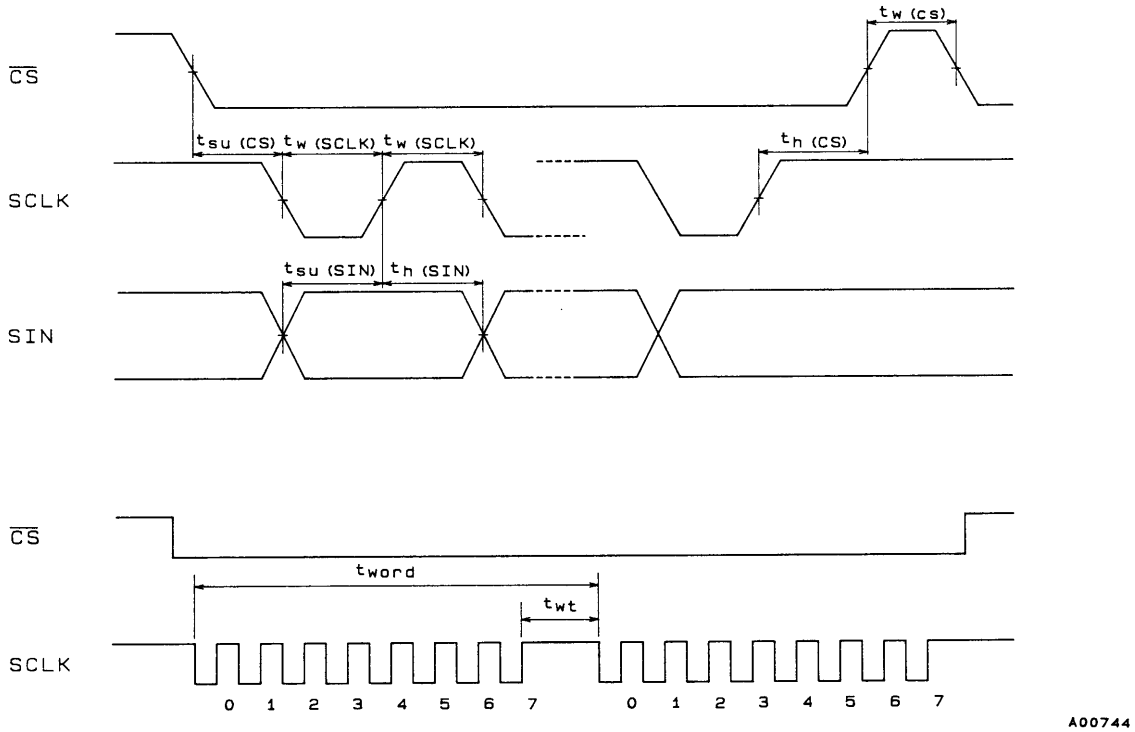
## Electrical Characteristics at Ta = –30 to +70°C, $V_{DD}$ = 5 V unless otherwise specified.

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output high-level voltage | $V_{OH}$ | BLK1, BLK2, CHA1, CHA2, P0 to P3: $V_{DD}$ = 5.0 V, $I_{OH}$ = –1.0 mA | 4.5 | | | V |
| Output low-level voltage | $V_{OL}$ | BLK1, BLK2, CHA1, CHA2, P0 to P3: $V_{DD}$ = 5.0 V, $I_{OL}$ = 1.0 mA | | | 0.5 | V |
| Input current | $I_{IH}$ | $\overline{RST}$, $\overline{CS}$, SIN, SCLK, $\overline{HSYNC}$, $\overline{VSYNC}$: $V_{IN}$ = $V_{DD}$ | | | 1 | µA |
| | $I_{IL}$ | $\overline{HSYNC}$, $\overline{VSYNC}$: $V_{IN}$ = $V_{SS}$ | –1 | | | µA |
| Operating current drain | $I_{DD}$ | $V_{DD}$: all outputs open, LC = 7 MHz | | | 10 | mA |

## Timing Characteristics at Ta = –30 to +70°C, $V_{DD}$ = 5 ± 0.5 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Minimum input pulse width | $t_{W\ (SCLK)}$ | SCLK | 200 | | | ns |
| | $t_{W\ (CS)}$ | $\overline{CS}$ (the period that $\overline{CS}$ is high) | 1 | | | µs |
| Data setup time | $t_{SU\ (CS)}$ | $\overline{CS}$ | 200 | | | ns |
| | $t_{SU\ (SIN)}$ | SIN | 200 | | | ns |
| Data hold time | $t_{h\ (CS)}$ | $\overline{CS}$ | 2 | | | µs |
| | $t_{h\ (SIN)}$ | SIN | 200 | | | ns |
| Single word write time | $t_{word}$ | The time to write 8 bits of data | 4.2 | | | µs |
| | $t_{wt}$ | The time to write RAM data | 1 | | | µs |

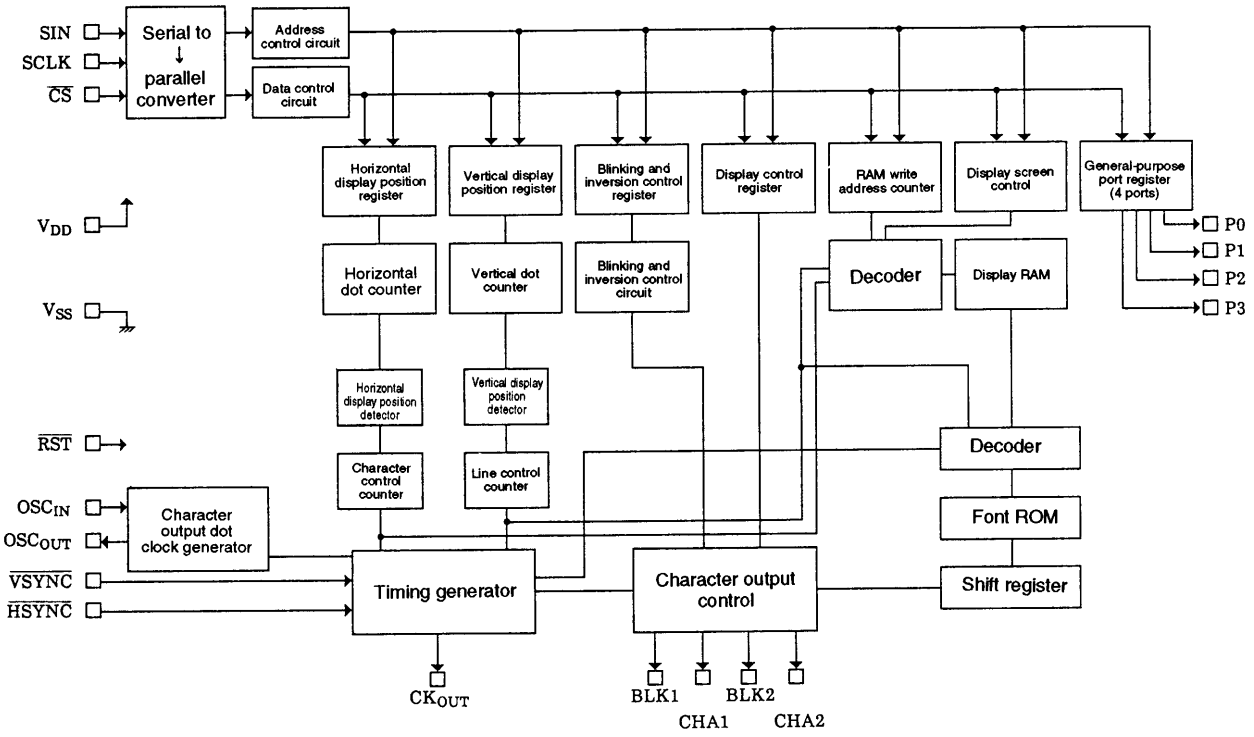
## Serial Data Input Timing




## Pin Functions

| No. | Symbol | Pin | Function |
|---|---|---|---|
| 1 | $V_{SS}$ | Ground pin | Ground connection |
| 2 | $OSC_{IN}$ | LC oscillator pin | Connections for the coil and capacitor that form the oscillator that generates the character output dot clock. |
| 3 | $OSC_{OUT}$ | | |
| 4 | $CK_{OUT}$/TEST | Clock output/test output pin | Provides the $OSC_{OUT}$ output (when $\overline{RST}$ is low) and the test mode output. |
| 5 | P0 | General-purpose port 0 output pin | General-purpose port (PORT0) output |
| 6 | P1 | General-purpose port 1 output pin | General-purpose port (PORT1) output |
| 7 | $\overline{CS}$ | Enable input pin | Enable input for the serial data input function. Serial data input is enabled when this pin is low. A pull-up resistor is built in, i.e., this is a hysteresis input. |
| 8 | SCLK | Clock input pin | Clock input for the serial data input function. A pull-up resistor is built in, i.e., this is a hysteresis input. |
| 9 | SIN | Data input pin | Serial data input. A pull-up resistor is built in, i.e., this is a hysteresis input. |
| 10 | $V_{SS}$ | Ground pin | Ground connection |
| 11 | NC | No connection | Unused pins. These pins must be left open or connected to ground. |
| 12 | NC | No connection | |
| 13 | NC | No connection | |
| 14 | NC | No connection | |
| 15 | CHA1 | Character 1 output pin | System 1 character data output |
| 16 | BLK1 | Blank 1 output pin | System 1 blank data output |
| 17 | CHA2 | Character 2 output pin | System 2 character data output |
| 18 | BLK2 | Blank 2 output pin | System 2 blank data output |
| 19 | P3 | General-purpose port 3 output pin | General-purpose port (PORT3) output |
| 20 | P2 | General-purpose port 2 output pin | General-purpose port (PORT2) output |
| 21 | $\overline{VSYNC}$ | Vertical synchronizing signal input pin | Input for the vertical synchronizing signal (active low) |
| 22 | $\overline{HSYNC}$ | Horizontal synchronizing signal input pin | Input for the horizontal synchronizing signal (active low) |
| 23 | $\overline{RST}$ | Reset input pin | System reset input (active low) A pull-up resistor is built in, i.e., this is a hysteresis input. |
| 24 | $V_{DD}$ | Power supply pin (+5 V) | Power supply (+5 V) |

## Block Diagram




## Display Control Commands

Display control commands have an 8-bit format and are transferred using the serial input function. Commands consist of a command identification code in the first byte and command data in the following bytes. The following commands are supported.

1 COMMAND 0: Display memory (VRAM) write address setup command
2 COMMAND 1: Display character data write command
3 COMMAND 2: Vertical display start position and vertical character size setup command
4 COMMAND 3: Horizontal display start position and horizontal character size setup command
5 COMMAND 4: Display control setup command
6 COMMAND 5: System 2 (BLK2 and CHA2) output control (lines 1 to 6) and line size setting command
7 COMMAND 6: System 2 (BLK2 and CHA2) output control (lines 7 to 12) and general-purpose port setting command

## Display Control Command Table

| Command | First byte | | | | | | | | Second byte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Command identification code | | | | Data | | | | Data | | | | | | | |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND 0<br>Write address | 1 | 0 | 0 | 0 | V3 | V2 | V1 | V0 | 0 | 0 | 0 | H4 | H3 | H2 | H1 | H0 |
| COMMAND 1<br>Character write | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | at | c6 | c5 | c4 | c3 | c2 | c1 | c0 |
| COMMAND 2<br>Vertical display position start position | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 |
| COMMAND 3<br>Horizontal display position start position | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 |
| COMMAND 4<br>Display control | 1 | 1 | 0 | 0 | TST | RCL | OSC | RST | 0 | MD1 | MD0 | EG | BK1 | BK0 | RV | DSP |
| COMMAND 5<br>BLK2 and CHA2 output control: lines 1 to 6, and line size control | 1 | 1 | 0 | 1 | 0 | 0 | 0 | LS | 0 | 0 | LN6 | LN5 | LN4 | LN3 | LN2 | LN1 |
| COMMAND 6<br>BLK2 and CHA2 output control: lines 7 to 12, and general-purpose port control | 1 | 1 | 1 | 0 | P3 | P2 | P1 | P0 | 0 | 0 | LN12 | LN11 | LN10 | LN9 | LN8 | LN7 |

Once written, the command identification code in the first byte is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74770M locks into the display character data write mode, and another first byte cannot be written.
When a high level is input to the $\overline{CS}$ pin, the LC74770M is set to COMMAND0 (display memory write address setup mode).

1 COMMAND 0 (Display memory write address setup command)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 1 | Command 0 identification code<br>Sets the display memory write address. | |
| 6 | — | 0 | | |
| 5 | — | 0 | | |
| 4 | — | 0 | | |
| 3 | V3 | 0 | Display memory address (0 to B hexadecimal) | |
| | | 1 | | |
| 2 | V2 | 0 | | |
| | | 1 | | |
| 1 | V1 | 0 | | |
| | | 1 | | |
| 0 | V0 | 0 | | |
| | | 1 | | |

Second byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 0 | Second byte identification bit | |
| 6 | — | 0 | | |
| 5 | — | 0 | | |
| 4 | H4 | 0 | Display memory address (0 to 17 hexadecimal) | |
| | | 1 | | |
| 3 | H3 | 0 | | |
| | | 1 | | |
| 2 | H2 | 0 | | |
| | | 1 | | |
| 1 | H1 | 0 | | |
| | | 1 | | |
| 0 | H0 | 0 | | |
| | | 1 | | |

Note: All registers are set to 0 when the LC74770M is reset by the RST pin.

## 2 COMMAND 1 (Display character data write setup command)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 1 | Command 1 identification code<br>Sets up display character data write. | When this command is input, the LC74770M locks into the display character data write mode until the $\overline{CS}$ pin goes high. |
| 6 | — | 0 | | |
| 5 | — | 0 | | |
| 4 | — | 1 | | |
| 3 | — | 0 | | |
| 2 | — | 0 | | |
| 1 | — | 0 | | |
| 0 | — | 0 | | |

Second byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | at | 0 | Character attribute off | |
| | | 1 | Character attribute on | |
| 6 | c6 | 0 | Character code (00 to 7F hexadecimal) | |
| | | 1 | | |
| 5 | c5 | 0 | | |
| | | 1 | | |
| 4 | c4 | 0 | | |
| | | 1 | | |
| 3 | c3 | 0 | | |
| | | 1 | | |
| 2 | c2 | 0 | | |
| | | 1 | | |
| 1 | c1 | 0 | | |
| | | 1 | | |
| 0 | c0 | 0 | | |
| | | 1 | | |

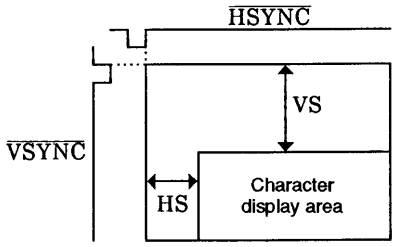
Note: All registers are set to 0 when the LC74770M is reset by the $\overline{RST}$ pin.

## 3 COMMAND 2 (Vertical display start position setup command)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 1 | Command 2 identification code<br>Sets the vertical display start position. | |
| 6 | — | 0 | | |
| 5 | — | 1 | | |
| 4 | — | 0 | | |
| 3 | — | 0 | | |
| 2 | — | 0 | | |
| 1 | — | 0 | | |
| 0 | — | 0 | | |

Second byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 0 | Second byte identification bit | |
| 6 | — | 0 | | |
| 5 | VP5 (MSB) | 0 | If VS is the vertical display start position then:<br>$VS = H \times (\sum_{n=0}^{5} 2^n VP_n)$<br>H: the horizontal synchronization pulse period<br>  <br> | The vertical display start position is set by the 6 bits VP0 to VP5.<br>The weight of bit 1 is 1H. |
| | | 1 | | |
| 4 | VP4 | 0 | | |
| | | 1 | | |
| 3 | VP3 | 0 | | |
| | | 1 | | |
| 2 | VP2 | 0 | | |
| | | 1 | | |
| 1 | VP1 | 0 | | |
| | | 1 | | |
| 0 | VP0 (LSB) | 0 | | |
| | | 1 | | |

Note: All registers are set to 0 when the LC74770M is reset by the $\overline{RST}$ pin.

## 4 COMMAND 3 (Horizontal display start position setup command)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 1 | Command 3 identification code<br>Sets the horizontal display start position. | |
| 6 | — | 0 | | |
| 5 | — | 1 | | |
| 4 | — | 1 | | |
| 3 | — | 0 | | |
| 2 | — | 0 | | |
| 1 | — | 0 | | |
| 0 | — | 0 | | |

Second byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 0 | Second byte identification bit | |
| 6 | — | 0 | | |
| 5 | HP5 (MSB) | 0 | If HS is the horizontal start position then:<br>$HS = Tc \times (\sum_{n=0}^{5} 2^n HP_n)$<br>Tc: Period of the oscillator connected to $OSC_{IN}/OSC_{OUT}$ in operating mode. | The horizontal display start position is set by the 6 bits HP0 to HP5.<br>The weight of bit 1 is 1Tc. |
| | | 1 | | |
| 4 | HP4 | 0 | | |
| | | 1 | | |
| 3 | HP3 | 0 | | |
| | | 1 | | |
| 2 | HP2 | 0 | | |
| | | 1 | | |
| 1 | HP1 | 0 | | |
| | | 1 | | |
| 0 | HP0 (LSB) | 0 | | |
| | | 1 | | |

Note: All registers are set to 0 when the LC74770M is reset by the $\overline{RST}$ pin.

## 5 COMMAND 4 (Display control setup command)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 1 | Command 4 identification code<br>Sets up display control. | |
| 6 | — | 1 | | |
| 5 | — | 0 | | |
| 4 | — | 0 | | |
| 3 | TST (TSTMOD) | 0 | Normal operating mode | This bit must be zero. |
| | | 1 | Test mode | |
| 2 | RCL (RAMCLR) | 0 | | Valid when display is off. |
| | | 1 | Erase display RAM (Data is set to 7F hexadecimal.) | |
| 1 | OSC (OSCSTP) | 0 | Do not stop the LC oscillator circuit. | This bit must be zero. |
| | | 1 | Stop the LC oscillator circuit. | |
| 0 | RST (SYSRST) | 0 | | The LSI is reset when the $\overline{CS}$ pin is low, and the reset is cleared when that pin goes high. |
| | | 1 | Reset all registers and turn the display off. | |

Second byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 0 | Second byte identification bit | |
| 6 | MD1 | 0 | The blank output also outputs character data. | Blank output control |
| | | 1 | The blank output only outputs blank data. | |
| 5 | MD0 | 0 | The system 1 output outputs all lines. | Output system 1 control |
| | | 1 | The system 1 output only outputs lines not output by system 2. | |
| 4 | EG | 0 | Border off | |
| | | 1 | Border on | |
| 3 | BK1 | 0 | Blinking period set to about 0.5 second. | Blinking period switching |
| | | 1 | Blinking period set to about 1 second. | |
| 2 | BK0 | 0 | Blinking off | Blinking of reverse video characters consists of alternation between normal and reverse video. |
| | | 1 | Blinking on | |
| 1 | RV | 0 | Reverse video off | |
| | | 1 | Reverse video on | |
| 0 | DSP (DSPON) | 0 | Character display off | |
| | | 1 | Character display on | |

Note: All registers are set to 0 when the LC74770M is reset by the $\overline{\text{RST}}$ pin.

## 6 COMMAND 5 (System 2 output control and line size setting command)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 1 | Command 5 identification code<br>Controls output system 2 and sets the line size.<br>(Output control for CHA2 and BLK2)<br>(Line size control) | |
| 6 | — | 1 | | |
| 5 | — | 0 | | |
| 4 | — | 1 | | |
| 3 | — | 0 | | |
| 2 | — | 0 | | |
| 1 | — | 0 | | |
| 0 | LS | 0 | Output line selection | The line is selected in the second byte. |
| | | 1 | Character size selection (line units) | |

Second byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 0 | Second byte identification bit | |
| 6 | — | 0 | | |
| 5 | LN6 | 0 | The sixth line of data is not output to CHA2 and BLK2. | Used for the line output setting when LS is low.<br>Used for the line size setting when LS is high.<br><br>Note:<br>LS = 1: Set the line size.<br>LS = 0: Specifies line output. |
| | | 1 | The sixth line of data is output to CHA2 and BLK2. | |
| 4 | LN5 | 0 | The fifth line of data is not output to CHA2 and BLK2. | |
| | | 1 | The fifth line of data is output to CHA2 and BLK2. | |
| 3 | LN4 | 0 | The fourth line of data is not output to CHA2 and BLK2. | |
| | | 1 | The fourth line of data is output to CHA2 and BLK2. | |
| 2 | LN3 | 0 | The third line of data is not output to CHA2 and BLK2. | |
| | | 1 | The third line of data is output to CHA2 and BLK2. | |
| 1 | LN2 | 0 | The second line of data is not output to CHA2 and BLK2. | |
| | | 1 | The second line of data is output to CHA2 and BLK2. | |
| 0 | LN1 | 0 | The first line of data is not output to CHA2 and BLK2. | |
| | | 1 | The first line of data is output to CHA2 and BLK2. | |

Note: All registers are set to 0 when the LC74770M is reset by the $\overline{\text{RST}}$ pin.

## 7 COMMAND 6 (System 2 output control and general-purpose port setting command)

### First byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 1 | Command 6 identification code<br>Controls output system 2 output.<br>(Output control for CHA2 and BLK2)<br>(General-purpose port output control) | |
| 6 | — | 1 | | |
| 5 | — | 1 | | |
| 4 | — | 0 | | |
| 3 | P3 | 0 | Sets the general-purpose port output (P3) to low. | |
| | | 1 | Sets the general-purpose port output (P3) to high. | |
| 2 | P2 | 0 | Sets the general-purpose port output (P2) to low. | |
| | | 1 | Sets the general-purpose port output (P2) to high. | |
| 1 | P1 | 0 | Sets the general-purpose port output (P1) to low. | |
| | | 1 | Sets the general-purpose port output (P1) to high. | |
| 0 | P0 | 0 | Sets the general-purpose port output (P0) to low. | |
| | | 1 | Sets the general-purpose port output (P0) to high. | |

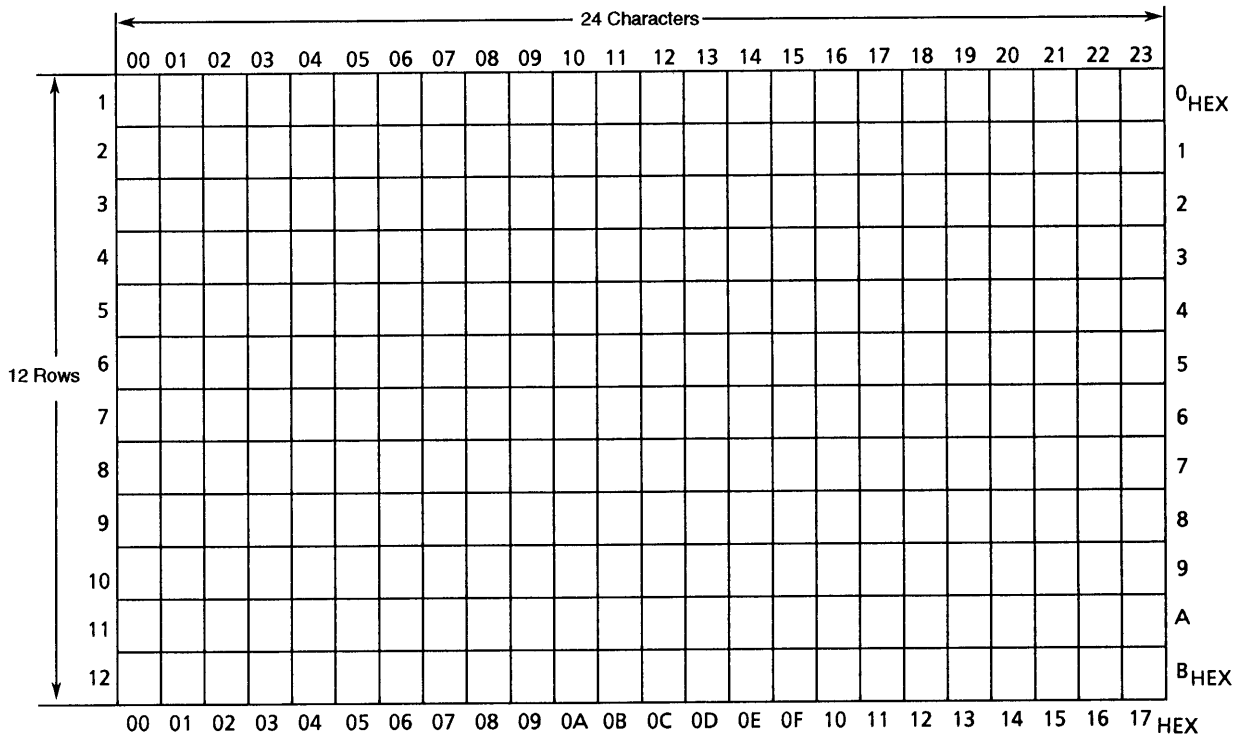
### Second byte

| DA0 to DA7 | Register name | Register content | | Note |
|---|---|---|---|---|
| | | State | Function | |
| 7 | — | 0 | Second byte identification bit | |
| 6 | — | 0 | | |
| 5 | LN12 | 0 | The twelfth line of data is not output to CHA2 and BLK2. | Used for the line output setting when LS is low.<br>Used for the line size setting when LS is high.<br><br>Note:<br>LS = 1: Set the line size.<br>LS = 0: Specifies line output. |
| | | 1 | The twelfth line of data is output to CHA2 and BLK2. | |
| 4 | LN11 | 0 | The eleventh line of data is not output to CHA2 and BLK2. | |
| | | 1 | The eleventh line of data is output to CHA2 and BLK2. | |
| 3 | LN10 | 0 | The tenth line of data is not output to CHA2 and BLK2. | |
| | | 1 | The tenth line of data is output to CHA2 and BLK2. | |
| 2 | LN9 | 0 | The ninth line of data is not output to CHA2 and BLK2. | |
| | | 1 | The ninth line of data is output to CHA2 and BLK2. | |
| 1 | LN8 | 0 | The eighth line of data is not output to CHA2 and BLK2. | |
| | | 1 | The eighth line of data is output to CHA2 and BLK2. | |
| 0 | LN7 | 0 | The seventh line of data is not output to CHA2 and BLK2. | |
| | | 1 | The seventh line of data is output to CHA2 and BLK2. | |

Note: All registers are set to 0 when the LC74770M is reset by the $\overline{\text{RST}}$ pin.

## Display Screen Structure

The display consists of 12 lines of 24 characters each and thus up to 288 characters can be displayed.
Display memory addresses are specified as row (0 to B hexadecimal) and column (0 to 17 hexadecimal) addresses.




**Display Screen Structure (display memory addresses)**