



Motion JPEG Decoder LSI

Preliminaly

Overview

The LC82220 is a single-chip JPEG decoder designed for wide range of digital video playback applications including amusement systems, video games and PC JPEG playback cards. The LC82220 is capable of decoding JPEG bitstreams of SIF resolution with a picture rate of 30 frames/sec. The digital video output can be formatted for NTSC, PAL, SECAM, or any other optional video standard. The complete decoding function is realised with the LC82220, a standard 8-bit or 16-bit microcontroller and a bank of DRAM. A typical memory configuration is a single 128 k \times 16 or 256 k \times 16 DRAM. The LC82220 also supports efficient video display functions such as scroll and overlay.

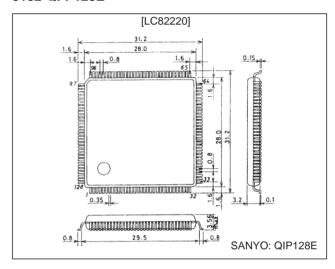
Functions

- Support for JPEG format
- Real-time decoding of motion-JPEG with rate of 30 frames/sec
- Lowest solution cost for amusement, game, PC systems
- Support for YUV 4:1:1 color format
- YUV or RGB digital video outputs compatible with optional video format
- · Programmable picture and display window format
- Support for trick display: scrolling, overlaying
- Standard 8/16-bit microcontroller interface with DMA support for compressed data input
- Support SOI and EOI markers
- Direct connect to video DAC
- Direct connect to 2 M or 4 M DRAM as bit and frame buffers
- · Two Q-tables included
- High-speed processing by fixed Huffman tables

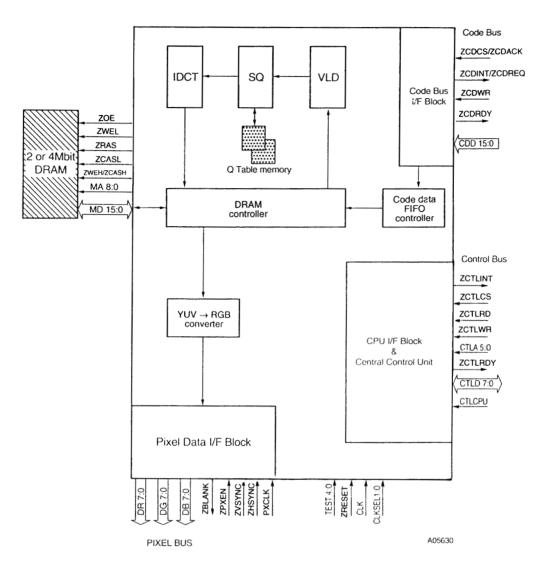
Package Dimensions

unit: mm

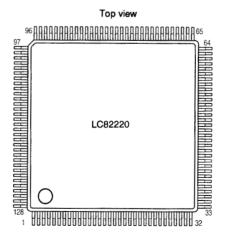
3182-QFP128E



Block Diagram



Pin Assignment



A05631

LC82220

Pin Functions

Pin No.	Symbol	I/O	Function
1	V _{DD}	1/0	+5 V power supply
2	ZCTLINT	0	Control bus interrupt request (open drain output)
3	ZCTLINI	1	Control bus select
4	ZCTLCS	<u>'</u>	Control bus read or R/W select
5	ZCTLWR	<u> </u>	Control bus write or Data strobe
6	ZCTLRDY	0	Control bus ready (tristate output)
7	TEST3	- 1	Test pin
8	TEST4	I	Test pin
9	CTLA5	I	-
10	CTLA4	ı	
11	CTLA3	I	Control bus address
12	CTLA2	I	
13	CTLA1	I	
14	CTLA0	I	
15	CTLCPU	I	Control bus CPU type selection
16	V _{DD}		+5 V power supply
17	V _{SS}		Ground
18	CTLD7	I/O	
19	CTLD6	I/O	
20	CTLD5	I/O	
21	CTLD4	I/O	1
22	CTLD3	I/O	Control bus data
23	CTLD2	I/O	
24	CTLD1	I/O	
25	CTLD0	I/O	
26	TEST0		Test pin
27	ZRESET	· I	Hardware reset
28	CLKSEL0	<u> </u>	
29	CLKSEL1	<u>'</u>	Clock divisor setting CLKSEL1:0 = 00: no divisor, 01: clock divided by 2, 10: clock divided by 3
30	CLKSELT	<u>'</u>	
		· ·	System (decode) clock input (CMOS level input)
31	TEST1	- 1	Test pin
32	V _{DD}		+5 V power supply
33	V _{SS}		Ground
34	ZCDCS/ZCDACK	<u> </u>	Code bus select or Code bus DMA acknowledge
35	ZCDINT/ZCDREQ	0	Code bus interrupt or Code bus DMA request
36	ZCDWR	<u> </u>	Code bus data write signal
37	ZCDRDY	0	Code bus ready (tristate output)
38	CCD15	I	
39	CCD14	I	
40	CCD13	I	
41	CCD12	I	
42	CCD11	I	Code bus data
43	CCD10	1	
44	CCD9	1	
45	CCD8	I	
46	CCD7	l	
47	CCD6	I	
48	V _{SS}		Ground
49	V_{DD}		+5 V power supply
50	CCD5	ı	
51	CCD4	I	Code bus data
52	CCD3	ı	
53	CCD2	1	
54	CCD1	<u> </u>	
55	CCD0		
	1 3050	•	

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Pin No.	Symbol	I/O	Function
56	DB7	0	
57	DB6	0	
58	DB5	0	
59	DB4	0	
60	DB3	0	Pixel data bus B (V)
61	DB2	0	
62	DB1	0	
63	DB0	0	
64	V _{SS}		Ground
65	V _{DD}		+5V power supply
66	ZBLANK	0	Blanking signal
67	ZPXEN	ı	Pixel data enable signal
68	PXCLK	i	Pixel clock
69	ZVSYNC	i	Vertical synchronizing signal
70	ZHSYNC	i	Horizontal synchronizing signal
71	DG7	0	Tionzonial Synonionizing Signal
72	DG7	0	+
73	DG5	0	+
74	DG5 DG4	0	+
75	DG4 DG3	0	Pixel data bus G (U)
76	DG3	0	+
77	DG2 DG1	0	1
78	DG1	0	1
79	TEST2	ı	Test pin
80		'	+5 V power supply
80	V _{DD}		Fo v power supply Ground
82	V _{SS} DR7	0	Giodila
83	DR7 DR6	0	
83	DR6 DR5	0	-
85	DR5 DR4	0	Bivel data hus B (V)
86	DR4 DR3	0	Pixel data bus R (Y)
86	DR3 DR2	0	
88	DR2 DR1	0	
89	DR1 DR0	0	-
90			Ground
90	V _{SS} ZOE	0	Ground Memory output populo
		0	Memory output enable
92	ZWEL	0	Memory write enable (L) Row address strobe
	ZRAS ZCASL	0	
94 95	ZWEH/ZCASH	0	Column address strobe (L) Memory write enable (H)/column address strobe (H)
95			+5 V power supply*1
96	V _{DD}		Fo v power supply** Ground
98	V _{SS} MD15	I/O	Olouliu
99	MD15	1/0	-
100	MD14 MD13	1/0	Frame memory interface data bus
100	MD13	1/0	Traine memory interiace data bus
101	MD12 MD11	1/0	-
102	MD11	1/0	-
103		1/0	+5 V power supply
104	V _{DD}		+5 v power supply Ground
106	V _{SS} MD9	I/O	Olouliu
106	MD8	1/0	1
107	MD7	1/0	Frame memory interface data bus
108		1/0	Traine memory interiace data bus
	MD6		
110	MD5	I/O I/O	
111	MD4	1/0	Continued on next need

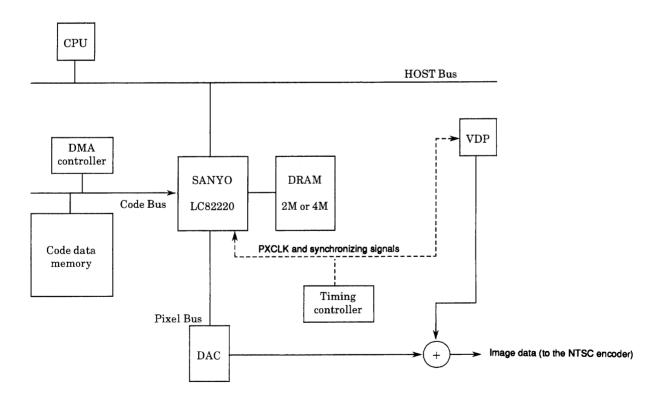
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Pin No.	Symbol	I/O	Function
112	V _{SS}		Ground
113	V _{DD}		+5 V power supply
114	MD3	I/O	
115	MD2	I/O	Frame memory interface data bus
116	MD1	I/O	
117	MD0	I/O	
118	V _{SS}		Ground
119	MA8	0	
120	MA7	0	
121	MA6	0	
122	MA5	0	
123	MA4	0	Frame memory address signals
124	MA3	0	
125	MA2	0	
126	MA1	0	
127	MA0	0	
128	V _{SS}		Ground

System Configuration Example

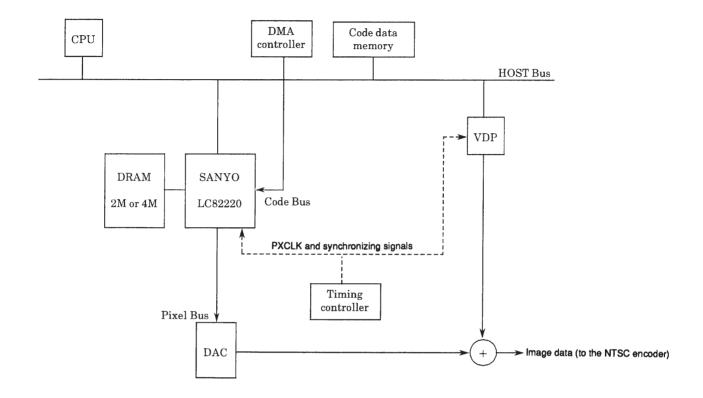
1. Separate code bus type

This is a system in which the code and system busses are separated. The coded data input does not load down the system bus.



2. Shared code bus type

This is a system in which code bus and the system bus are connected. Coded data is written by the CPU, or alternatively, data can be written using the DMA controller.



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