



LC83025E

Digital Signal Processor for Karaoke Products

Overview

The LC83025E is a special-purpose karaoke DSP that implements the signal processing required by karaoke systems, including pitch shift, microphone echo, voice muting and simple surround, with only a single 256Kb external DRAM. Since the LC83025E includes built-in A/D and D/A converters, it can also handle analog inputs and outputs in addition to digital inputs and outputs. The LC83025E uses serial transfer of coefficient data from a microcontroller to handle changes in functions and characteristics required for each application.

Features

- Applications

- Pitch shift

The LC83025E can shift the music pitch or the microphone pitch by ± 15 steps in 1/4 interval steps, or ± 1 octave in scale tone steps according to command data sent from the microcontroller. Furthermore, the pitch can be changed up to ± 1 octave in arbitrary steps by setting internal coefficients.

- Microphone echo

The LC83025E implements echo processing for the signal input from the microphone A/D converter. The amount of echo, the delay time and other parameters can be changed by setting coefficients.

- Voice mute

The LC83025E implements processing that removes monaural signal components included in the music signal. This allows CDs with vocals to be used as karaoke CDs. Command data is used to turn the voice mute function on or off.

- Simple surround

The LC83025E implements a simple surround function by adding delayed components to the music signal. The LC83025E includes six sets of simple surround coefficients as built-in preset data. These values can be switched by sending command data. Applications can implement their own original surround effects by setting the coefficients. However, the algorithm itself is fixed.

- Flexible input mixing

The LC83025E supports hybrid mixing of digital and analog left and right channel song inputs, and thus can handle a wide range of disk processing configurations.

- Audio inputs and outputs

- Inputs: Digital - One system (stereo)

A/D converter - Three channels

- Outputs: Digital - One system (stereo)

D/A converter - Two channels

- A/D converter

Second order $\Delta\Sigma$ modulation - Three channels

- D/A converter

4 \times oversampling digital filters

plus second order noise shaper

plus 5-bit PWM system - Two channels

- Master clock: 768 fs

- External memory: Up to two 256K (64K \times 4-bit) DRAMs can be used

- Microcontroller input: Synchronous 8-bit serial data

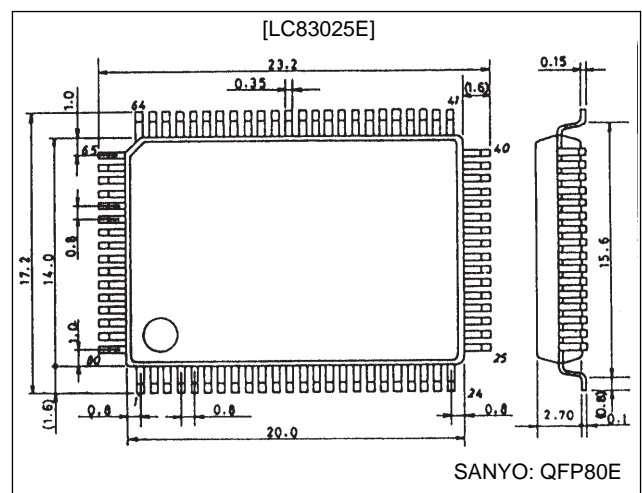
- Supply voltage: 5 V single-voltage

- Package: QFP80E

Package Dimensions

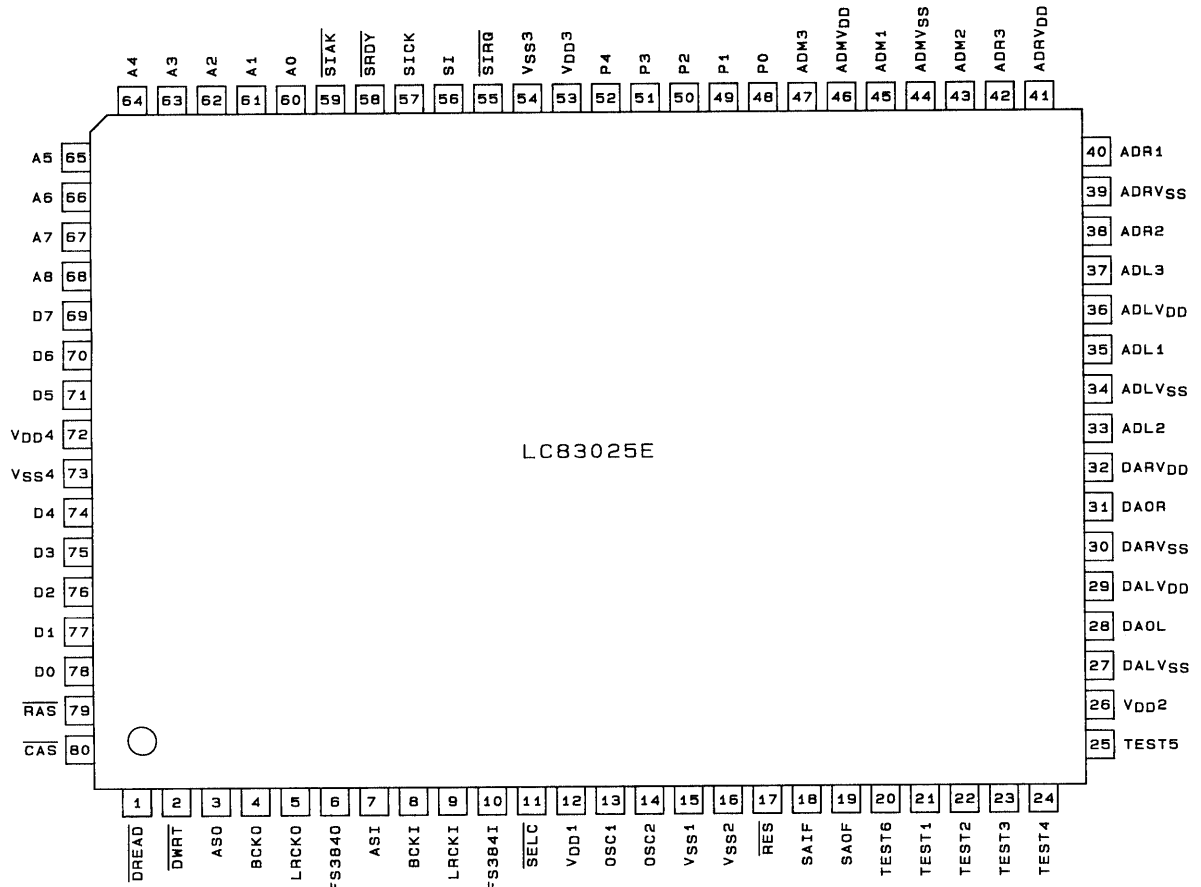
unit: mm

3174-QFP80E



LC83025E

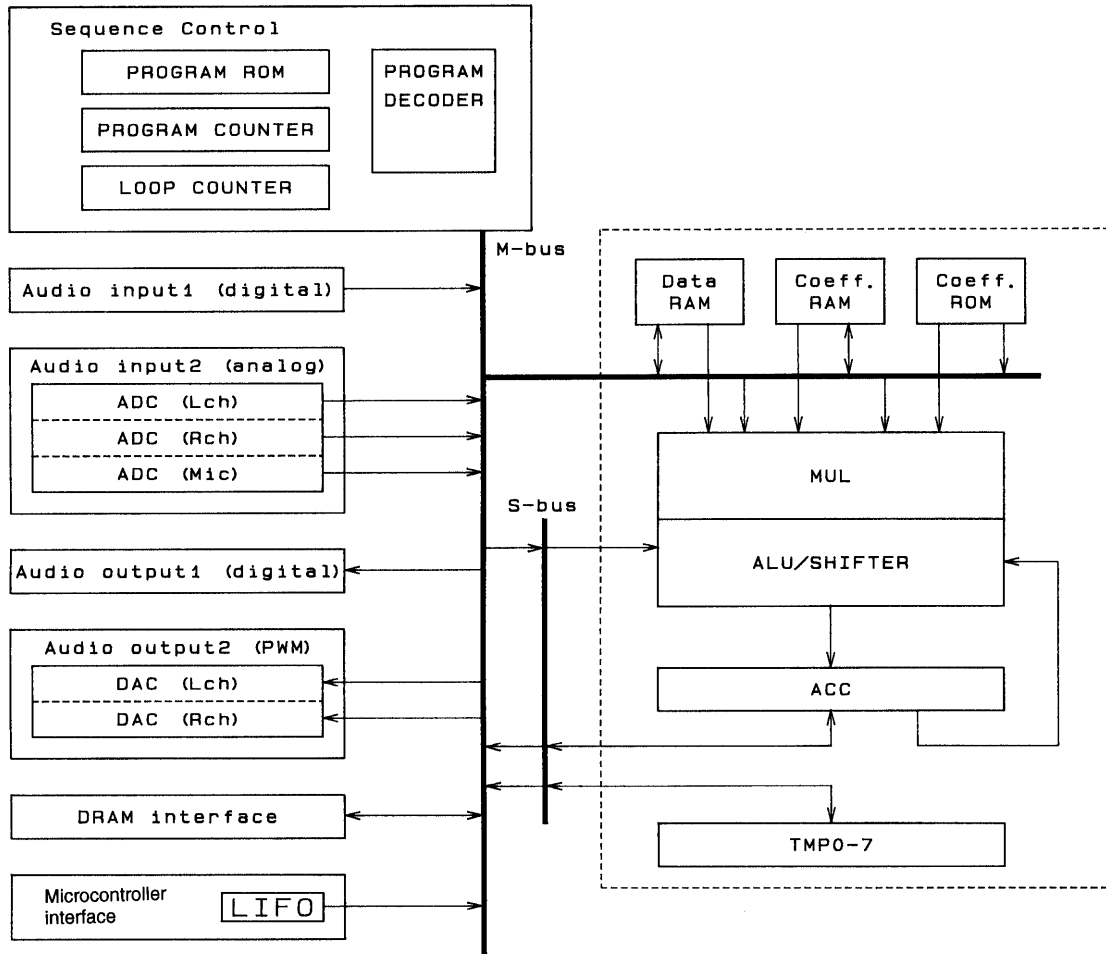
Pin Assignment



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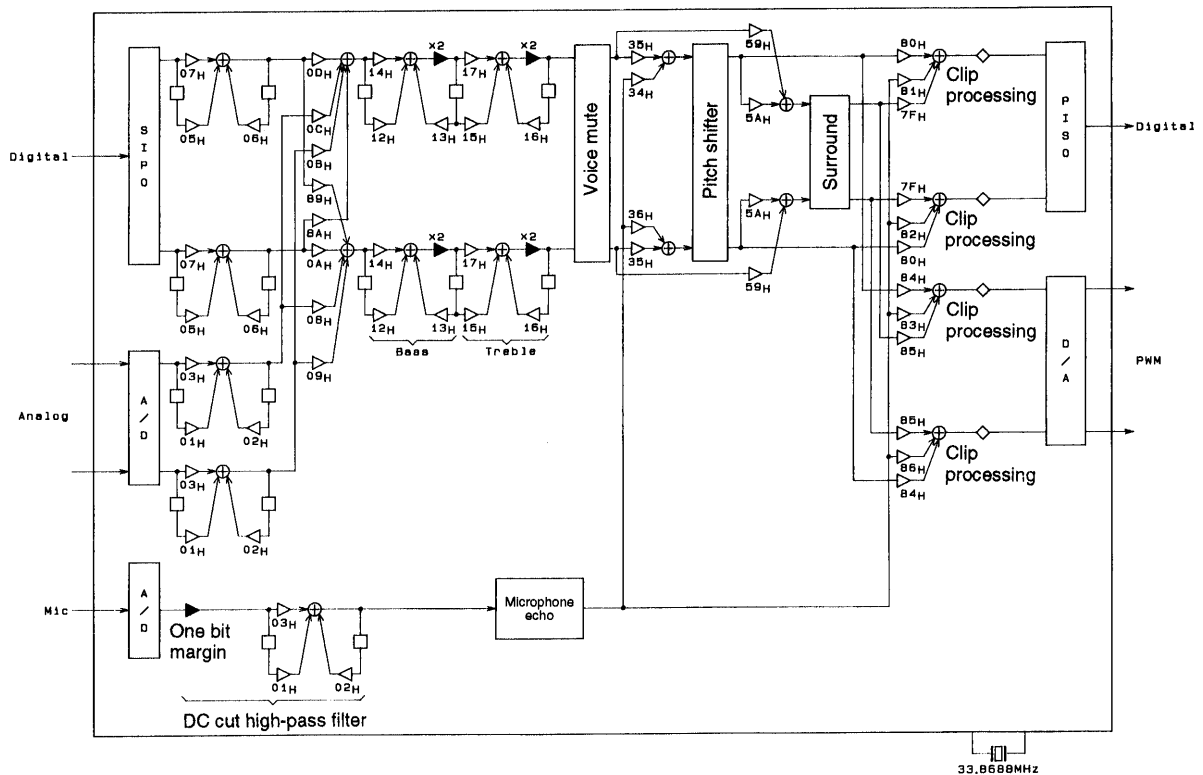
Top view

Block Diagram



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Signal Flow Overview



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LC83025E

Pin Functions

Pin No.	Symbol	I/O	Function
[Control pins]			
13	OSC1	I	Crystal oscillator connection (768 fs)
14	OSC2	O	Crystal oscillator connection (768 fs)
10	FS384I	I	384 fs input (Apply a clock that is equal to the OSC1/OSC2 768 fs clock divided by 2.)
11	$\overline{\text{SEL}}\text{C}$	I	Audio clock source switching (High: Fixes FS384I as the clock)
18	SAIF	I	Digital audio input mode switching (Low: backward packed, High: forward packed)
19	SAOF	I	Digital audio output mode switching (Low: 48 fs, High: 64 fs)
17	$\overline{\text{RES}}$	I	Reset
25 to 21	TEST5 to TEST1	I	Test (Must be tied to ground in normal operation.)
20	TEST6	O	Test (Must be left open in normal operation.)
48	P0	I	Coefficient transfer mode switching
50, 49	P2, P1	I	Initial operating mode setting (This pin should be held high in normal operation.)
51	P3	O	Microphone signal present (low output) or absent (high output) indication output
52	P4	O	Music signal present (low output) or absent (high output) indication output
[External memory interface]			
79	$\overline{\text{RAS}}$	O	$\overline{\text{RAS}}$ signal output
80	$\overline{\text{CAS}}$	O	$\overline{\text{CAS}}$ signal output
1	$\overline{\text{DREAD}}$	O	External memory read signal output
2	$\overline{\text{DWRT}}$	O	External memory write signal output
68 to 60	A8 to A0	O	Address outputs
69 to 71, 74 to 78	D7 to D0	I/O	Data I/O (Normally, only D3 to D0 are used.)
[Audio interface]			
9	LRCKI	I	ASI L/R clock input (1 fs)
5	LRCKO	O	ASO L/R clock output (1 fs)
8	BCKI	I	ASI bit clock input (32 fs or higher)
4	BCKO	O	ASO bit clock output (48 fs or 64 fs)
6	FS384O	O	ASO 384 fs output
7	ASI	I	Digital audio data input (MSB first, 16 bits)
3	ASO	O	Digital audio data output (MSB first, backward packed, 16 bits)
35	ADL1	I	A/D converter input (left channel)
33	ADL2	O	A/D converter output (left channel)
37	ADL3	O	A/D converter output (left channel)
40	ADR1	I	A/D converter input (right channel)
38	ADR2	O	A/D converter output (right channel)
42	ADR3	O	A/D converter output (right channel)
45	ADM1	I	A/D converter input (microphone)
43	ADM2	O	A/D converter output (microphone)
47	ADM3	O	A/D converter output (microphone)
28	DAOL	O	D/A converter output (left channel)
31	DAOR	O	D/A converter output (right channel)
[Microcontroller interface]			
55	$\overline{\text{SIRQ}}$	I	Serial input request signal input
59	$\overline{\text{SIAK}}$	O	Output indicating serial input execution in progress
56	SI	I	Serial data input from the control microcontroller (8-bit serial data)
57	SICK	I	SI transfer clock input
58	$\overline{\text{SRDY}}$	I	Ready signal input from the control microcontroller that indicates that serial data input has completed

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LC83025E

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Pin No.	Symbol	I/O	Function
[Power supply pins]			
12, 26, 53, 72	V_{DD}	—	V_{DD} for the digital block (Connect to +5 V.) (Keep connections as short as possible so that potential differences between the V_{DD} pins do not occur.)
15, 16, 54, 73	V_{SS}	—	V_{SS} for the digital block (Connect to ground.) (Keep connections as short as possible so that potential differences between the V_{SS} pins do not occur.)
36	$ADLV_{DD}$	—	A/D converter V_{DD} (left channel) (Connect to +5 V.)
41	$ADRV_{DD}$	—	A/D converter V_{DD} (right channel) (Connect to +5 V.)
46	$ADMV_{DD}$	—	A/D converter V_{DD} (microphone) (Connect to +5 V.)
29	$DALV_{DD}$	—	D/A converter V_{DD} (left channel) (Connect to +5 V.)
32	$DARV_{DD}$	—	D/A converter V_{DD} (right channel) (Connect to +5 V.)
34	$ADLV_{SS}$	—	A/D converter V_{SS} (left channel) (Connect to ground.)
39	$ADRV_{SS}$	—	A/D converter V_{SS} (right channel) (Connect to ground.)
44	$ADMV_{SS}$	—	A/D converter V_{SS} (microphone) (Connect to ground.)
27	$DALV_{SS}$	—	D/A converter V_{SS} (left channel) (Connect to ground.)
30	$DARV_{SS}$	—	D/A converter V_{SS} (right channel) (Connect to ground.)

LC83025E

Pin Circuits

Specification	Circuit	Pins
TTL output	<p style="text-align: right;">Output data A03570</p>	ASO, LRCKO, BCKO, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{DREAD}}$, $\overline{\text{DWRT}}$, FS384O, A0 to A8
CMOS intermediate current output		P3, P4, $\overline{\text{SIK}}$, TEST6
Analog output	<p style="text-align: right;">Output data A03571</p>	DAOL, DAOR, ADL2, ADL3, ADM2, ADM3, ADR2, ADR3
Schmitt input	<p style="text-align: right;">Input data A03572</p>	SI, SICK, $\overline{\text{SIRQ}}$, $\overline{\text{SRDY}}$, (OSC1)
Low Schmitt input		FS384I, BCKI, ASI, LRCKI
Normal input	<p style="text-align: right;">Input data A03573</p>	TEST1 to TEST5
Input with built-in pull-up resistor	<p style="text-align: right;">Input data A03574</p>	$\overline{\text{RES}}$
Input with built-in pull-down resistor	<p style="text-align: right;">Input data A03575</p>	$\overline{\text{SEL}}$ C, SAIF, SAOF
CMOS intermediate current output Low Schmitt input	<p style="text-align: right;">Input data I/O control Output data A03576</p>	D0 to D7
N-channel open drain intermediate current output Normal input	<p style="text-align: right;">Input data Test output data Off during normal operation A03577</p>	P0 to P2
Analog input	<p style="text-align: right;">A03573</p>	ADL1, ADR1, ADM1

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit	Note
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +7.0	V	
Output voltage	V_{O1}	OSC2 output	Allowed up to the oscillator voltage.	V	
	V_{O2}	Pins other than OSC2	-0.3 to $V_{DD} + 0.3$	V	
Input voltage	V_{IN}		-0.3 to $V_{DD} + 0.3$	V	
Peak output current	I_{OP1}	Audio interface, external RAM interface	-2 to +4	mA	1
	I_{OP2}	Microcontroller interface, P3, P4	-2 to +10	mA	2
Average output current	I_{OA1}	Audio interface, external RAM interface: per pin	-2 to +4	mA	1
	I_{OA2}	Microcontroller interface, P3, P4: per pin	-2 to +10	mA	2
	ΣI_{OA1}	Total for FS384O, LRCKO, BCKO, and ASO	-10 to +10	mA	
	ΣI_{OA2}	Total for \overline{DWR} T, \overline{DRE} AD, \overline{RAS} , \overline{CAS} , A3 to A8 and D0 to D7	-30 to +30	mA	
	ΣI_{OA3}	Total for A0 to A2, \overline{SLA} K, P3 and P4	-10 to +10	mA	
Allowable power dissipation	$P_{d\text{ max}}$	$T_a = -30$ to $+70^\circ\text{C}$	700	mW	
Operating temperature	T_{opr}		-30 to +70	$^\circ\text{C}$	
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$	

Allowable Operating Ranges

at $T_a = -30$ to $+70^\circ\text{C}$, all $V_{DD} = 4.75$ to 5.25 V , all $V_{SS} = 0\text{ V}$ unless otherwise specified

Parameter	Symbol	Conditions	min	typ	max	Unit	Note
Operating supply voltage	V_{DD}		4.75		5.25	V	
Input high level voltage	V_{IH1}	Audio interface, external RAM interface	2.4			V	4
	V_{IH2}	P0 to P2, \overline{SE} LC, SAIF, SAOF, TEST1 to TEST5	$0.7 V_{DD}$			V	5
	V_{IH3}	\overline{RES} , OSC1, microcontroller interface	$0.75 V_{DD}$			V	6
Input low level voltage	V_{IL1}	Audio interface, external RAM interface			0.8	V	4
	V_{IL2}	P0 to P2, \overline{SE} LC, SAIF, SAOF, TEST1 to TEST5			$0.3 V_{DD}$	V	5
	V_{IL3}	\overline{RES} , OSC1, microcontroller interface			$0.25 V_{DD}$	V	6
Instruction cycle time	t_{CYC}		58		59.11	ns	
[External Clock Input Conditions]							
Frequency	f_{EXT}		16.85		17.01	MHz	
Pulse width	t_{EXTH}	Related to the FS384I pin. Shown in Figure 1. max: $44.1\text{ kHz} \times 384 \times 1.005$ min: $44.1\text{ kHz} \times 384 \times 0.995$	23			ns	
	t_{EXTL}		23			ns	
Rise time	t_{EXTR}				9	ns	
Fall time	t_{EXTF}				9	ns	
[Self-Excitation Oscillation Conditions]							
Oscillator frequency	f_{OSC}	OSC1 and OSC2: shown in Figure 2. $44.1\text{ kHz} \times 768 \times \pm 0.1\%$	33.84		33.90	MHz	
Oscillator stabilization period	f_{OSCS}	Shown in Figure 3.			100	ms	
[Audio Data Input Conditions]							
Transfer bit clock period	t_{BCYC}	Related to the BCKI and ASI pins. Shown in Figure 4.	354			ns	
Transfer bit clock pulse width	t_{BCW}		100			ns	
Data setup time	t_S		70			ns	
Data hold time	t_H		70			ns	
[Serial Input Clock Conditions]							
Serial clock period	t_{SCYC}	Related to the microcontroller interface. Shown in Figure 5. (Related to the SICK, SI and \overline{SRDY} pins.)	480			ns	
Serial clock pulse width	t_{SCW}		200			ns	
Data setup time	t_{SS}		70			ns	
Data hold time	t_{SH}		70			ns	
\overline{SRDY} hold time	t_{SYH}		200			ns	
\overline{SRDY} pulse width	t_{SYW}		200			ns	
[DRAM Input Conditions]							
Input data setup time	t_{DSI}	Related to external DRAM data input. Shown in Figure 6.	20			ns	
Input data hold time	t_{DHI}	(Related to the \overline{CAS} and D0 to D7 pins.)	0			ns	

LC83025E

Electrical Characteristics 1

at $T_a = -30$ to $+70^\circ\text{C}$, all $V_{DD} = 4.75$ to 5.25 V, all $V_{SS} = 0$ V unless otherwise specified

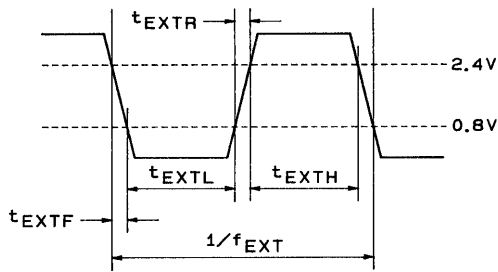
Parameter	Symbol	Conditions	min	typ	max	Unit	Note
Input low level current	I_{IL1}	RES, $V_{IN} = V_{SS}$ (Input pins with built-in pull-up resistor)	-250	-100		μA	8
	I_{IL2}	P0 to P2, $V_{IN} = V_{SS}$	-10			μA	
	I_{IL3}	Other input-only pins	-10			μA	
Input high level current	I_{IH1}	SELC, SAIF, SAOF, $V_{IN} = V_{DD}$ (Input pins with built-in pull-down resistor)		100	250	μA	8
	I_{IH2}	P0 to P2, $V_{IN} = V_{DD}$ (n-channel transistor: off)			10	μA	
	I_{IH3}	Other input-only pins			10	μA	
Output high level voltage	V_{OH1}	$I_{OH} = -0.4$ mA	4.0	4.98		V	1, 8
	V_{OH2}	$I_{OH} = -50$ μA	$V_{DD} - 1.2$	4.997		V	2, 3, 8
Output low level voltage	V_{OL1}	$I_{OL} = 2$ mA		0.065	0.4	V	1, 8
	V_{OL2}	$I_{OL} = 10$ mA		0.32	1.5	V	2, 3, 8
Output off leakage current	I_{OFF}	$V_O = V_{SS}, V_{DD}$	-40		+40	μA	
I/O capacitance	C_{IO}				10	pF	
[Audio Data Output Timing]							
Output data hold time	t_{OH}	BCKO and ASO: shown in Figure 7.	-30			ns	7
Output data delay time	t_{OD}				50	ns	7
[External DRAM Access Timing]							
$\overline{\text{RAS}}$ high pulse width	t_{RP}	Timing for output to the external DRAM. Shown in Figure 8.	80			ns	7
$\overline{\text{RAS}}$ low pulse width	t_{RAS}		700			ns	7
$\overline{\text{CAS}}$ high pulse width	t_{CP}		50			ns	7
$\overline{\text{CAS}}$ low pulse width	t_{CAS}		95			ns	7
$\overline{\text{CAS}}$ cycle time	t_{PC}		175			ns	7
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}		60			ns	7
$\overline{\text{CAS}}$ hold time	t_{CSH}		170			ns	7
$\overline{\text{RAS}}$ hold time	t_{RSH}		95			ns	7
$\overline{\text{RAS}}$ address setup time	t_{ASR}		60			ns	7
$\overline{\text{RAS}}$ address hold time	t_{RAH}		20			ns	7
$\overline{\text{CAS}}$ address setup time	t_{ASC}		30			ns	7
$\overline{\text{CAS}}$ address hold time	t_{CAH}		90			ns	7
$\overline{\text{DWR}}$ pulse width	t_{WP}		95			ns	7
Write command setup time	t_{WCS}		12			ns	7
Write command hold time	t_{WCH}		65			ns	7
Output data setup time	t_{DSO}		30			ns	7
Output data hold time	t_{DHO}		100			ns	7
Crystal oscillator	C1	OSC1 and OSC2: shown in Figure 2.		13		pF	8
	C2			29		pF	8
Current drain	L	$V_{DD1}, V_{DD2}, V_{DD3}$; oscillator frequency: 33.8688 MHz		1.5		μH	8
	I_{DD}			60	95	mA	9

LC83025E

Electrical Characteristics 2 at $T_a = 25^\circ\text{C}$, all $V_{DD} = 5.0\text{ V}$, all $V_{SS} = 0\text{ V}$ unless otherwise specified

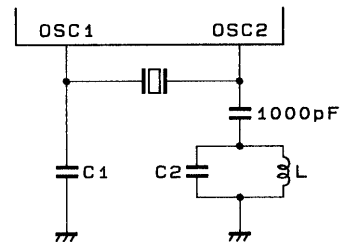
Parameter	Symbol	Conditions	min	typ	max	Unit	Note
[A/D Converter Block]							
Total harmonic distortion	A-THD	1 kHz, 0 dB: Lch		0.065		%	10, 11
		1 kHz, 0 dB: Rch		0.065		%	10, 11
		1 kHz, 0 dB: Mic		0.070		%	10, 11
Signal-to-noise ratio	A-S/N	1 kHz, 0 dB	70	75		dB	10, 11
Crosstalk	A-C · T	1 kHz, 0 dB		-72		dB	10
[D/A Converter Block]							
Total harmonic distortion	D-THD	1 kHz, -1 dB		0.045		%	10
Signal-to-noise ratio	D-S/N	1 kHz, -1 dB		78		dB	10
Crosstalk	D-C · T	1 kHz, -1 dB		-75		dB	10

- Note:
1. TTL output level pins: ASO, FS384O, BCKO, LRCKO, D0 to D7, A0 to A8, RAS, CAS, DREAD, DWRT
 2. CMOS intermediate current output pins: P3, P4, SIAK, TEST6
 3. N-channel open-drain intermediate current output pins: P0 to P2
 4. Low Schmitt input pins: BCKI, ASI, LRCKI, D0 to D7, FS384I
 5. Normal input pins: P0 to P2, TEST1 to TEST5, SELC, SAIF, SAOF
 6. Schmitt input pins: RES, SI, SICK, SIRQ, SRDY, OSC1
 7. When the load capacitance is 50 pF
 8. The values for the oscillator capacitors C1 and C2 include the wiring capacitances.
 9. The value for the current drain is a typical value for $V_{DD} = 5\text{ V}$, room temperature, and a typical sample.
 10. With weight A filter present, with $F_s = 44.1\text{ kHz}$, and tested in the Sanyo evaluation board.
 11. Varies with the values of the external components. The listed value is for the circuit structure and values shown in Figure 9 in the Sanyo evaluation board.



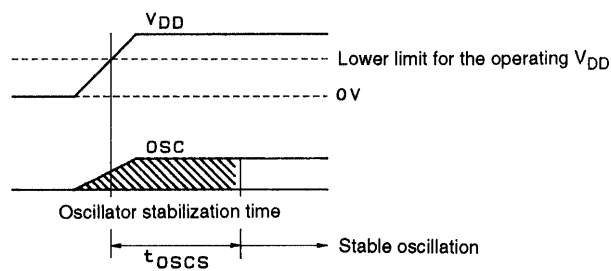
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Figure 1 External Clock Input Waveform (FS384I)



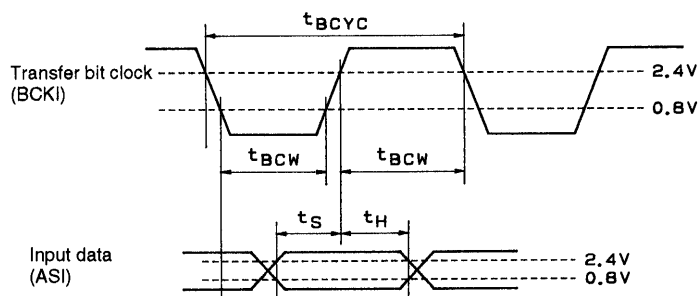
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Figure 2 Crystal Oscillator Circuit



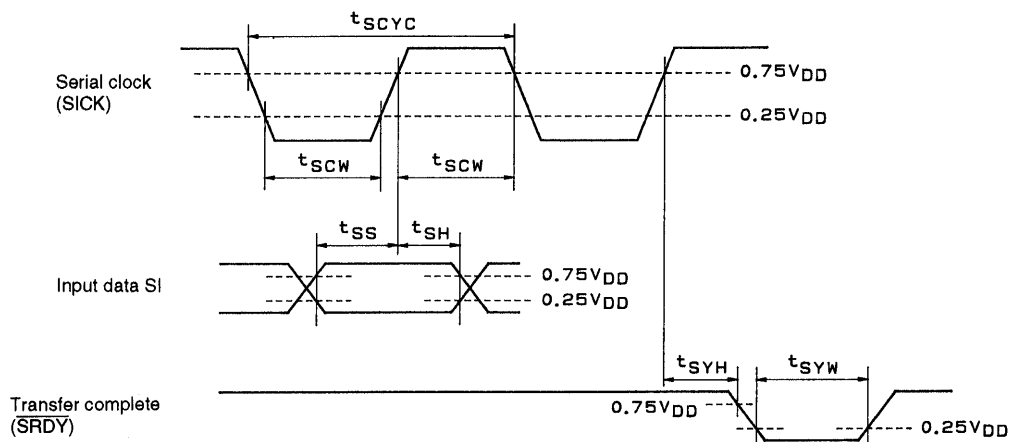
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Figure 3 Oscillator Stabilization Time



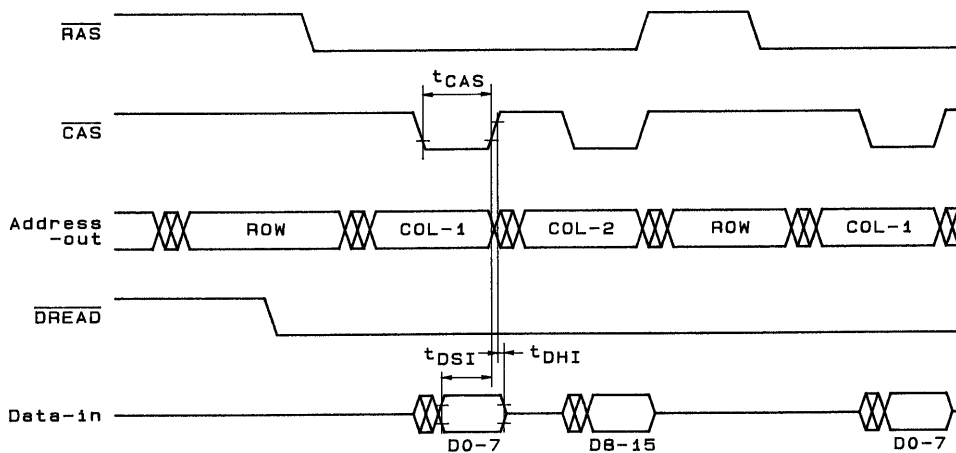
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Figure 4 Audio Data Input Conditions



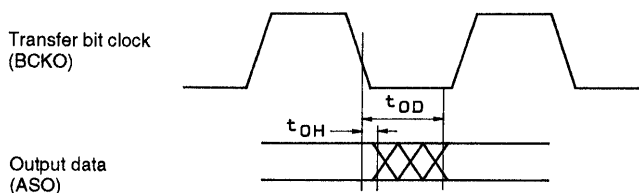
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Figure 5 Microcontroller Interface



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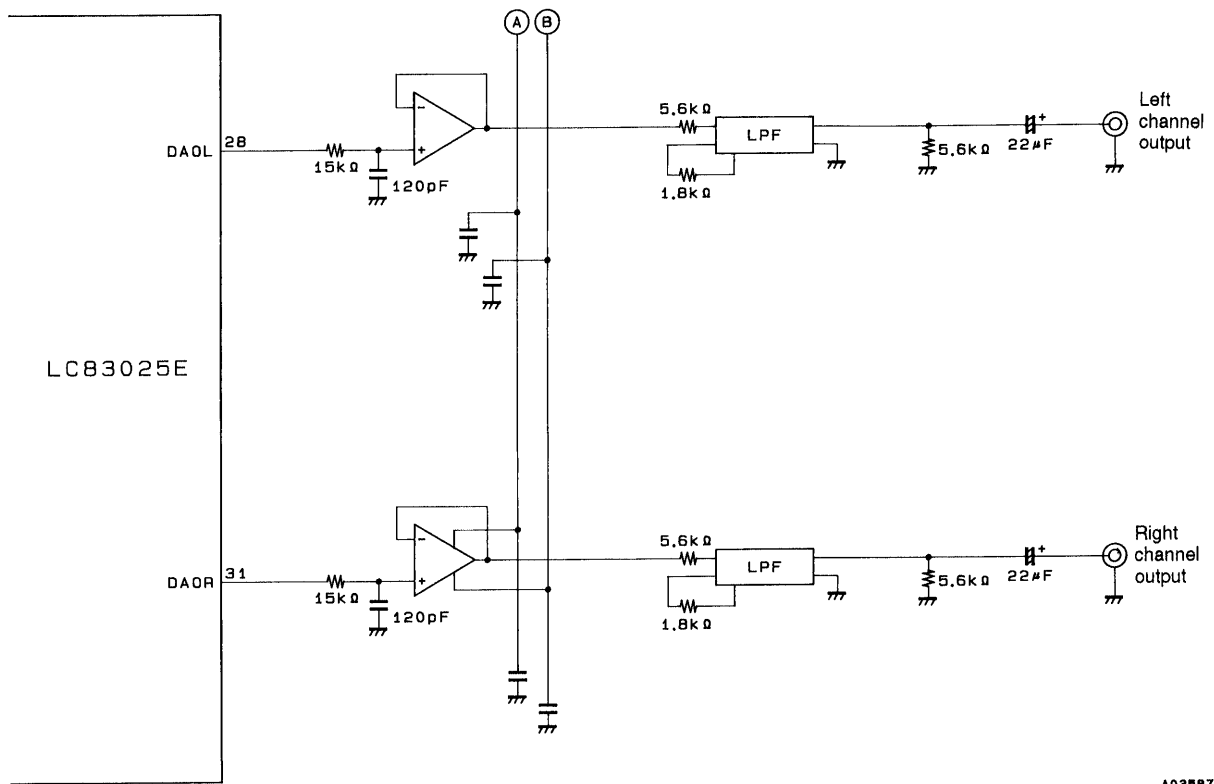
Figure 6 Timing for Data Input from External DRAM



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Figure 7 Audio Data Output Timing

LC83025E

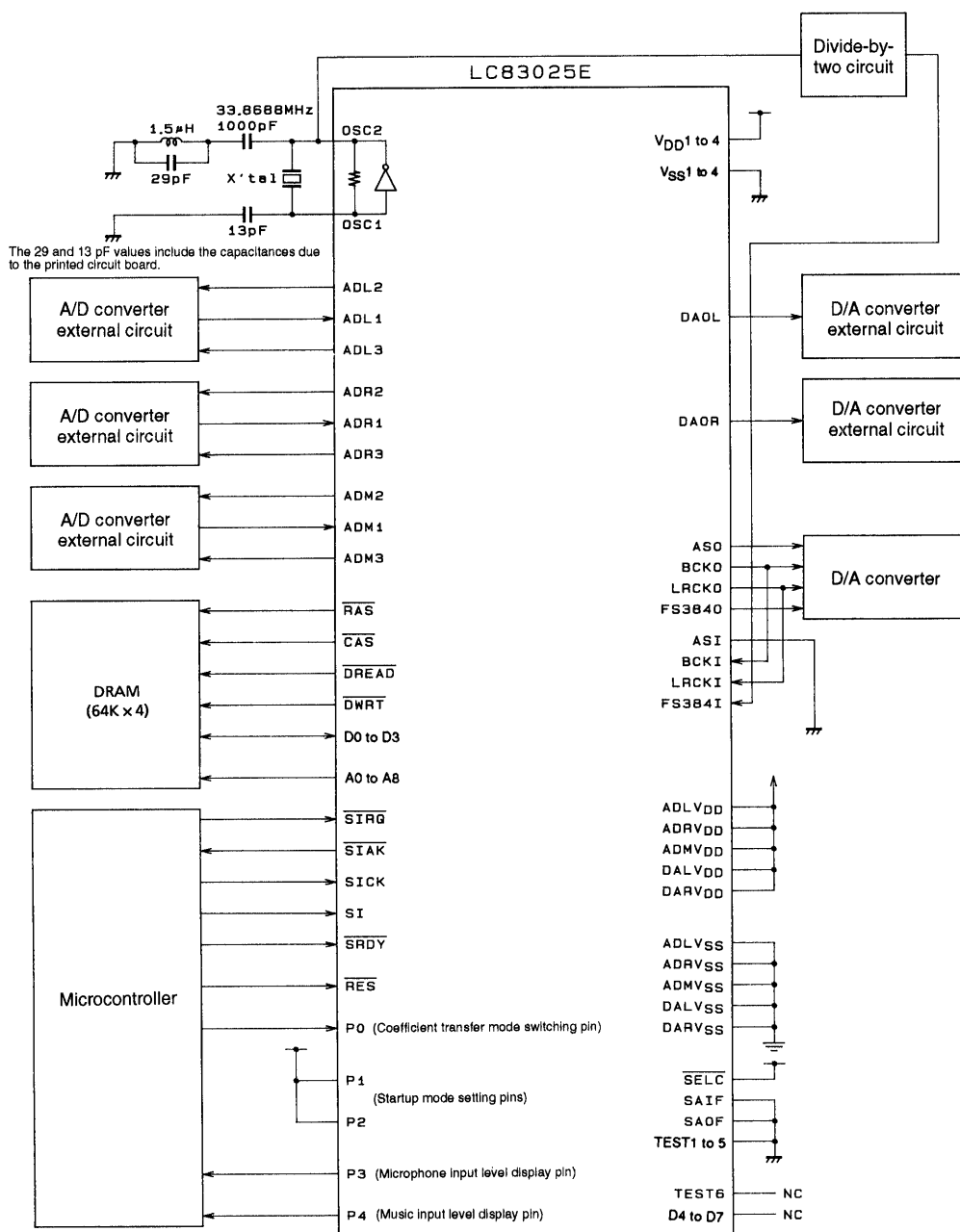


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Figure 10 Sample D/A Converter External Circuit

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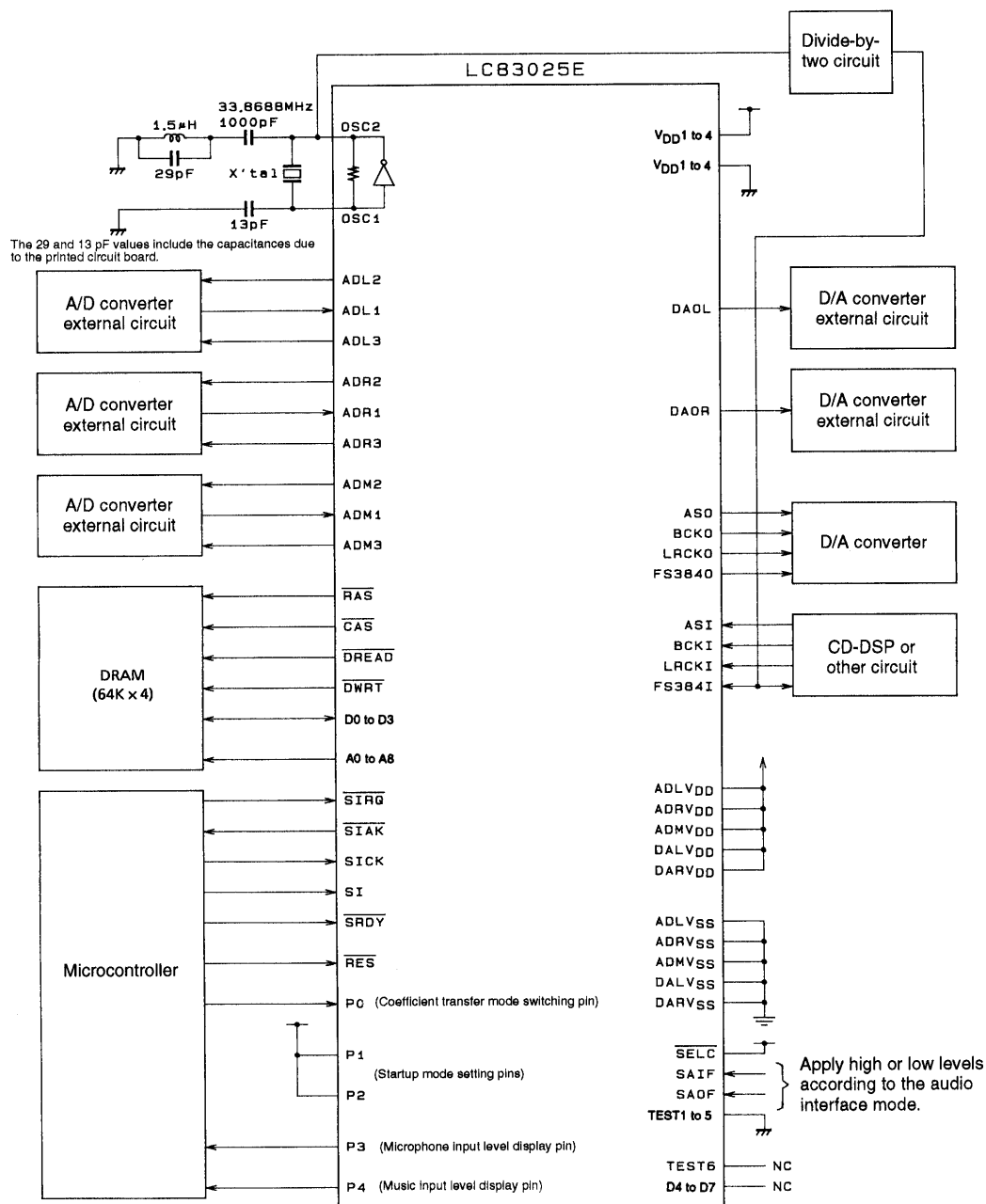
Sample Peripheral Circuit Connection (For applications that do not use digital input)



Whether or not the digital outputs and the analog L/R outputs will be used will be determined by the end product specifications. These pins should be left open if unused.

LC83025E

Sample Peripheral Circuit Connection (For applications that use digital input.)



Whether or not the analog L/R inputs and the analog L/R outputs will be used will be determined by the end product specifications. A high or low level should be applied to unused input pins, and unused output pins should be left open.

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