

**LC895194**

CD-ROM Error Correction LSI with On-Chip ATA-PI (IDE) Interface

Preliminary**Functions**

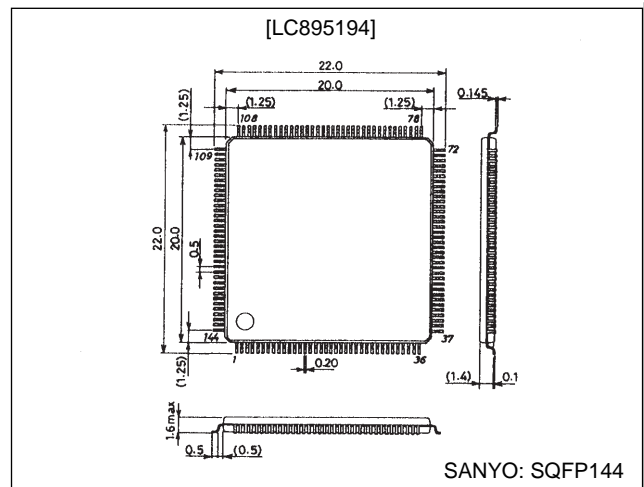
CD-ROM error detection and correction, ATA-PI (IDE) interface (including the register and other blocks)

Features

- ATA-PI (IDE) interface
- Supports 16×-speed playback (with IORDY): Using 16× 70 ns DRAMs
- 16.6 MB/s transfer rate: Using 16× 70 ns DRAMs
- Supports the use of from 1 M to 32 M of buffer RAM. (DRAM)
- Allows the user to arbitrarily set the CD main channel and C2 flag areas in buffer RAM.
- Batch transfer function (function for transferring the CD main channel and C2 flag data in one operation)
- Multi-transfer function (function for sending multiple blocks in one operation)

Package Dimensions

unit: mm

3214-SQFP144**Specifications****Absolute Maximum Ratings at $V_{SS} = 0$ V**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	$T_a = 25^\circ\text{C}$	-0.3 to +7.0	V
I/O voltages	V_I, V_O	$T_a = 25^\circ\text{C}$	-0.3 to $V_{DD} + 0.3$	V
Allowable power dissipation	P_d max	$T_a \leq 70^\circ\text{C}$	550	mW
Operating temperature	T_{opr}		-30 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^\circ\text{C}$
Soldering heat resistances (pins only)		10 seconds	235	$^\circ\text{C}$
I/O power	I_I, I_O		$\pm 20^*$	mA

Note: * Per cell for basic I/O cells

Allowable Operating Ranges at $T_a = -30$ to $+75^\circ\text{C}$, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

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DC Characteristics at $V_{SS} = 0\text{ V}$, $V_{DD} = 4.5\text{ to }5.5\text{ V}$, $T_a = -30\text{ to }+75^\circ\text{C}$

Parameter	Symbol	Applicable Pins* (See below)	min	typ	max	Unit
Input high level voltage	V_{IH}	TTL compatible: (1)	2.2	—	—	V
Input low level voltage	V_{IL}		—	—	0.8	V
Input high level voltage	V_{IH}	TTL compatible, with pull-up resistor: (13)	2.2	—	—	V
Input low level voltage	V_{IL}		—	—	0.8	V
Input high level voltage	V_{IH}	TTL compatible, with pull-down resistor: (2)	2.2	—	—	V
Input low level voltage	V_{IL}		—	—	0.8	V
Input high level voltage	V_{IH}	TTL compatible, Schmitt: (3), (5), and (14)	2.4	—	—	V
Input low level voltage	V_{IL}		—	—	0.8	V
Input high level voltage	V_{IH}	COMS compatible, Schmitt: (4)	$0.8 V_{DD}$	—	—	V
Input low level voltage	V_{IL}		—	—	$0.2 V_{DD}$	V
Output high level voltage	V_{OH}	$I_{OH} = -2\text{ mA}$	$V_{DD} - 2.1$	—	—	V
Output low level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$				
Output high level voltage	V_{OH}	$I_{OH} = -8\text{ mA}$	$V_{DD} - 2.1$	—	—	V
Output low level voltage	V_{OL}	$I_{OL} = 8\text{ mA}$				
Output high level voltage	V_{OH}	$I_{OH} = 4\text{ mA}$	$V_{DD} - 2.1$	—	—	V
Output low level voltage	V_{OL}	$I_{OL} = 24\text{ mA}$				
Output high level voltage	V_{OH}	$I_{OH} = -2\text{ mA}$	$V_{DD} - 2.1$	—	—	V
Output low level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$				
Output low level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$ (11)	—	—	0.4	V
Output low level voltage	V_{OL}	$I_{OL} = 24\text{ mA}$ (12)	—	—	0.4	V
Input leakage current	I_{IL}	$V_I = V_{SS}, V_{DD}$: (1), (3), (4), (9), and (14)	-10	—	+10	μA
Output leakage current	I_{OZ}	For high-impedance outputs: (6), (12), and (14)	-10	—	+10	μA
Pull-up resistance	R_{UP}	(13)	40	80	160	$\text{k}\Omega$
Pull-down resistance	R_{DN}	(2), (5)	40	80	160	$\text{k}\Omega$
Input voltage hysteresis	V_{HYS}	(3), and (14)	0.8	1.0	1.3	mV

Note: * The entries in the "Applicable Pins" column specify the following pin sets.

[Input]

1: CCTRL, SUA0 to SUA6

2: TEST0 to TEST4

3: DA0 to DA2, ZCS1FX, ZCS3FX, ZDIOR, ZDIOW, ZDMACK, ZHRST, ZRESET, BCK, C2PO, LRCK, SDATA

4: ZCS, ZRD, ZWR

5: WFCK, SCOR

[Output]

6: ZINT1

7: MCK, MCK2

8: ZINT, ZSWAIT

9: DMARQ, HINTRQ

10: RA0 to RA9, ZCAS0, ZCAS1, ZLWE, ZOE, ZRAS0, ZRAS1, ZUWE

11: ZRSTCPU, ZRSTIC

12: IORDY, ZIOCS16

[I/O]

13: D0 to D7, IO0 to IO15

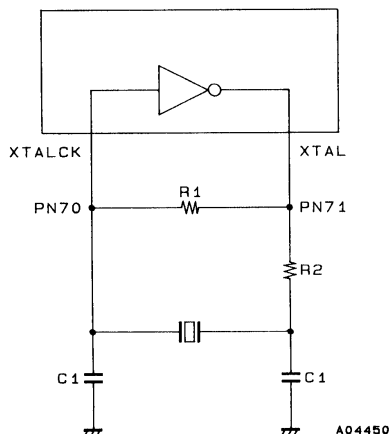
14: DD0 to DD15, ZDASP, ZPDIAG

Note: XTAL, XTALCK

The above pins are not included in the DC characteristics.

Sample Recommended Oscillator Circuit

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$R1 = 120\text{ k}\Omega$

$R2 = 47\text{ k}\Omega$

$C1 = 30\text{ pF}$

For a crystal oscillator frequency of 16.9344 MHz.

Alternatively:

$R1 = 3.3\text{ k}\Omega$

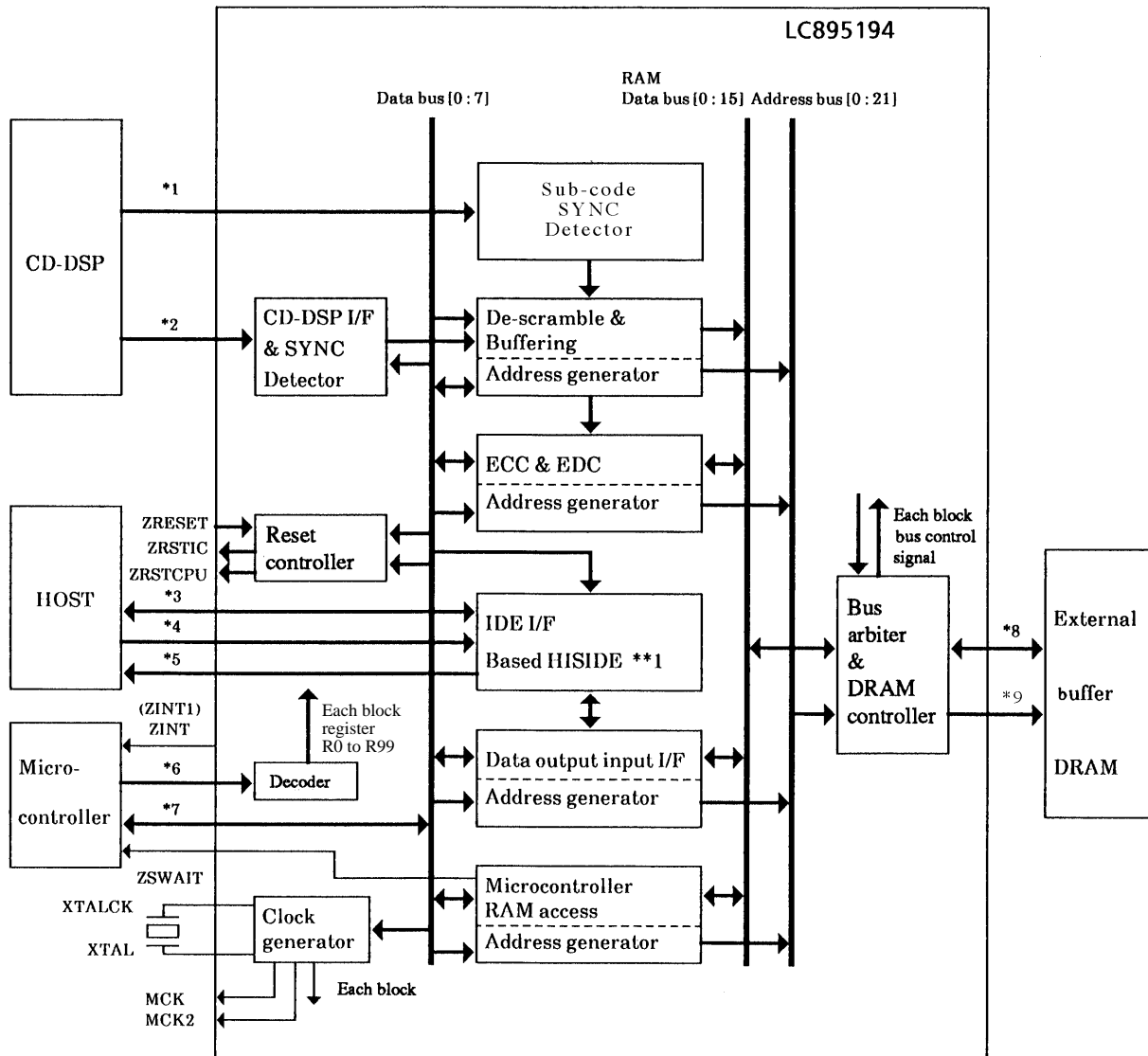
$R2 = \text{None}$

$C1 = 5\text{ pF}$

For a crystal oscillator frequency of 33.8688 MHz.

For an oscillator frequency of 33.8688, the third harmonic is used. This means that precise component values will be influenced by the printed circuit board. Consult the manufacturer of the crystal to determine the circuit constants for this frequency.

Block Diagram



- Note: 1. WFCK, SCOR
 2. BCK, SDATA, LRCK, C2PO
 3. DD0 to DD15, ZDASP, ZPDIAG
 4. ZCS1FX, ZCS3FX, DA0 to DA2, ZDIOR, ZDIOW, ZDMACK
 5. DMARQ, HINTRQ, ZIOCS16, IORDY, ZHRST
 6. ZRD, ZWR, SUA0 to SUA6, ZCS, CSCTRL
 7. D0 to D7
 8. IO0 to IO15
 9. RA0 to RA9, ZRAS0, ZRAS1, ZCAS0, ZCAS1, ZOE, ZUWE, ZLWE

Note: HISIDE (WD25C32) is made by WESTERN DIGITAL.

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Pin Functions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
1	V _{SS0}	P	
2	ZRAS0	O	Buffer DRAM RAS signal output 0 (This pin is used normally.)
3	ZRAS1	O	Buffer DRAM RAS signal output 1
4	V _{SS0}	P	
5	ZCAS0	O	Buffer DRAM CAS signal output 0 (This pin is used normally.)
6	ZCAS1	O	Buffer DRAM CAS signal output 1
7	V _{SS0}	P	
8	ZOE	O	Buffer RAM output enable
9	ZUWE	O	Buffer RAM upper write enable
10	ZLWE	O	Buffer RAM lower write enable
11	RA0	O	RA0 to RA9 are the data buffer DRAM address lines.
12	RA1	O	
13	RA2	O	
14	RA3	O	
15	RA4	O	
16	RA5	O	
17	RA6	O	
18	V _{DD}	P	
19	V _{SS0}	P	
20	RA7	O	RA0 to RA9 are the data buffer DRAM address lines.
21	RA8	O	
22	RA9	O	
23		NC	
24		NC	
25	TEST0	NC	Test pins.
26	TEST1	NC	
27	TEST2	NC	
28	TEST3	NC	
29		NC	
30	IO0	B	Data buffer RAM data I/O These pins have built-in pull-up resistors.
31	IO1	B	
32	IO2	B	
33	IO3	B	
34	IO4	B	
35	IO5	B	
36	V _{SS0}	P	
37	V _{DD}	P	
38	IO6	B	Data buffer RAM data I/O These pins have built-in pull-up resistors.
39	IO7	B	
40	IO8	B	
41	IO9	B	
42	IO10	B	
43	IO11	B	
44	IO12	B	
45	IO13	B	
46	IO14	B	
47	IO15	B	
48	EXCK	O	SUB-CODE input/out pin
49	WFCK	I	
50	SBSO	I	
51	SCOR	I	

- Note:
1. NC (no connection) pins must be left open.
 2. Pin names (signal names) that begin with a Z have negative (inverted) logic.
 3. V_{SS0} is the logic system ground and V_{SS1} is the IDE interface driver ground.

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
52	V _{SS0}	P	
53	V _{SS0}	P	
54	TEST4	I	Test input. This pin must be tied low.
55	V _{SS0}	P	
56	V _{SS0}	P	
57	ZINT1	O	Interrupt request signal output to the microcontroller from the IDE block
58	V _{SS0}	P	
59	V _{SS0}	P	
60	V _{SS0}	P	
61		NC	
62		NC	
63	V _{SS0}	P	
64	SDATA	I	CD-DSP interface
65	BCK	I	
66	LRCK	I	
67	C2PO	I	
68	MCK2	O	XTALCK 1/1, 1/2, 1/512, and stop output
69	V _{SS0}	P	
70	XTALCK	I	Crystal oscillator input
71	XTAL	O	Crystal oscillator output
72	V _{SS0}	P	
73	V _{DD}	P	
74	MCK	O	XTALCK 1/1, 1/2, and stop output
75	V _{SS0}	P	
76	ZRSTIC	O	Reset signal to drive reset IC
77	CSCTRL	I	Selects active high or active low for the microcontroller CS line.
78	ZRESET	I	LSI reset
79	ZRD	I	Microcontroller data read signal input
80	ZWR	I	Microcontroller data write signal input
81	ZCS	I	Input for the register chip select signal from the microcontroller
82	V _{SS0}	P	
83	SUA0	I	Microcontroller register select signals
84	SUA1	I	
85	SUA2	I	
86	SUA3	I	
87	SUA4	I	
88	SUA5	I	
89	SUA6	I	
90	V _{DD}	P	
91	V _{SS0}	P	
92	D0	B	Microcontroller data signals These pins have built-in pull-up resistors.
93	D1	B	
94	D2	B	
95	D3	B	
96	D4	B	
97	D5	B	
98	D6	B	
99	D7	B	
100	ZINT	O	Interrupt request signal output to the microcontroller

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
101	ZRSTCPU	O	Reset signal to CPU
102	ZSWAIT	O	Wait signal output to the microcontroller
103	ZHRST	I	ATAPI control signals
104	ZDASP	B	
105	ZCS3FX	I	
106	ZCS1FX	I	
107	DA2	I	
108	V _{SS0}	P	
109	V _{DD}	P	
110	DA0	I	ATAPI control signals
111	ZPDIAG	B	
112	DA1	I	
113	ZIOCS16	O	
114	HINTRQ	O	
115	ZDMACK	I	
116	V _{SS1}	P	
117	IORDY	O	ATAPI control signals
118	ZDIOR	I	
119	ZDIOW	I	
120	DMARQ	O	
121	DD15	B	ATAPI data bus
122	V _{SS1}	P	
123	DD0	B	ATAPI data bus
124	DD14	B	
125	DD1	B	
126	DD13	B	
127	V _{SS1}	P	
128	V _{DD}	P	
129	DD2	B	ATAPI data bus
130	DD12	B	
131	DD3	B	
132	V _{SS1}	P	
133	DD11	B	ATAPI data bus
134	DD4	B	
135	DD10	B	
136	V _{SS1}	P	
137	V _{DD}	P	
138	DD5	B	ATAPI data bus
139	DD9	B	
140	DD6	B	
141	V _{SS1}	P	
142	DD8	B	ATAPI data bus
143	DD7	B	
144	V _{DD}	P	

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