Ordering number: EN※3981

CMOS LSI

No. ※3981

LC89581

Encoder for CD-ROM and CD-I Data

SANYO

Preliminary

Overview

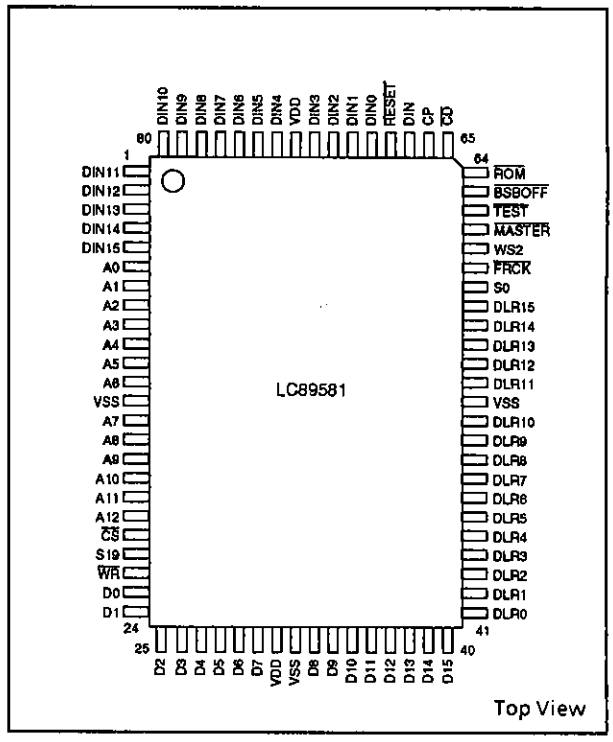
The LC89581 is an encoder for CD-ROM and CD-I data formats. It accepts 16-bit parallel input data, generates error detection and correction codes, and performs bit scrambling. It can operate in either master or slave mode.

The LC89581 operates from a 5 V supply and is available in 80-pin QIPs.

Features

- Encodes CD-ROM and CD-I format data
- Generates error detection and correction codes
- Selectable bit scrambling
- Selectable master/slave operation
- Automatic CD-ROM data format recognition
- 5 V supply
- 80-pin QIP

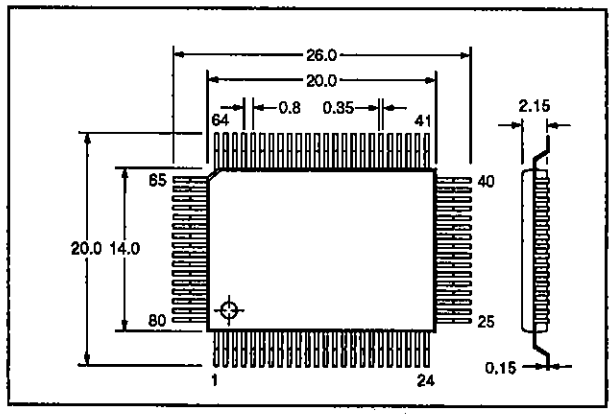
Pin Assignment



Package Dimensions

unit: mm

3044B-QIP80A



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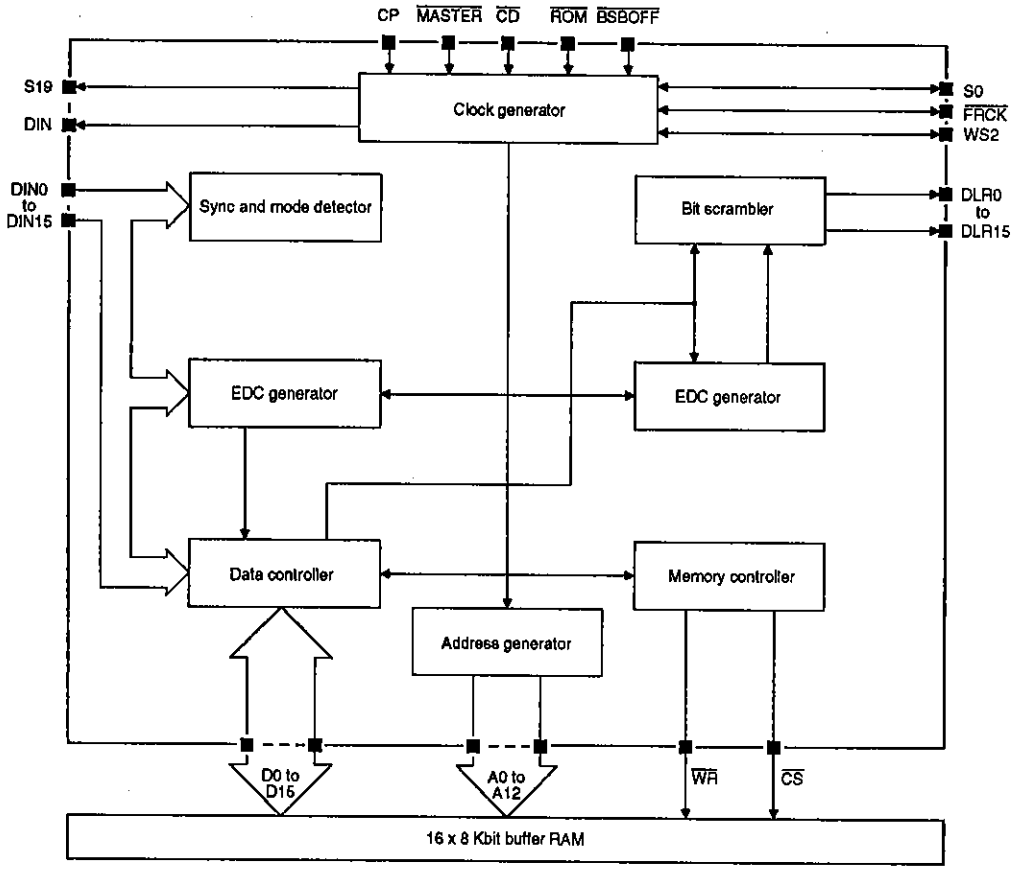
Block Diagram



Pin Functions

Number	Name	Function
69 to 72, 74 to 80, 1 to 5	DIN0 to DIN15	Data inputs
6 to 12, 14 to 19	A0 to A12	Buffer memory address bus
13, 32, 52	VSS	Ground
20	$\overline{CS}$	Buffer memory chip select output
21	S19	Input data start pulse output
22	$\overline{WR}$	Buffer memory write output
23 to 30, 33 to 40	D0 to D15	Buffer memory data bus
31, 73	VDD	Supply voltage
41 to 51, 53 to 57	DLR0 to DLR15	Encoded data outputs
58	S0	Data output sector input/output. See note.
59	$\overline{FRCK}$	CD frame sync clock input/output. See note.
60	WS2	Double word sync clock input/output. See note.
61	$\overline{MASTER}$	Slave/master mode select input. See note.
62	$\overline{TEST}$	Test input. Internal pull-up resistor
63	$\overline{BSBOFF}$	Bit scamble select input. Internal pull-up resistor

Number	Name	Function
64	$\overline{ROM}$	CD-ROM or CD-I input data format select input. Internal pull-up resistor
65	$\overline{CD}$	CD-ROM/CD-I or CD-DA input data format select input. Internal pull-up resistor
66	CP	Clock pulse input
67	DIN	Data input clock output
68	$\overline{RESET}$	Reset input

Note

$\overline{MASTER}$ selects whether S0, $\overline{FRCK}$ and WS2 are in input or output mode.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD}	−0.3 to 7.0	V
Input voltage range	V_I	−0.3 to V_{DD} + 0.3	V
Output voltage range	V_O	−0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	−30 to 70	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Soldering temperature	T_{sol}	260	°C
Soldering time	t_{sol}	10	s

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD}	4.5 to 5.5	V

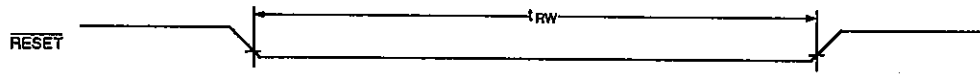
Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −30 to 70 °C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
LOW-level input voltage	V_{IL}		–	–	0.8	V
HIGH-level input voltage	V_{IH}		2.2	–	–	V
Input voltage	V_I		0	–	V_{DD}	V
LOW-level output voltage	V_{OL}	I_{OL} = 3 mA	–	–	0.4	V
HIGH-level output voltage	V_{OH}	I_{OH} = 3 mA	2.4	–	–	V

Timing Characteristics

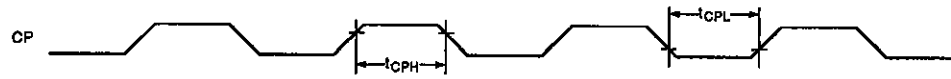
Reset timing



V_{DD} = 4.5 to 5.5 V, T_a = −30 to 70 °C, C_L = 50 pF, V_H = 2.2 V, V_L = 0.8 V

Parameter	Symbol	Ratings		Unit
		min	max	
$\overline{\text{RESET}}$ LOW-level pulsewidth	t_{RW}	$10/f_{CP}$	–	ns

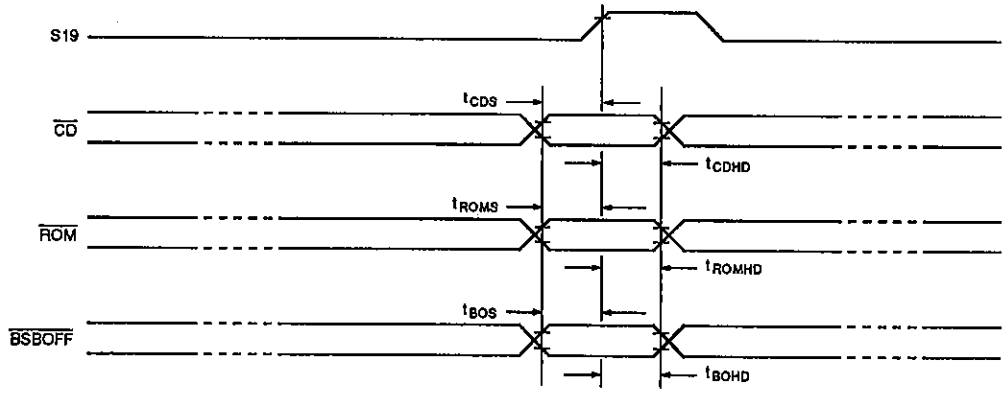
System clock timing



V_{DD} = 4.5 to 5.5 V, T_a = −30 to 70 °C, C_L = 50 pF, V_H = 2.2 V, V_L = 0.8 V

Parameter	Symbol	Ratings			Unit
		min	typ	max	
CP input frequency	f_{CP}	–	4.3218	–	MHz
CP LOW-level pulsewidth	t_{CPL}	80	–	–	ns
CP HIGH-level pulsewidth	t_{CPH}	80	–	–	ns

Encode mode set timing

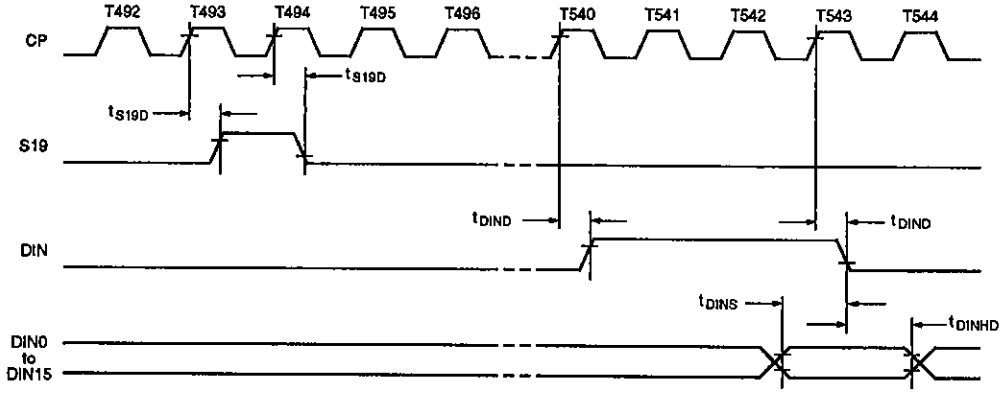


V_{DD} = 4.5 to 5.5 V, T_a = −30 to 70 °C, C_L = 50 pF, V_H = 2.2 V, V_L = 0.8 V

Parameter	Symbol	Ratings		Unit
		min	max	
$\overline{\text{CD}}$ setup time	t_{CDS}	–	30	ns
$\overline{\text{CD}}$ hold time	t_{CDHD}	–	5	ns
$\overline{\text{ROM}}$ setup time	t_{ROMS}	–	30	ns

Parameter	Symbol	Ratings		Unit
		min	max	
$\overline{ROM}$ hold time	t_{ROMHD}	–	5	ns
$\overline{BSBOFF}$ setup time	t_{BOS}	–	30	ns
$\overline{BSBOFF}$ hold time	t_{BOHD}	–	5	ns

Data input timing



V_{DD} = 4.5 to 5.5 V, T_a = –30 to 70 °C, C_L = 50 pF, V_H = 2.2 V, V_L = 0.8 V

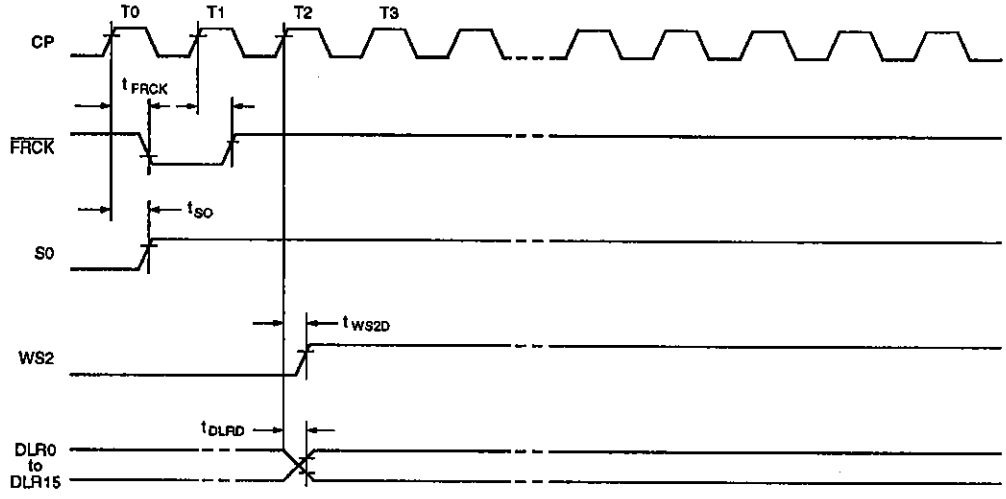
Parameter	Symbol	Ratings		Unit
		min	max	
S19 output delay time	t_{S19D}	–	70	ns
DIN output delay time	t_{DIND}	–	70	ns
DIN0 to DIN15 setup time	t_{DINS}	–	$2/f_{CP}$ + 70	ns
DIN0 to DIN15 hold time	t_{DINHD}	–	0	ns

Note

There are 588 CP cycles for each $\overline{FRCK}$ cycle. $\overline{FRCK}$ goes LOW in sync with the first cycle of CP (T0). DIN goes HIGH on the leading edge of CP cycles T44, T90, T136, T182, T228, T274, T320, T366, T412, T458, T540 and T586.

Data output timing

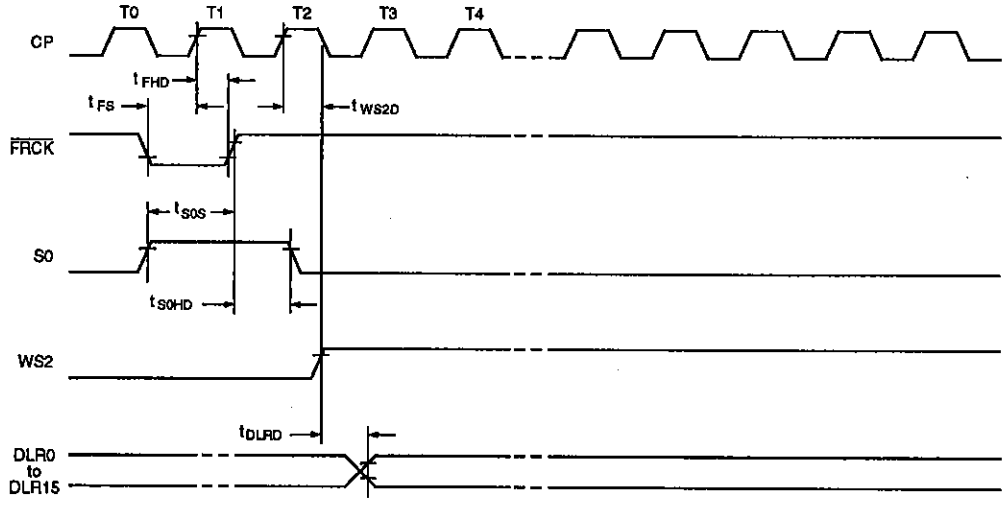
Master mode



V_{DD} = 4.5 to 5.5 V, T_a = –30 to 70 °C, C_L = 50 pF, V_H = 2.2 V, V_L = 0.8 V

Parameter	Symbol	Ratings		Unit
		min	max	
FRCK output delay time	t_{FD}	–	50	ns
SO output delay time	t_{SOD}	–	60	ns
WS2 output delay time	t_{WS2D}	–	50	ns
DLR0 to DLR15 output delay time	t_{DLRD}	–	100	ns

Slave mode

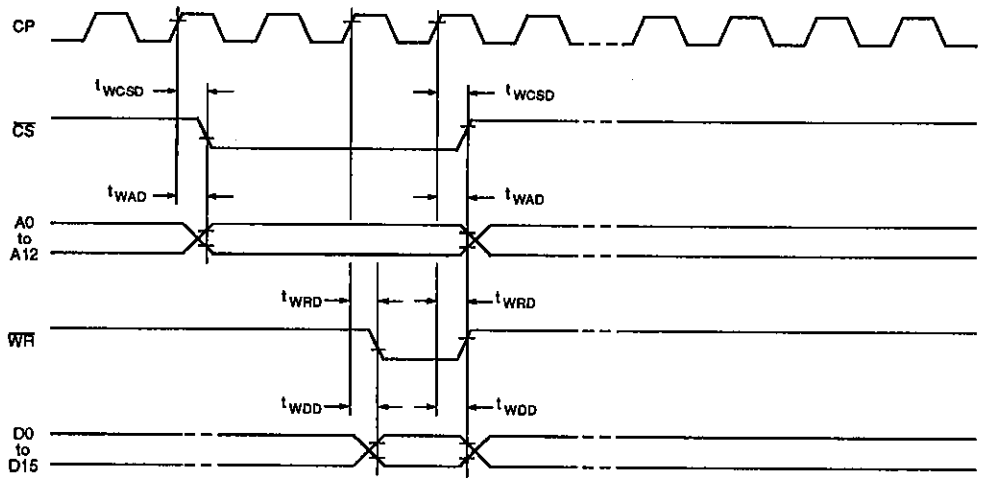


V_{DD} = 4.5 to 5.5 V, T_a = –30 to 70 °C, C_L = 50 pF, V_H = 2.2 V, V_L = 0.8 V

Parameter	Symbol	Ratings		Unit
		min	max	
FRCK input setup time	t_{FS}	5	–	ns
FRCK input hold time	t_{FHD}	10	–	ns

Parameter	Symbol	Ratings		Unit
		min	max	
SO input setup time	t_{SOS}	5	–	ns
SO input hold time	t_{SOHD}	10	–	ns
WS2 input delay time	t_{WS2D}	10	100	ns
DLR0 to DLR15 output delay time	t_{DLRD}	–	80	ns

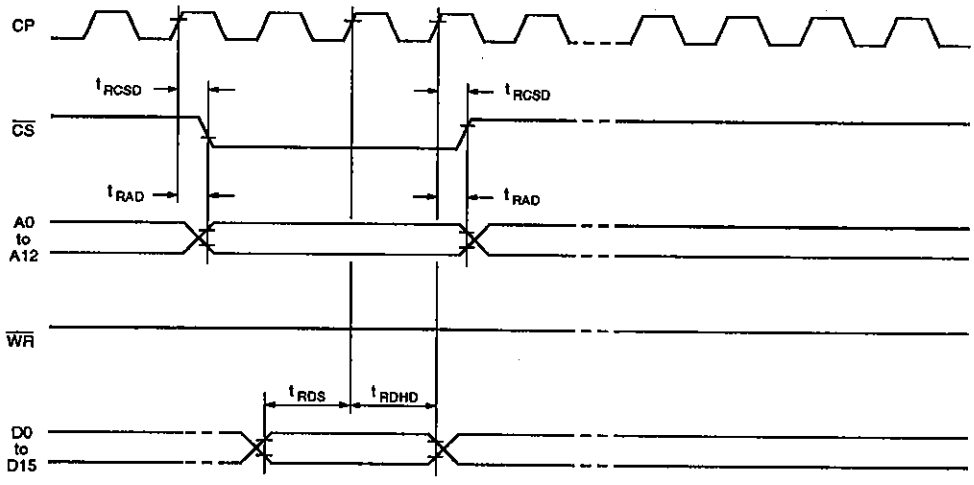
SRAM interface write cycle



V_{DD} = 4.5 to 5.5 V, T_a = –30 to 70 °C, C_L = 50 pF, V_H = 2.2 V, V_L = 0.8 V

Parameter	Symbol	Ratings		Unit
		min	max	
$\overline{CS}$ output delay time	t_{WCSD}	–	80	ns
A0 to A12 output delay time	t_{WAD}	–	100	ns
$\overline{WR}$ output delay time	t_{WRD}	–	60	ns
D0 to D15 output delay time	t_{WDD}	–	100	ns

SRAM interface read cycle



V_{DD} = 4.5 to 5.5 V, T_a = –30 to 70 °C, C_L = 50 pF, V_H = 2.2 V, V_L = 0.8 V

Parameter	Symbol	Ratings		Unit
		min	max	
$\overline{CS}$ output delay time	t_{RCSD}	–	70	ns
A0 to A12 address output delay time	t_{RAD}	–	100	ns
D0 to D15 input setup time	t_{RDS}	–	80	ns
D0 to D15 input hold time	t_{RDHD}	–	5	ns

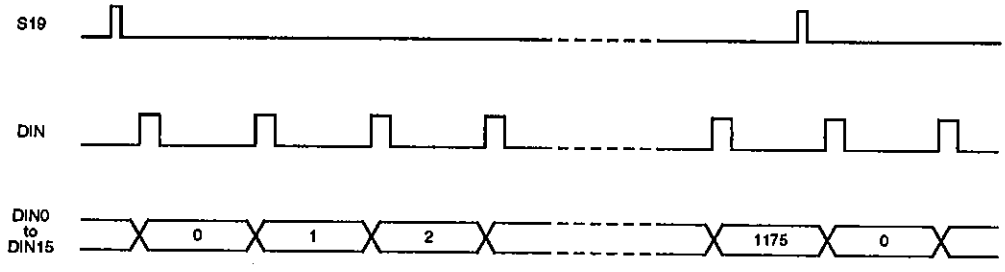
Functional Description

Input data is processed as CD-DA format data when $\overline{CD}$ is LOW and as CD-ROM or CD-I format data when $\overline{CD}$ is HIGH, depending on the state of $\overline{ROM}$. The data is processed as CD-ROM format data when $\overline{ROM}$ is LOW, and as CD-I format data when $\overline{ROM}$ is HIGH. Note that if a CD-ROM sync pattern is not detected in the input data, the data is processed as CD-DA format data, regardless of whether $\overline{CD}$ is LOW or HIGH.

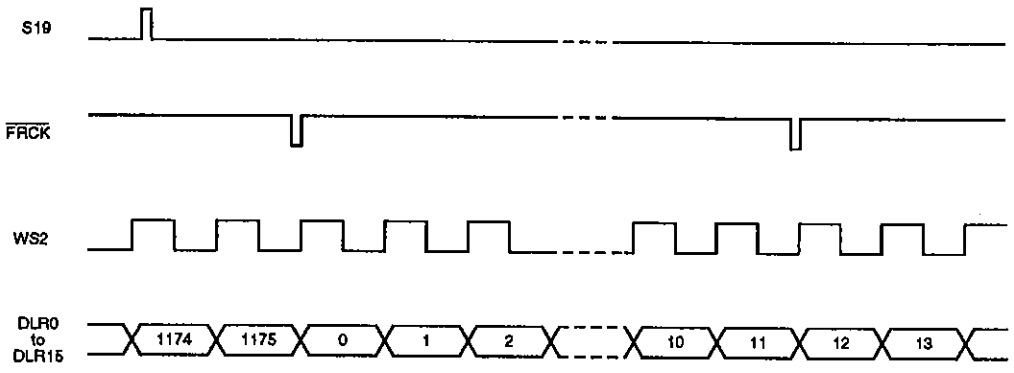
In CD-ROM or CD-I format data processing modes, bit scrambling is OFF when $\overline{BSBOFF}$ is LOW, and ON when $\overline{BSBOFF}$ is HIGH.

When $\overline{MASTER}$ is LOW, master operation mode is selected and WS2, $\overline{FRCK}$ and S0 are outputs. When $\overline{MASTER}$ is HIGH, slave operation mode is selected and WS2, $\overline{FRCK}$ and S0 are inputs.

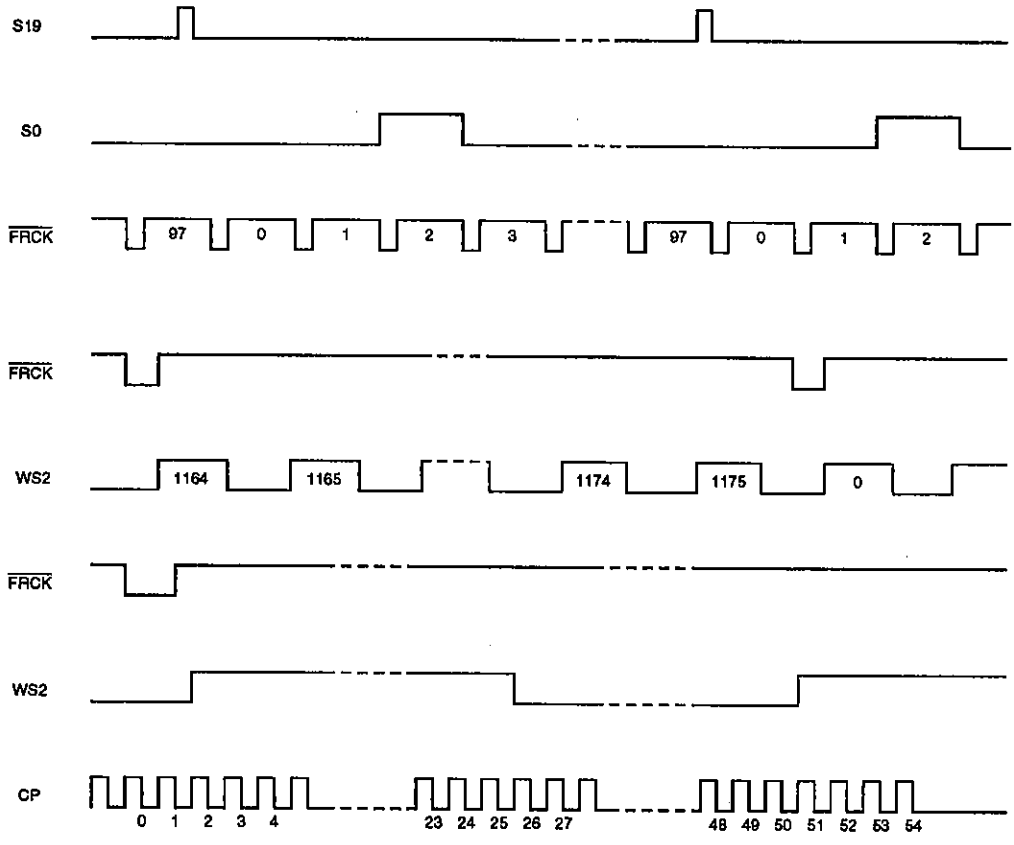
The data input sequence is shown in the following figure. After S19 goes LOW, data is read from DIN0 goes DIN15 when DIN goes HIGH.



The data output sequence is shown in the following figure. Note that encoded data output lags 2 sectors behind the input.



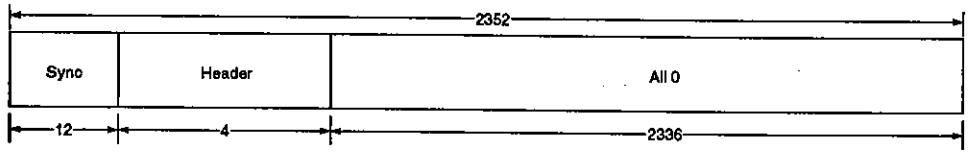
The timing of S0, FRCK, WS2 and CP is shown in the following figure



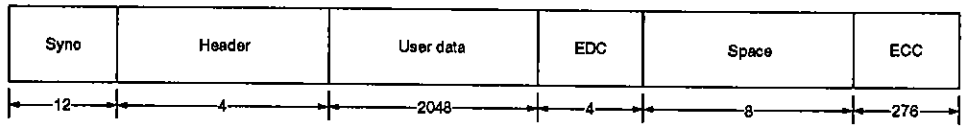
Data Formats

CD-ROM

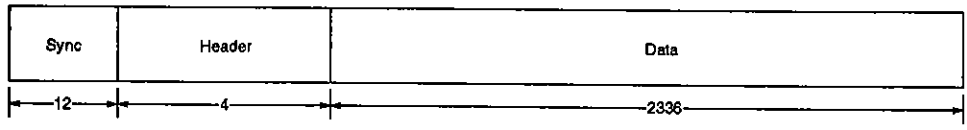
Mode 0



Mode 1

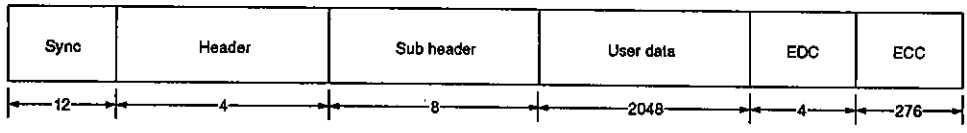


Mode 2



CD-I

Mode 2, form 1



Mode 2, form 2