Ordering number : EN*5784

CMOS LSI

LC895925

Signal Processing LSI for CD-R Drives

Preliminaly

Overview

The LC895925 provides the following signal processing functions for CD-R drives: CD-ROM decoding/encoding (complete with ECC processing for the former), subcode decoding/encoding, CD encoding, ATIP decoding, CLV servo, and SCSI interface registers.

Features

- CD-ROM decoding/encoding complete with error detection and error correction
- Subcode decoding/encoding complete with error correction
- ATIP decoding and CRC checking for both encoding and decoding
- CLV servo control using ATIP data during encoding
- CIRC code insertion and EFM modulation during encoding
- Support for PCA random EFM output during encoding
- Support for CD-ReWritable (CD-RW) Write Strategy signal output
- Access to buffer RAM from microcontroller via LC895925
- Built-in SCSI interface
- Speeds of 12× for decoding and 4× for encoding
  - — Frequencies
    Decoding: 17.2872 MHz
    Encoding: 17.2872 MHz without Write Strategy support
    69.1488 MHz with Write Strategy support
- Transfers speeds of 10 megabytes/s (synchronous) and 5 megabytes/s (asynchronous) with 16 80-ns DRAMs *1
- Buffer RAM sizes between 1 and 32 megabits (using 16-bit DRAMs)
- User control over sizes of CD main channel, C2 flag, and subcode areas in buffer RAM
- Built-in batch transfer function for transferring entire CD main channel, C2 flag, or subcode area in a single operation
- Built-in multiblock transfer function for transferring multiple blocks in a single operation

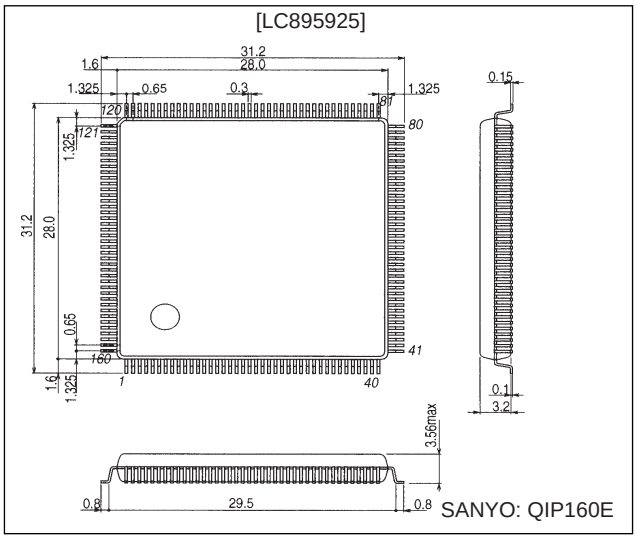
Notes:

1. Using a SCSI master clock of 20 MHz with speeds up to 8×.
2. Using a SCSI master clock of 17.2872 MHz with speeds up to 4×.

Package Dimensions

unit: mm

3153A-QFP160E



Specifications

Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	V_{DD} max		–0.3 to +7.0	V
I/O voltage	V_I, V_O		–0.3 to V_{DD}+0.3	V
Maximum power dissipation	Pd max	Ta ≤ 70°C	600	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Solder resistance		10 seconds	260	°C

Permissible Operating Range at Ta = –30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics at Ta = –30 to +70°C, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage	V_{IH}	TTL levels, for pin types 1 and 6	2.2			V
Input low level voltage	V_{IL}				0.8	V
Input high level voltage	V_{IH}	TTL levels, for pin type 4, with pull-up resistors	2.2			V
Input low level voltage	V_{IL}				0.8	V
Input high" level voltage	V_{IH}	TTL levels, for pin 0 and 7, with Schmitt inputs	2.5			V
Input low level voltage	V_{IL}				0.6	V
Output high level voltage	V_{OH}	I_{OH} = –2 mA, for pin type 3	V_{DD} – 2.1			V
Output low level voltage	V_{OL}	I_{OL} = 2 mA, for pin type 3			0.4	V
Output high level voltage	V_{OH}	I_{OH} = -2 mA, for pin types 2, 4, and 6	V_{DD} – 2.1			V
Output low level voltage	V_{OL}	I_{OL} = 2 mA, for pin types 2, 4, and 6			0.4	V
Output high level voltage	V_{OH}	I_{OH} = -48 mA, for pin type 7	V_{DD} – 2.1			V
Output low level voltage	V_{OL}	I_{OL} = 48 mA, for pin type 7			0.4	V
Output low level voltage	V_{OL}	I_{OL} = 2 mA, for pin type 5			0.4	V
Input leak current	I_{IL}	V_I = V_{SS}, V_{DD}, for pin types 0, 1, 6, and 7	–10		+10	µA
Pull-up resistance	R_{UP}	For pin types 4 and 5	40	80	160	kΩ

The pin types above refer to the following groups.

Input

(0) BCK, BICLKIN, BIDATAI, C2PO, LOCKIN, LRCK, PLLOUTIN, ROUGH, SBSO, SCOR, SDATA, WFCK, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$

(1) SUA0 to SUA6, TEST0 to TEST6, X1EN, $\overline{RESET}$

Output

(2) CLV^+, CLV^-, FSW

(3) DATACKO, EFM, EFMG, EFMGATE0 to EFMGATE6, EXCK, LOCK, MCK, MON, PSUBSYNC, RA0 to RA9, SUBSYNC, $\overline{CAS0}$ to $\overline{CAS1}$, $\overline{RAS0}$ to $\overline{RAS1}$, $\overline{ERROR}$, $\overline{EXTACK}$, $\overline{FRCK}$, $\overline{LWE}$, $\overline{UWE}$, $\overline{OE}$

Input/Output

(4) D0 to D7, IO0 to IO15

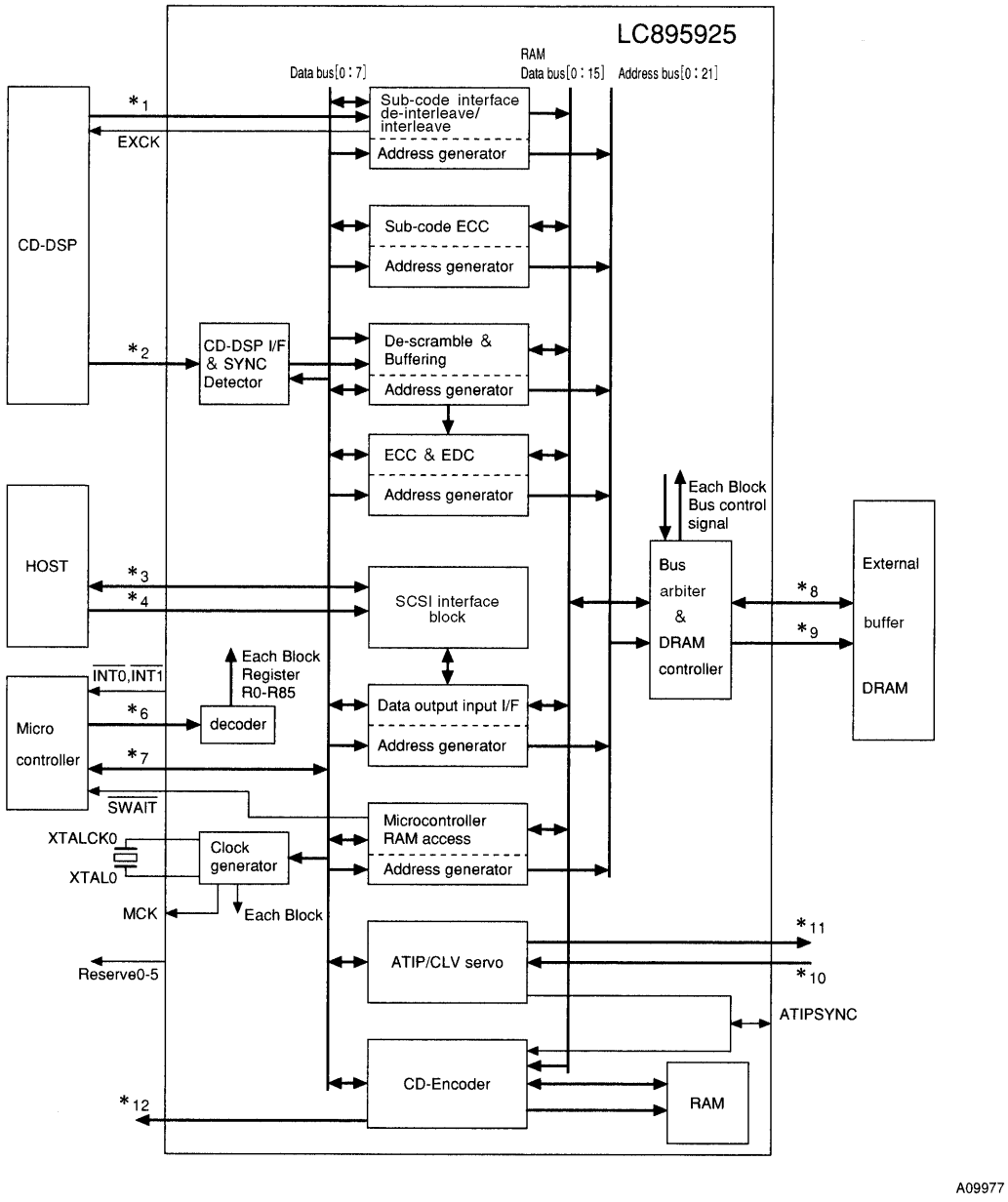
(5) INT0 to INT1, $\overline{SWAIT}$

(6) ATIPSYNC, Reserve0 to Reserve5

(7) $\overline{ACK}$, $\overline{ATN}$, $\overline{BSY}$, C/D, $\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, I/O, $\overline{MSG}$, $\overline{REQ}$, $\overline{RST}$, $\overline{SEL}$

Note: The XTAL0, XTAL1, XTALCK0, and XTALCK1 pins fall outside of these DC characteristic specifications.

Block Diagram



*1 WFCK, SBSO, SCOR
*2 BCK, SDATA, LRCK, C2PO
*3 $\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{BSY}$, $\overline{MSG}$, $\overline{SEL}$, $\overline{RST}$, $\overline{REQ}$, I/O, C/D
*4 $\overline{ACK}$, $\overline{ATN}$
*6 $\overline{RD}$, $\overline{WR}$, SUA0 to SUA6, $\overline{CS}$
*7 D0 to D7
*8 IO0 to IO15
*9 RA0 to RA9, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS0}$, $\overline{CAS1}$, $\overline{OE}$, $\overline{UWE}$, $\overline{LWE}$
*10 PLLOUTIN, ROUGH, LOCKIN, BICLKIN, BIDATAIN
*11 $\overline{ERROR}$, LOCK, CLV^{+} (MDP), CLV^{-} (MDS), MON, FSW
*12 SUBSYNC, PSUBSYNC, $\overline{FRCK}$, EFM, EFMG, EFMGATE3 to EFMGATE0, $\overline{EXTACK}$, DATACK0

Pin Descriptions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
1	V_{SS}	P	
2	Reserve0	B	Reserved for future expansion (leave open)
3	Reserve1	B	Reserved for future expansion (connect to ground)
4	Reserve2	B	Reserved for future expansion (connect to ground)
5	TEST1	I	Test pin (connect to V_{SS})
6	XTALCK0	I	Crystal oscillator circuit input pin (17.2872 to 69.1488 MHz)
7	XTAL0	O	Crystal oscillator circuit output pin
8	TEST2	I	Test pin (connect to V_{SS})
9	MCK	O	Master Clock output pin
10	TEST3	I	Test pin (connect to V_{SS})
11	XTALCK1	I	Crystal oscillator circuit input pin (20 MHz)
12	XTAL1	O	Crystal oscillator circuit output pin
13	TEST4	I	Test pin (connect to V_{SS})
14	V_{DD}	P	
15	V_{SS}	P	
16	CLV^{+} (MDP)	O	CLV servo signal output pins
17	CLV^{-} (MDS)	O	
18	MON	O	
19	FSW	O	
20	V_{DD}	P	
21	V_{SS}	P	
22	PLLOUTIN	I	Wobble signal carrier clock input pin
23	ROUGH	I	Rough CLV servo wobble signal input pin
24	LOCKIN	I	CD decoder lock signal input pin
25	LOCK	O	CLV servo lock monitor pin
26	$\overline{\text{ERROR}}$	O	ATIP parity error detection pin
27	ATIPSYNC	B	ATIP synchronization signal I/O pin
28	BIDATAI	I	Biphase data input pin
29	BICLKIN	I	Biphase data transfer clock input pin
30	V_{DD}	P	
31	IO0	B	Data signal pins for ROM encoder/decoder buffer RAM, with pull-up resistors
32	IO1	B	
33	IO2	B	
34	IO3	B	
35	IO4	B	
36	IO5	B	
37	IO6	B	
38	IO7	B	
39	IO8	B	
40	V_{DD}	P	
41	V_{SS}	P	

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
42	IO9	B	Data signal pins for ROM encoder/decoder DRAM, with pull-up resistors
43	IO10	B	
44	IO11	B	
45	IO12	B	
46	IO13	B	
47	IO14	B	
48	IO15	B	
49	V_{SS}	P	
50	RA0	O	Address signal pins for ROM encoder/decoder DRAM
51	RA1	O	
52	RA2	O	
53	RA3	O	
54	RA4	O	
55	RA5	O	
56	RA6	O	
57	RA7	O	
58	RA8	O	
59	RA9	O	
60	V_{DD}	P	
61	V_{SS}	P	
62	$\overline{RAS0}$	O	DRAM $\overline{RAS}$ signal output pins
63	$\overline{RAS1}$	O	
64	$\overline{CAS0}$	O	DRAM $\overline{CAS}$ signal output pins
65	$\overline{CAS1}$	O	
66	$\overline{OE}$	O	DRAM Output Enable signal output pin
67	$\overline{UWE}$	O	DRAM Output Upper Write Enable signal output pin
68	$\overline{LWE}$	O	DRAM Output Lower Write Enable signal output pin
69	TEST0	I	Test pin (connect to V_{SS})
70	V_{DD}	P	
71	EXCK	O	Subcode data read shift clock output pin
72	WFCK	I	Subcode frame synchronization input pin
73	SBSO	I	Subcode serial data input pin
74	SCOR	I	Subcode block synchronization input pin
75	V_{SS}	P	
76	BCK	I	Serial data input clock input pin
77	SDATA	I	Serial data input pin
78	LRCK	I	44.1-kHz strobe signal input pin
79	C2PO	I	C2 pointer input pin
80	V_{DD}	P	
81	V_{SS}	P	
82	$\overline{DB0}$	B	SCSI pins
83	$\overline{DB1}$	B	
84	V_{DD}	P	
85	$\overline{DB2}$	B	SCSI pins
86	$\overline{DB3}$	B	
87	VSS	P	
88	$\overline{DB4}$	B	SCSI pins
89	$\overline{DB5}$	B	

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
90	V_{DD}	P	
91	$\overline{DB6}$	B	SCSI pins
92	V_{DD}	P	
93	V_{SS}	P	
94	$\overline{DB7}$	B	SCSI pins
95	$\overline{DBP}$	B	
96	V_{DD}	P	
97	V_{SS}	P	
98	$\overline{ATN}$	B	SCSI pins
99	$\overline{BSY}$	B	
100	V_{DD}	P	
101	V_{SS}	P	
102	$\overline{ACK}$	B	SCSI pins
103	$\overline{RST}$	B	
104	V_{DD}	P	
105	V_{SS}	P	
106	$\overline{MSG}$	B	SCSI pins
107	$\overline{SEL}$	B	
108	V_{DD}	P	
109	C/D	B	SCSI pins
110	V_{DD}	P	
111	$\overline{REQ}$	B	SCSI pins
112	I/O	B	
113	V_{SS}	P	
114	X1EN	I	Pin for selecting SCSI interface clock (XTALCK0 or XTALCK1)
115	$\overline{RESET}$	I	RESET pin
116	V_{DD}	P	
117	DATACKO	O	4.3218-MHz (Normal Speed) oscillator output pin
118	PSUBSYNC	O	Pseudo subcode synchronization output pin
119	$\overline{EXTACK}$	O	ATIP synchronization interval acknowledgment output pin
120	V_{DD}	P	
121	V_{SS}	P	
122	SUBSYNC	O	Subcode synchronization signal output pin
123	$\overline{FRCK}$	O	EFM frame synchronization signal output pin
124	FRCK	O	EFM output gate signal output pin
125	EFM	O	EFM signal output pin
126	EFMGATE0	O	EFM pulse width detection gate signals
127	EFMGATE1	O	
128	EFMGATE2	O	
129	EFMGATE3	O	
130	TEST5	I	Test pin (connect to V_{SS})
131	V_{SS}	P	
132	TEST6	I	Test pin (connect to V_{SS})

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
133	SUA0	I	Command register selection address input pinsI
134	SUA1	I	
135	SUA2	I	
136	SUA3	I	
137	SUA4	I	
138	SUA5	I	
139	SUA6	I	
140	V_{DD}	P	
141	V_{SS}	P	
142	D0	B	Microcontroller data signal pins, with pull-up resistors
143	D1	B	
144	D2	B	
145	D3	B	
146	D4	B	
147	D5	B	
148	D6	B	
149	D7	B	
150	V_{DD}	P	
151	$\overline{CS}$	I	Chip select signal from microcontroller
152	$\overline{RD}$	I	Data read signal from microcontroller
153	$\overline{WR}$	I	Data write signal from microcontroller
154	$\overline{SWAIT}$	O	Wait signal to microcontroller
155	$\overline{INT0}$	O	Interrupt request signals to microcontroller. Open drain outputs with built-in pull-up resistors
156	$\overline{INT1}$	O	
157	Reserve3	B	Reserved for future expansion (leave open)
158	Reserve4	B	
159	Reserve5	B	
160	V_{DD}	P	