

### Conversion from the Intel® TE28F128J3A(C)-120 to the SHARP LH28F128SPHT-PTL12

#### DEVICE ID

Table 1. Device ID

PART NUMBER	TE28F128J3A	LH28F128SPHT
Manufacturer ID	0089H	00B0H
Device ID	0018H	0018H

#### COMMAND DIFFERENCES

The commands for the Intel device are supported by the SHARP device. However, during the first bus cycle, the Word Address or Block Address must be on the address bus. Typically, software is written to include these addresses on the address bus so that this is not an issue. If a problem does occur because the Word Address or Block Address is not on the address bus during the first bus cycle, a minor software change is required to ensure that no problems occur in the future. See Table 2 for the software command differences between the Intel and SHARP devices.

Table 2. Software Command Comparison

COMMAND	ADDRESS BUS		DATA BUS	
	INTEL TE28F128J3A	SHARP LH28F128SPHT	INTEL TE28F128J3A	SHARP LH28F128SPHT
Read ID codes	x + IA or OA	BA + IA or OA	90H + ID or OD	
Read Status Register	x + x	BA + BA	70H	
Clear Status Register	x	BA	50H	
Write to Buffer	BA + BA	WA + WA	E8H + N	
Word/Byte Write	x + WA	WA + WA	40H/10H + D0H	
Block Erase, Program Suspend	x	BA	B0H	
Block Erase, Program Resume	x	BA	D0H	
Set Block Lock Bit	x + BA	BA + BA	60H + 01H	
Erase Block Lock Bit	x + BA	BA + BA	60H + D0H	
OTP Program	x + OA	BA + OA	C0H + OD	

**NOTES:** BA = Any address within the block  
IA = Identifier code address  
OA = Address of OTP area to be read or programmed  
ID = Identifier code data  
WA = Word program address  
x = Any address within Flash memory area  
N = Number of words to be programmed  
OD = Data that will be programmed into the OTP location

## PIN DIFFERENCES

Intel's pin 29 has a third Chip Enable line that the SHARP device does not. For customers who use Intel's three CE pins to select between multiple Flash memory chips, some additional logic might be necessary. Typically, boards that only have one or two Flash memory devices will not run into this issue because the extra  $\overline{CE}_2$  pin is tied LOW to reduce current consumption. If the  $\overline{CE}_2$  pin is tied LOW, both the Intel and SHARP devices are accessed in the same way using pins  $\overline{CE}_0$  and  $\overline{CE}_1$ .

Intel's pin 30 is A23, while SHARP's is a Bank Select pin. Under most conditions this difference will not cause an issue; however, a potential compatibility issue may arise because the SHARP device has read while write capabilities. See Table 3 for pin differences between the Intel and SHARP devices.

**Table 3. Pin Differences**

PIN NUMBER	INTEL TE28F128J3A	SHARP LH28F128SPHT
29	$\overline{CE}_2$	NC
30	A23	Bank Select

**NOTE:** NC = No Connect

**SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.**

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