LM1292

LM1292 Video PLL System for Continuous-Sync Monitors

Literature Number: SNOS880

National Semiconductor

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LM1292
Video PLL System for Continuous-Sync Monitors

General Description

The LM1292 is a very low jitter, integrated horizontal time base solution specifically designed to operate in high performance, continuous-sync video monitors. It automatically synchronizes to any H frequency from 22 kHz to 125 kHz and provides the drive pulse to the high power deflection circuit.

Available sync processing includes a vertical sync separator and a composite video sync stripper. An internal sync selection scheme gives highest priority to separate H and V sync, then composite sync, and finally sync on video; no external switching between sync sources is necessary. The LM1292 provides polarity-normalized H/HV and V sync outputs.

The LM1292 design uses an on-chip FVC (Frequency-to-Voltage Converter) to set the center frequency of the VCO (Voltage-Controlled Oscillator). This technique allows autosync operation over the entire frequency range using just one optimized set of external components.

The system includes a second phase detector which compensates for storage time variation in the horizontal output transistor; the picture's horizontal position is thus independent of temperature and component variance.

The LM1292 provides DC control pins for H Drive duty cycle and flyback phase.

Features

- Wide continuous autosync range — 22 kHz–125 kHz (1:5.7) with no component switching or external adjustments
- No manufacturing trims required — internal VCO capacitor trimmed on chip
- No costly high-precision components needed
- Very low phase jitter (below 800 ps at 125 kHz)
- DC controlled H phase and duty cycle
- Video mute pulse for blanking during H frequency transitions
- Input sync prioritization
- Clamp pulse position and width control
- Continuous clamp pulse output, even with no sync input
- Resistor-programmable minimum and maximum VCO frequency
- X-ray input disables H drive and mutes video until V_{CC} powered down
- H drive disabled for $V_{CC} < 9.5V$
- Horizontal output transistor protected against accidental turn-on during flyback
- Capacitor-programmable frequency ramping, df_{vco}/dt, protects H output transistor during scanning mode changes

Connection Diagram

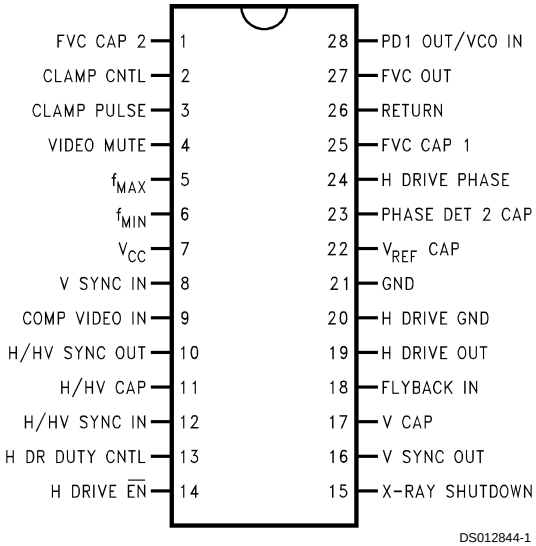


FIGURE 1. Order Number LM1292N
See NS Package Number N28B

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	14V
Input Voltage, V_{DC}	
Pin 14	5V
Pin 24	$1.3V < V_{IN} < 7.2V$
Pins 5, 6	8V
Pins 8, 28	10V
Pins 2, 9, 12, 13, 15, 18	V_{CC}
Power Dissipation (P_D)	2.5W
(Above 25˚C, derate based on θ_{JA} and T_J)	
Thermal Resistance (θ_{JA})	50˚C/W
Junction Temperature (T_J)	150˚C
ESD Susceptibility (Note 5)	2 kV
Storage Temperature	−65˚C to +80˚C
Lead Temperature (Soldering 10 sec.)	265˚C

Operating Ratings (Note 2)

Operating Temperature Range	−20˚C to +80˚C
Supply Voltage	$10.8V \le V_{CC} \le 13.2V$

Electrical Characteristics See Test Circuit (*Figure 2*); T_A = 25˚C; V_{CC} = 12V; V_{14} = 0V; V_{15} = 0V unless otherwise stated

Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units
Supply Current		30	41	mA (max)
Minimum Composite Video Input Amplitude (Pin 9)	Cap Coupled (0.01 µF), Sync Tip to Black Level	0.14		V_{PP}
DC Clamp Level, Composite Video Input		2.0		V
Clamp Charging Current, Composite Video Input		6		mA
Minimum H/HV Sync Input Amplitude (Pin 12)	Cap Coupled, 10% Duty Cycle (Note 8)	1.0		V_{PP}
Minimum V Sync Input Amplitude (Pin 8)	Cap Coupled, 1% Duty Cycle	1.0		V_{PP}
High Level Output Voltage V_{OH} (Pins 10, 16)	I_{OH} = −100 µA	4.3	3.8	V (Min)
Low Level Output Voltage V_{OL} (Pins 10, 16)	I_{OL} = 1.6 mA	0.25	0.4	V (Max)
Video Mute Low Level Output Voltage (Pin 4)	I_{OL} = 2 mA		0.4	V (Max)
Mute Detection Voltage Threshold	ΔV, | FVC Cap 1 - FVC Cap 2 | for Mute Output Low	100		mV
Flyback Input Threshold (Pin 18)	Positive Going Flyback Pulse	1.4		V
Under-Voltage Lockout (Pin 7)	V_{CC} Below Threshold: H Drive Output Open (Unlatched)	10.8		V
Frequency to Voltage Gain	22 kHz ≤ f_H ≤ 125 kHz	0.047		V/kHz
VCO Gain Constant	f_{VCO} = 100 kHz	1.34×10^5		Rad/s/V
PD1 Phase Detector Gain Constant	f_{VCO} = 100 kHz	130		µA/Rad
	f_{VCO} = 60 kHz	78.1		
	f_{VCO} = 22 kHz	28.6		
Frequency to Voltage Linearity	22 kHz ≤ f_H ≤ 125 kHz	1.0		%
VCO Linearity	22 kHz ≤ f_{VCO} ≤ 125 kHz	1.0		%
Jitter	f_H = 30 kHz (Note 9)	3.25		ns p-p
	f_H = 60 kHz	1.45		
	f_H = 100 kHz	895		ps p-p
	f_H = 125 kHz	763		
H Drive Duty Cycle Control Gain	V_{13} = 0V–4V; 30%–70% Allowed	0.11		T_H/V
H Drive Phase Control Gain	V_{24} = 1.5V–7V (Note 10)	32		˚/V
PD1 Phase Detector Leakage Current + VCO Input Bias Current (Pin 28)			1	µA

Electrical Characteristics

See Test Circuit (*Figure 2*); T_A = 25˚C; V_{CC} = 12V; V_{14} = 0V; V_{15} = 0V unless otherwise stated (Continued)

Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units
H Drive Low Level Output Voltage (Pin 19)	I_{OL} = 100 mA	0.7		V
H Drive $\overline{EN}$ Low Level Input Voltage (Pin 14)	H Drive Output Active		0.8	V (Max)
H Drive $\overline{EN}$ High Level Input Voltage (Pin 14)	H Drive Output Open (Unlatched)		2.0	V (Min)
X-Ray Shutdown Threshold Voltage (Pin 15)	V_{15} Above Threshold, H Drive Output Open (Latched)	1.8	1.7 1.9	V (Min) V (Max)
H/HV Sync Out Propagation Delay Change	H/HV In vs Comp Video In	32		ns
Clamp Pulse Width	(Back Porch)R_{SET} = 15 kΩ; V_{SET} = 0V	0.4		µs
	(Back Porch)R_{SET} = 15 kΩ; V_{SET} = 1.5V	1.4		µs
	(Sync Tip)R_{SET} = 15 kΩ; V_{SET} = 4V	0.6		µs
Clamp Pulse Delay	(Back Porch) Trailing Edge H/HV Sync In to Leading Edge Clamp Pulse	0.1		µs
	(Sync Tip) Leading Edge H/HV Sync In to Leading Edge Clamp Pulse	0.025 T_H		s

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any elevated temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{JMAX} = 150˚C. The typical thermal resistance (θ_{JA}) of these parts when board mounted follow: LM1292N 50˚C/W.

Note 5: Human Body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 6: Typical specifications are at T_A = 25˚C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The typical duty cycle range allowed for the H sync tip is from 5%–26%.

Note 9: The standard deviation, σ, of the flyback pulse period is measured with HP 53310A Modulation Domain Analyzer. Peak-to-peak jitter of the flyback pulse is defined by 6σ.

Note 10: Phase Limits: $-0.15 < \phi < \left(0.35 - \frac{t_{DFB}}{T_H}\right)$,

expressed as a fraction of the horizontal period T_H, where T_{DFB} is the horizontal output transistor turn-off delay from the rising edge of H Drive to the FBP peak. A positive phase value represents a phase lead of the FBP peak with reference to the leading edge of H sync.

Test Circuit

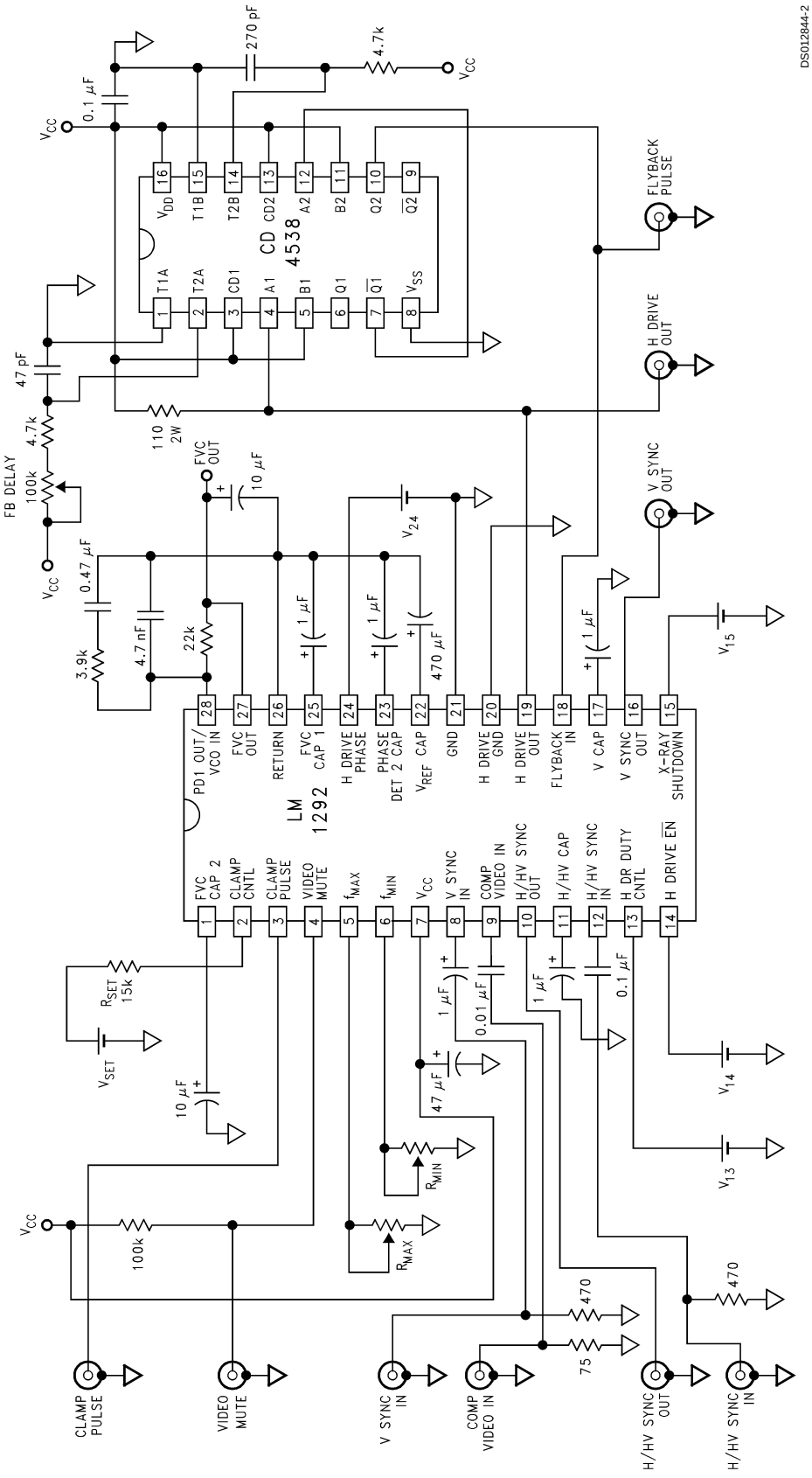


FIGURE 2.

Block Diagram

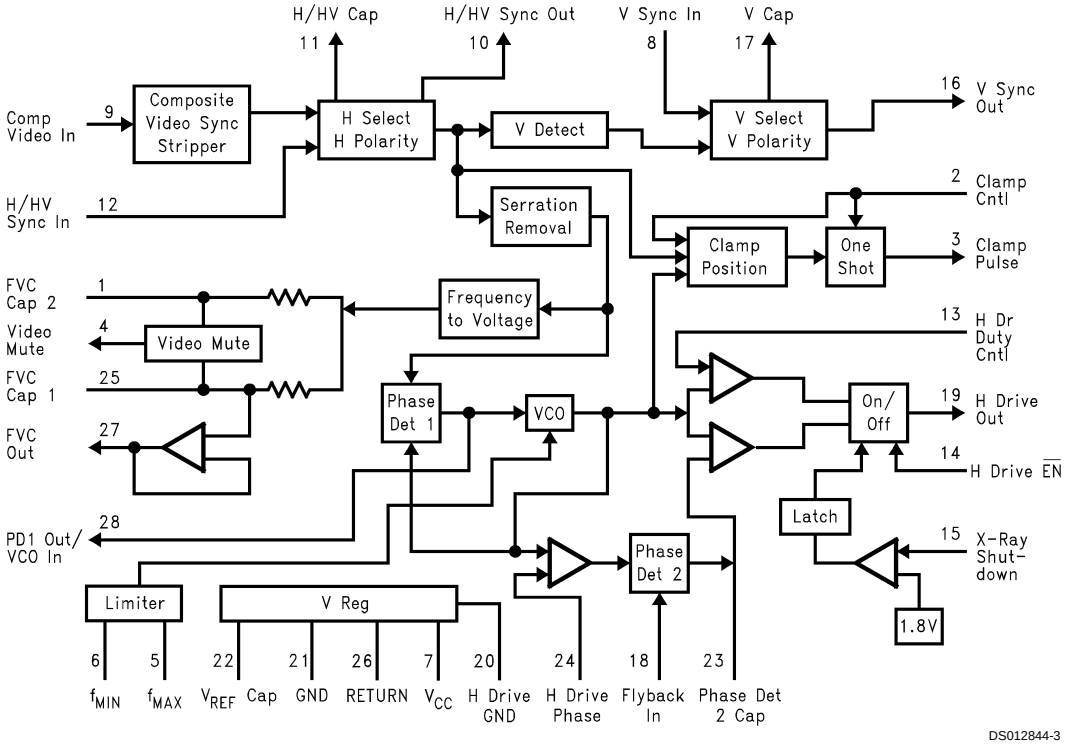


FIGURE 3.

Pin Descriptions

See *Figure 4* through *Figure 14* for input and output schematics.

Pin 1—FVC CAP 2: Secondary FVC filter pin. C_{FVC2} is connected from this pin to ground. The width of the VIDEO MUTE (pin 4) pulse is controlled by the time constant difference between the filters at pins 1 and 25.

Pin 2–CLAMP CNTL: This low-impedance current-mode input pin is internally biased to 2V. The direction of current sets the pulse position (back porch or sync-tip), while the current magnitude sets the pulse width. In a typical application, a control voltage of 0V–4V is applied to this pin through a 15 kΩ resistor. A voltage below 2V positions the pulse on the back porch of the horizontal sync pulse and decreasing voltage narrows the pulse. A voltage above 2V sets the pulse on the H sync-tip (slightly delayed from the leading edge) and increasing voltage narrows the pulse. At the boundary of the switchover between the two modes, there is a narrow region of uncertainty resulting in oscillation, which should be no problem in most applications.

When there is no H sync in sync-tip mode, the clamp pulse is generated by the VCO at the frequency preset by pin 6 (f_{MIN}). This feature is intended for use in On Screen Display systems.

Pin 3—CLAMP PULSE: Active-low clamp pulse output. See *Figure 4* for the output schematic.

Pin 4—VIDEO MUTE: This NPN open-collector output produces an active-low pulse when triggered by a step change of H sync frequency. See *Figure 5* for the output schematic.

Pin 5—f_{MAX}: A resistor from this pin to ground sets the upper frequency limit of the VCO. f_{MAX} is approximately:

$$2.13 \times 10^3 + \frac{1.69 \times 10^9}{(R_{MAX} + 500)} \text{ Hz}$$

Pin 6—f_{MIN}: A resistor from this pin to ground sets the lower frequency limit of the VCO. f_{MIN} is approximately:

$$4.21 \times 10^3 + \frac{5.56 \times 10^8}{(R_{MIN} + 500)} \text{ Hz}$$

Pin 7—V_{CC}: 12V nominal power supply pin. This pin should be decoupled to pin 21 (GND) via a short path with a cap of at least 47 µF.

Pin 8—V SYNC IN: This pin accepts AC-coupled V sync of either polarity. The pin is internally biased at 5.2V; its input resistance is approximately 50 kΩ. For best noise immunity, a resistor of 2 kΩ or less should be connected from the input side of the coupling cap to pin 21 (GND) via a short path. See *Figure 6* for the input schematic.

Pin 9—COMP VIDEO IN: The composite video sync stripper is active only when no signal is present at pin 12 (H/HV IN). The signal to pin 9 must have negative-going sync tips which are at least 0.14V below black level. For best noise immunity, a resistor of 2 kΩ or less should be connected from the input side of the coupling cap to pin 21 (GND) via a short path. See *Figure 7* for the input schematic.

Pin 10—H/HV SYNC OUT: The sync processor outputs active-low H/HV sync derived from the active sync input (pin 9 or pin 12). Pin 10 stays low in the absence of sync input. See *Figure 4* for the output schematic.

Pin 11—H/HV CAP: A capacitor is connected from this pin to ground for detecting the polarity and existence of H/HV sync at pin 12.

Pin 12—H/HV SYNC IN: This pin accepts AC-coupled H or composite sync of either polarity. For best noise immunity, a

Pin Descriptions (Continued)

resistor of 2 kΩ or less should be connected from the input side of the coupling cap to pin 21 (GND) via a short path. See *Figure 8* for the input schematic.

Pin 13 — H DR DUTY CNTL: A DC voltage applied to this pin sets the duty cycle of the horizontal drive output (pin 19), with a range of approximately 30%–70%. 2V sets the duty cycle to 50%. See *Figure 9* for the input schematic.

Pin 14 — H DRIVE $\overline{EN}$: A low logic level input enables H DRIVE OUT (pin 19). See *Figure 10* for the input schematic.

Pin 15 — X-RAY SHUTDOWN: This pin is for monitoring CRT anode voltage. If the input voltage exceeds an internal threshold, H DRIVE OUT (pin 19) is latched high and VIDEO MUTE (pin 4) is latched low. V_{CC} has to be reduced to below approximately 2V to clear the latched condition, i.e., power must be turned off. See *Figure 11* for the input schematic.

Pin 16 — V SYNC OUT: The sync processor outputs active-low V sync derived from the active sync input (pin 8, pin 9 or pin 12). Pin 16 stays low in the absence of sync input. See *Figure 4* for the output schematic.

Pin 17 — V CAP: A capacitor is connected from this pin to ground for detecting the polarity and existence of V sync at pin 8.

Pin 18 — FLYBACK IN: Input pin for phase detector 2. For best operation, the flyback peak should be at least 5V but not greater than V_{CC}. Any pulse width greater than 1.5 µs is acceptable. See *Figure 12* for the input schematic.

Pin 19 — H DRIVE OUT: This is an open-collector output which provides the drive pulse for the high power deflection circuit. The pulse duty cycle is controlled by pin 13. Polarity convention: Horizontal deflection output transistor is on when H DRIVE OUT is low. See *Figure 5* for the output schematic.

Pin 20 — H DRIVE GND: Ground return for H DRIVE OUT. For best jitter performance, this pin should be kept separate from the system ground (pin 21); the respective ground traces should meet at a single point, located as close as possible to the power supply output.

Pin 21 — GND: System ground. For best jitter performance, all bypass capacitors should be connected to this pin via short paths.

Pin 22 — V_{REF} CAP: This is the decoupling pin for the internal 8.2V reference. It should be decoupled to pin 26 (RETURN) via a short path with a cap of at least 470 µF.

Pin 23 — PHASE DET 2 CAP: The low-pass filter cap for the output of phase detector 2 is connected from this pin to pin 26 (RETURN) via a short path.

Pin 24 — H DRIVE PHASE: A DC control voltage applied to this pin sets the phase of the flyback pulse with respect to the leading edge of H sync. See *Figure 13* for the input schematic.

Pin 25 — FVC CAP 1: Primary FVC filter pin. C_{FVC1} is either connected from this pin to pin 21 (GND) or pin 26 (RETURN) via a short path. The voltage at this pin is buffered to pin 27 (FVC OUT).

Pin 26 — RETURN: Ground return for the decoupling capacitor at pin 22 (V_{REF} CAP), the filter capacitor at pin 23 (PHASE DET 2 CAP) as well as the loop filter at pin 28 (PD1 OUT/VCO IN). This pin must be isolated from GND and H DRIVE GND.

Pin 27 — FVC OUT: Buffered output of the Frequency-to-Voltage Converter, which sets the VCO center frequency through an external resistor to pin 28. Care should be taken when further loading this pin, since during the vertical interval it presents a high output impedance. Excessive loading can cause top-of-screen phase recovery problems. See *Figure 14* for the output schematic.

Pin 28 — PD1 OUT/VCO IN: Phase detector 1 has a gated charge pump output which requires an external low-pass filter. For best jitter performance, the filter should be grounded to pin 26 (RETURN) via a short path. If a voltage source is applied to this pin, the phase detector is disabled and the VCO can be controlled directly.

Application Hints

1. PHASE CONTROL FOR GEOMETRY CORRECTION

Pin 24 (H DRIVE PHASE) is designed to control static phase (picture horizontal position), while pin 23 (PHASE DET 2 CAP) controls dynamic phase for geometry correction. With the use of both pins 23 and 24, complete control of static and dynamic phase can be achieved. To accomplish this, the low-pass filter cap at pin 23 is not connected to pin 26 (RETURN), but is connected instead to a modulating AC voltage source. The cap then functions both as a low-pass filter (for phase detector 2) and as an input coupling cap (for the AC source).

2. PROGRAMMABLE FREQUENCY RAMPING

H frequency transitions from high to low present a special problem for deflection output stages without current limiting. If, during such a transition, the output transistor on-time increases excessively before the B+ voltage has decreased to its final level, then the deflection inductor current ramps too high and the induced flyback pulse can exceed the breakdown voltage, BV_{CEX}, of the output transistor. To prevent this, the rate of change of the VCO frequency must be limited.

Consider a scanning mode transition at t = 0 from f_1 to f_2. The VCO frequency as a function of time, $f_{VCO}(t)$, is described by the equation,

$$f_{VCO}(t) \approx f_1 + (f_2 - f_1)\,(1 - \exp(-t/\tau)),$$

$$\text{where } \tau = 40 \times 10^3 \times C_{FVC1}.$$

The above equation can be used to predict VCO behavior during frequency transitions, but in practice the value of C_{FVC1} is most easily determined empirically. In general, large values minimize the chance of exceeding BV_{CEX}, but generate long PLL capture times.

3. VIDEO MUTE

Numerous designs require video blanking during scanning mode transitions. The LM1292 provides an active-low pulse at pin 4 when triggered by a step change of H sync frequency from f_1 to f_2. The pulse width is controlled by the time constants set up through capacitors C_{FVC2} and C_{FVC1}, at pins 1 and 25 respectively. For $C_{FVC2} \geq 3 \times C_{FVC1}$, the pulse width is approximately:

$$40 \times 10^3 \times C_{FVC2} \times \ln\left(\frac{|f_2 - f_1|}{2.13 \times 10^3}\right) \text{ seconds}$$

Many sync sources fail to exhibit a clean step change of H sync frequency during scanning mode transitions. For this reason, in most applications a pulse smoothing circuit is needed at pin 4. Typically a 2.2 µF cap to ground is used in conjunction with a 100 kΩ pull-up resistor. See *Figure 15*. The resulting pulse has a slow rise time at the trailing edge, which extends the effective mute duration slightly.

Input/Output Schematics

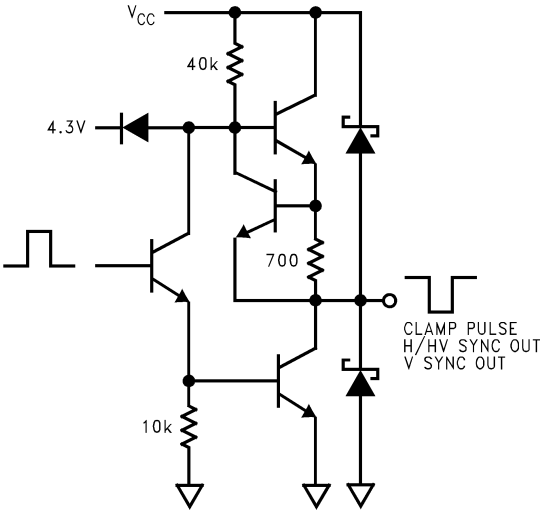


FIGURE 4.

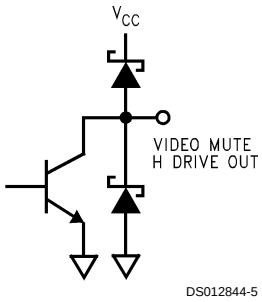


FIGURE 5.

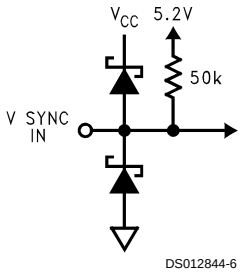


FIGURE 6.

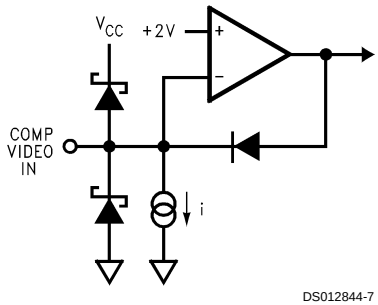


FIGURE 7.

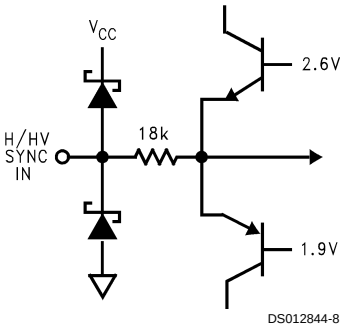


FIGURE 8.

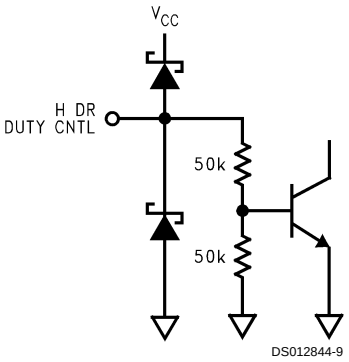


FIGURE 9.

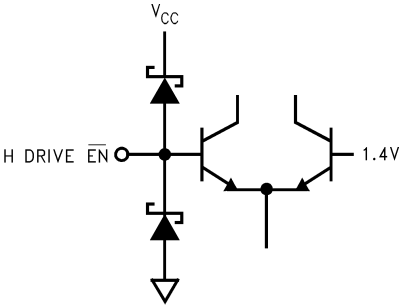


FIGURE 10.

Input/Output Schematics (Continued)

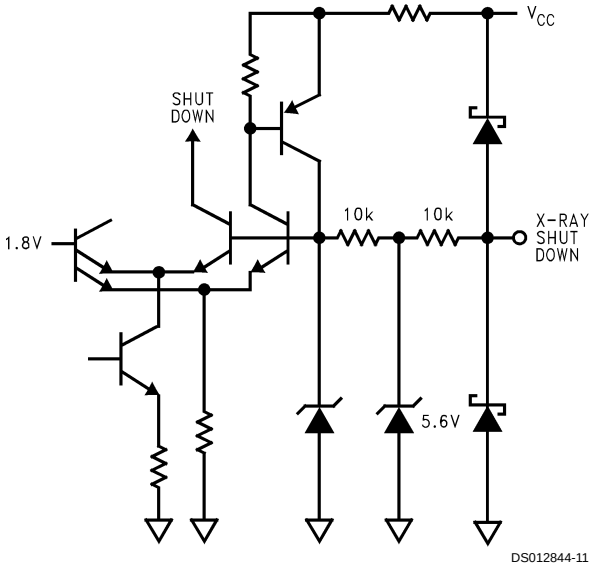


FIGURE 11.

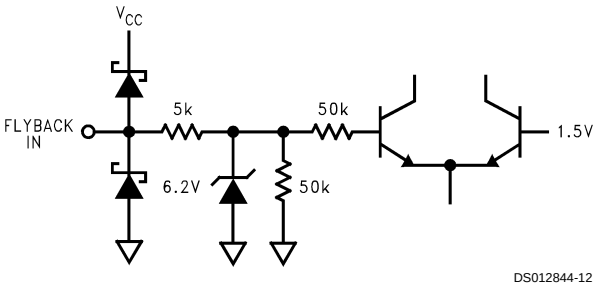


FIGURE 12.

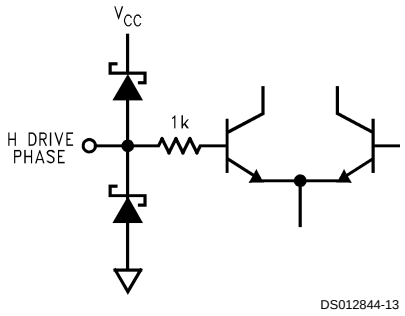


FIGURE 13.

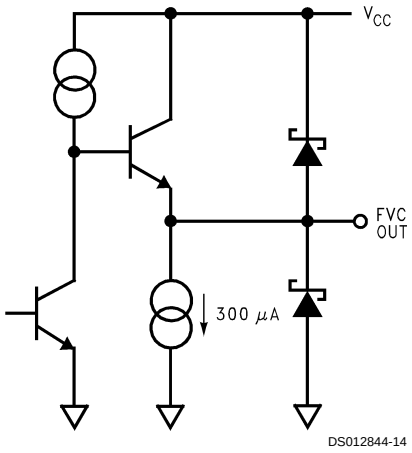


FIGURE 14.

Typical Application

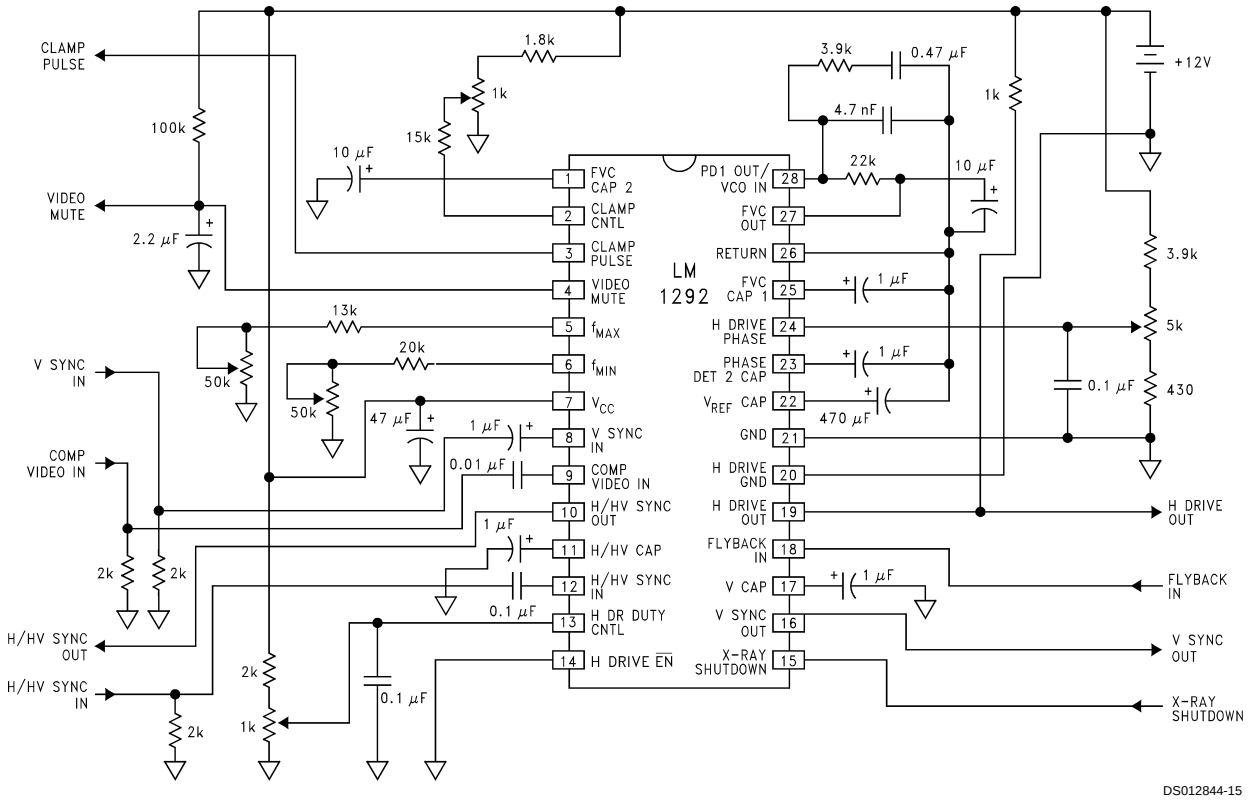
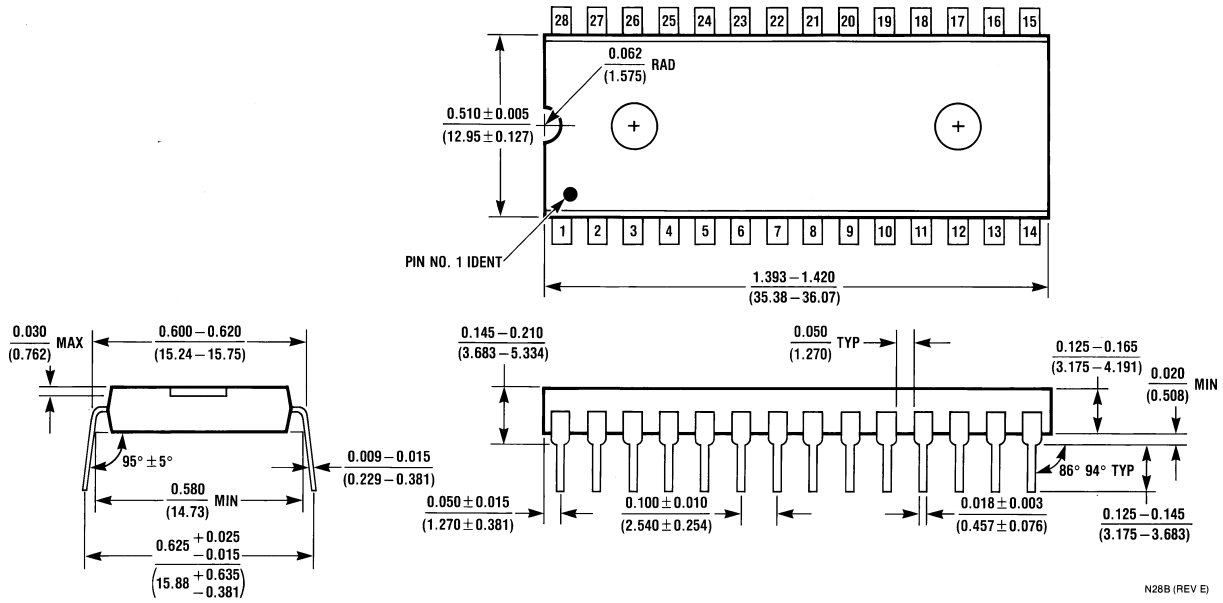


FIGURE 15.

Physical Dimensions inches (millimeters) unless otherwise noted



28-Lead (0.600" Wide) Molded Dual-In-Line Package
Order Number LM1292N
See NS Package Number N28B

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