December 2002

National Semiconductor

LP2996
DDR Termination Regulator

General Description

The LP2996 linear regulator is designed to meet the JEDEC SSTL-2 specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination. The LP2996 also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output as a reference for the chipset and DIMMs.

An additional feature found on the LP2996 is an active low shutdown ($\overline{SD}$) pin that provides Suspend To RAM (STR) functionality. When $\overline{SD}$ is pulled low the V_{TT} output will tri-state providing a high impedance output, but, V_{REF} will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

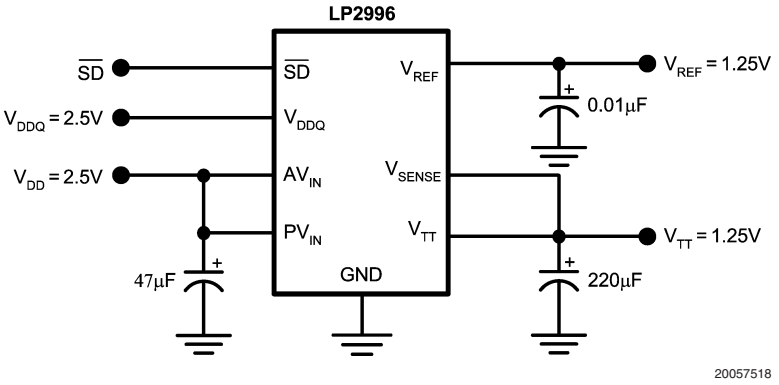
Features

- Source and sink current
- Low output voltage offset
- No external resistors required
- Linear topology
- Suspend to Ram (STR) functionality
- Low external component count
- Thermal Shutdown
- Available in SO-8, PSOP-8 or LLP-16 packages

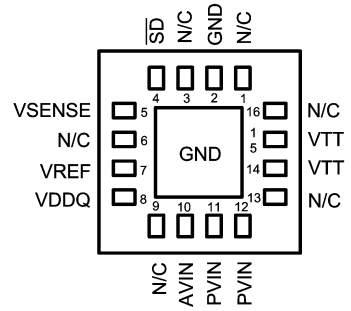
Applications

- DDR-I and DDR-II Termination Voltage
- SSTL-2 and SSTL-3 Termination
- HSTL Termination

Typical Application Circuit



Connection Diagrams



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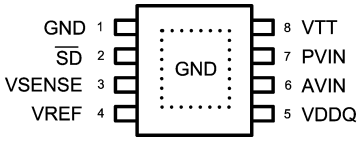
LLP-16 Layout



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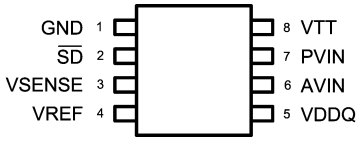
PSOP-8 Layout



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SO-8 Layout

Pin Description

SO-8 Pin or PSOP-8 Pin	LLP Pin	Name	Function
1	2	GND	Ground
2	4	$\overline{SD}$	Shutdown
3	5	VSENSE	Feedback pin for regulating V_{TT}.
4	7	VREF	Buffered internal reference voltage of $V_{DDQ}/2$
5	8	VDDQ	Input for internal reference equal to $V_{DDQ}/2$
6	10	AVIN	Analog input pin
7	11, 12	PVIN	Power input pin
8	14, 15	VTT	Output voltage for connection to termination resistors
-	1, 3, 6, 9, 13, 16	NC	No internal connection

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LP2996M	SO-8	M08A	95 Units per Rail
LP2996MX	SO-8	M08A	2500 Units Tape and Reel
LP2996MR	PSOP-8	MRA08A	95 Units Tape and Reel
LP2996MRX	PSOP-8	MRA08A	2500 Units Tape and Reel
LP2996LQ	LLP-16	LQA16A	1000 Units Tape and Reel
LP2996LQX	LLP-16	LQA16A	4500 Units Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

PVIN, AVIN, VDDQ to GND	−0.3V to +6V
Storage Temp. Range	−65˚C to +150˚C
Junction Temperature	150˚C
SO-8 Thermal Resistance (θ_{JA})	151˚C/W
PSOP-8 Thermal Resistance (θ_{JA})	43˚C/W
LLP-16 Thermal Resistance (θ_{JA})	51˚C/W
Lead Temperature (Soldering, 10 sec)	260˚C
ESD Rating (Note 2)	1kV

Operating Range

Junction Temp. Range (Note 3)	0˚C to +125˚C
AVIN to GND	2.2V to 5.5V

Electrical Characteristics

Specifications with standard typeface are for T_J = 25˚C and limits in **boldface type** apply over the full **Operating Temperature Range** (T_J = 0˚C to +125˚C) (Note 4). Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V (Note 5).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REF}	V_{REF} Voltage	VIN = VDDQ = 2.3V	**1.135**	1.158	**1.185**	
		VIN = VDDQ = 2.5V	**1.235**	1.258	**1.285**	V
		VIN = VDDQ = 2.7V	**1.335**	1.358	**1.385**	
Z_{VREF}	V_{REF} Output Impedance	I_{REF} = -30 to +30 µA		2.5		kΩ
V_{TT}	V_{TT} Output Voltage	I_{OUT} = 0A				V
		VIN = VDDQ = 2.3V	**1.125**	1.159	**1.190**	
		VIN = VDDQ = 2.5V	**1.225**	1.259	**1.290**	
		VIN = VDDQ = 2.7V	**1.325**	1.359	**1.390**	
		I_{OUT} = ±1.5A (Note 8)				
		VIN = VDDQ = 2.3V	**1.125**	1.159	**1.190**	
		VIN = VDDQ = 2.5V	**1.225**	1.259	**1.290**	
		VIN = VDDQ = 2.7V	**1.325**	1.359	**1.390**	
Vos_{TT}/V_{TT}	V_{TT} Output Voltage Offset (V_{REF}-V_{TT})	I_{OUT} = 0A	**-20**	0	**20**	mV
		I_{OUT} = -1.5A (Note 8)	**-25**	0	**25**	
		I_{OUT} = +1.5A (Note 8)	**-25**	0	**25**	
I_Q	Quiscent Current (Note 6)	I_{OUT} = 0A (Note 4)		320	**500**	µA
Z_{VDDQ}	VDDQ Input Impedance			100		kΩ
I_{SD}	Quiescent Current in Shutdown (Note 6)	SD = 0V		115	**150**	µA
I_{Q_SD}	Shutdown Leakage Current	SD = 0V		2	**5**	µA
V_{IH}	Minimum Shutdown High Level		**1.9**			V
V_{IL}	Minimum Shutdown Low Level				**0.8**	V
I_V	V_{TT} Leakage Current in Shutdown	SD = 0V V_{TT} = 1.25V		1	**10**	µA
I_{SENSE}	V_{SENSE} Input Current			13		nA
T_{SD}	Thermal Shutdown	(Note 7)		165		Celcius
$T_{SD_}$HYS	Thermal Shutdown Hysteresis			10		Celcius

Electrical Characteristics

Specifications with standard typeface are for T_J = 25˚C and limits in **boldface type** apply over the full **Operating Temperature Range** (T_J = 0˚C to +125˚C) (Note 4). Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V (Note 5). (Continued)

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions see Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Note 3: At elevated temperatures, devices must be derated based on thermal resistance. The device in the SO-8 package must be derated at θ_{JA} = 151.2˚ C/W junction to ambient with no heat sink.

Note 4: Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 5: VIN is defined as VIN = AVIN = PVIN.

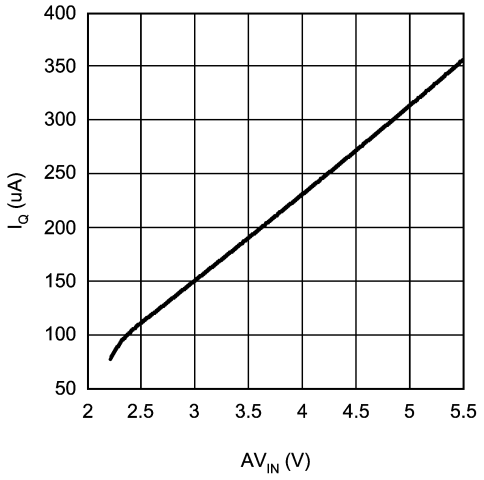
Note 6: Quiescent current defined as the current flow into AVIN.

Note 7: The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction to ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cauyse excessive die temperature and the regulator will go into thermal shutdown.

Note 8: V_{TT} load regulation is tested by using a 10 ms current pulse and measuring V_{TT}.

Typical Performance Characteristics

Iq vs AV_{IN} in SD



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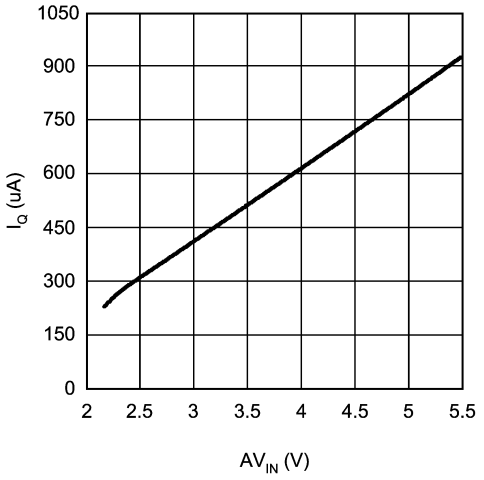
Iq vs AV_{IN}



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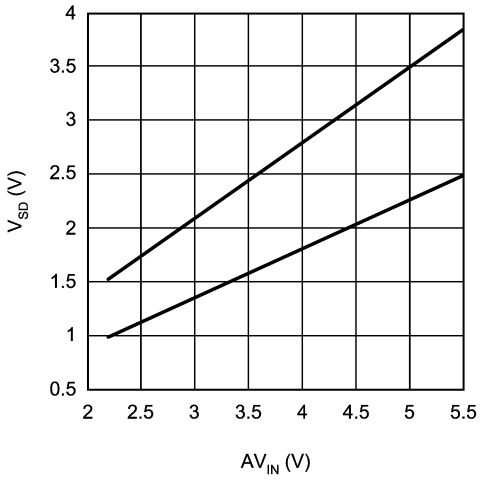
V_{IH} and V_{IL}



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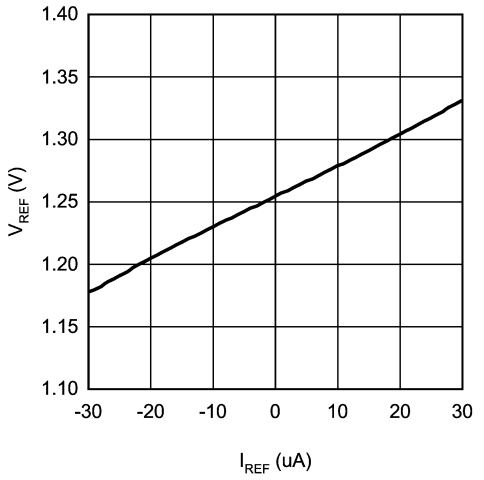
V_{REF} vs I_{REF}



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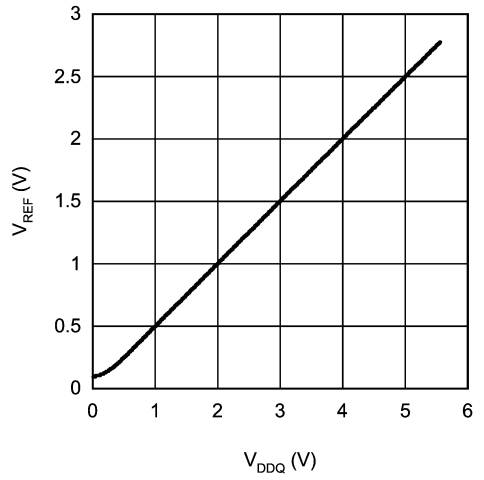
V_{REF} vs V_{DDQ}



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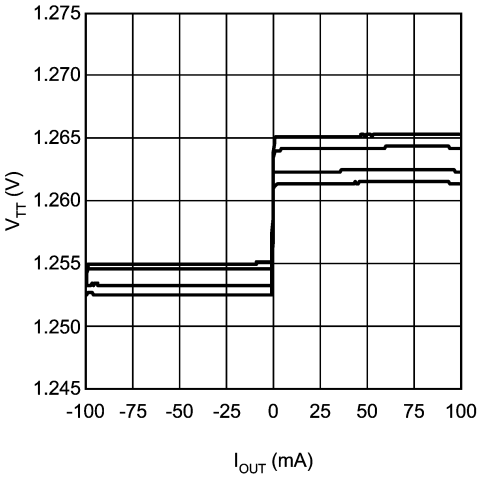
V_{TT} vs I_{OUT}



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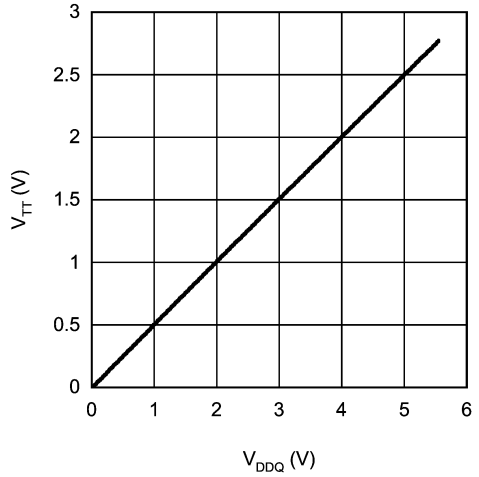
Typical Performance Characteristics (Continued)

V_{TT} vs V_{DDQ}



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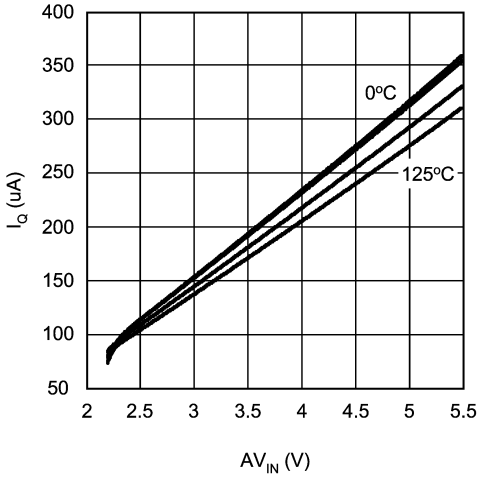
Iq vs AV_{IN} in SD Temperature



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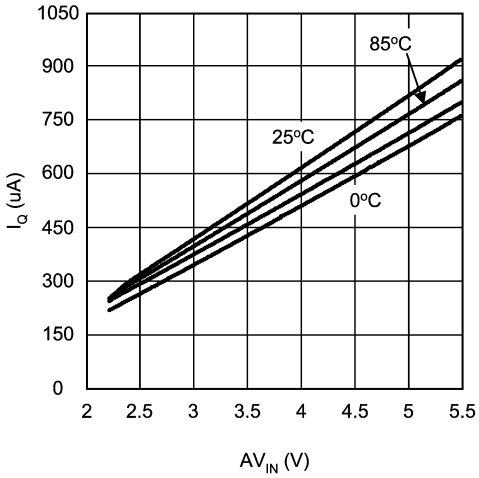
Iq vs AV_{IN} Temperature



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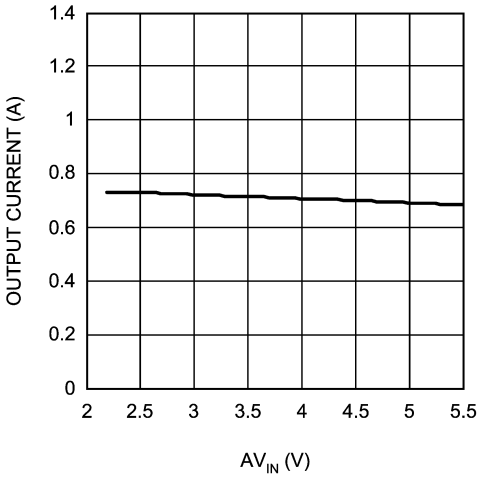
Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 2.5V, PV_{IN} = 1.8V)



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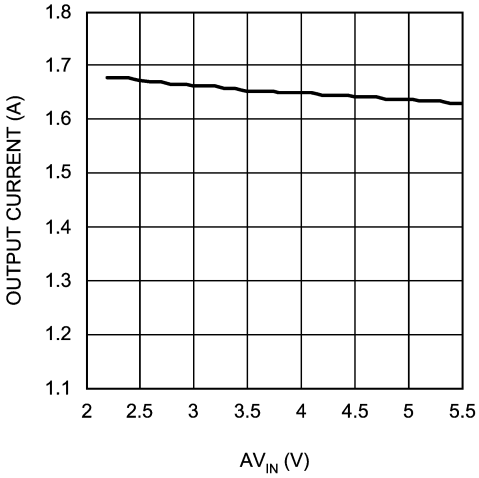
Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 2.5V, PV_{IN} = 2.5V)



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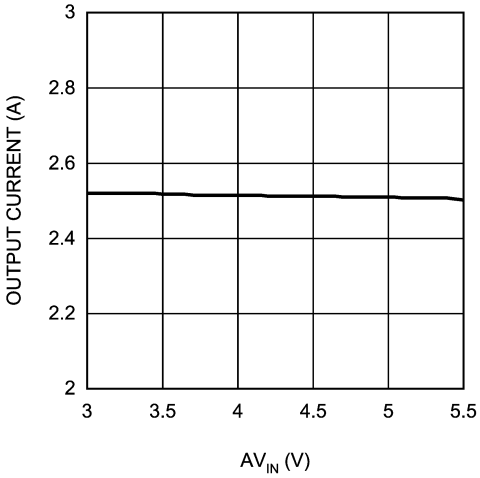
Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 2.5V, PV_{IN} = 3.3V)



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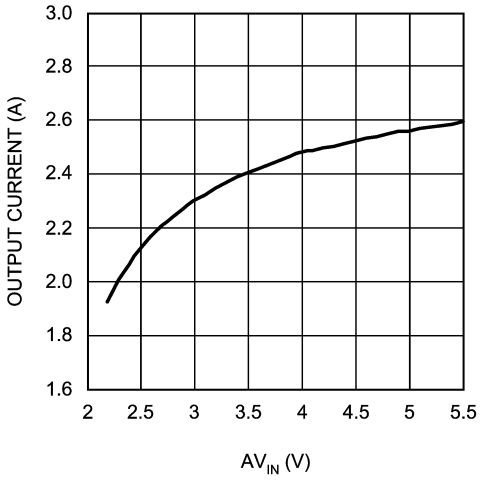
Typical Performance Characteristics (Continued)

Maximum Sinking Current vs AV_{IN} (V_{DDQ} = 2.5V)



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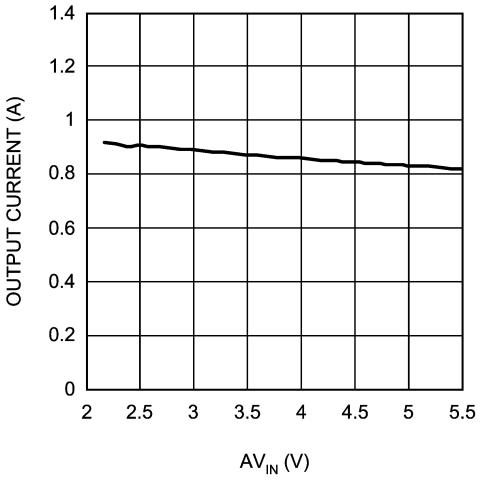
Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 1.8V, PV_{IN} = 1.8V)



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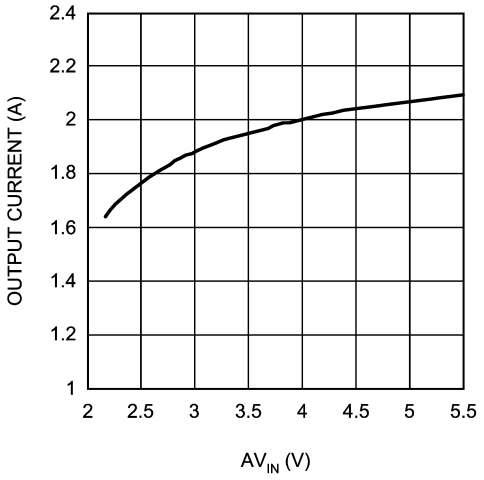
Maximum Sinking Current vs AV_{IN} (V_{DDQ} = 1.8V)



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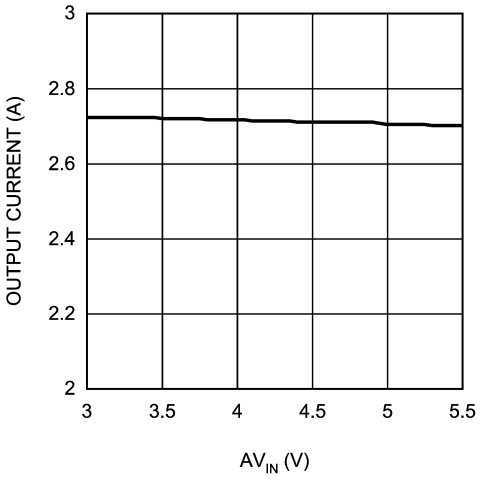
Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 1.8V, PV_{IN} = 3.3V)



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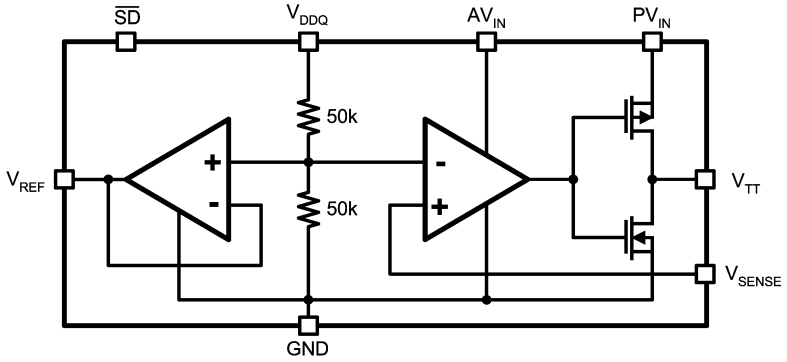
Block Diagram



Description

The LP2996 is a linear bus termination regulator designed to meet the JEDEC requirements of SSTL-2. The output, V_{TT} is capable of sinking and sourcing current while regulating the output voltage equal to VDDQ / 2. The output stage has been designed to maintain excellent load regulation while preventing shoot through. The LP2996 also incorporates two distinct power rails that separates the analog circuitry from the power output stage. This allows a split rail approach to be utilized to decrease internal power dissipation. It also permits the LP2996 to provide a termination solution for the next generation of DDR-SDRAM memory (DDRII). The LP2996 can also be used to provide a termination voltage for other logic schemes such as SSTL-3 or HSTL.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The most common form of termination is Class II single parallel termination. This involves one R_S series resistor from the chipset to the memory and one R_T termination resistor. Typical values for R_S and R_T are 25 Ohms, although these can be changed to scale the current requirements from the LP2996. This implementation can be seen below in *Figure 1*.

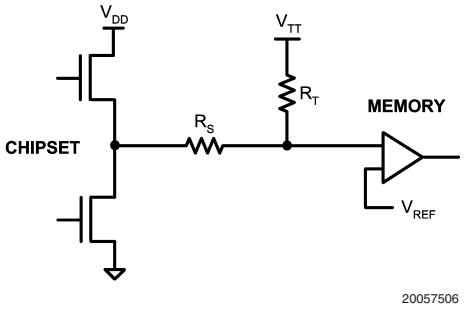


FIGURE 1. SSTL-Termination Scheme

Pin Descriptions

AVIN AND PVIN

AVIN and PVIN are the input supply pins for the LP2996. AVIN is used to supply all the internal control circuitry. PVIN, however, is used exclusively to provide the rail voltage for the output stage used to create VTT. These pins have the capability to work off separate supplies depending on the application. Higher voltages on PVIN will increase the maximum continuous output current because of output RDSON limitations at voltages close to VTT. The disadvantage of high values of PVIN is that the internal power loss will also increase, thermally limiting the design. For SSTL-2 applications, a good compromise would be to connect the AVIN and PVIN directly together at 2.5V. This eliminates the need for bypassing the two supply pins separately. The only limitation on input voltage selection is that PVIN must be equal to or lower than AVIN. It is recommended to connect PVIN to voltage rails equal to or less than 3.3V to prevent the thermal limit from tripping because of excessive internal power dissipation. If the junction temperature exceeds the thermal shutdown than the part will enter a shutdown state identical to the manual shutdown where V_{TT} is tri-stated and V_{REF} remains active.

VDDQ

VDDQ is the input used to create the internal reference voltage for regulating V_{TT}. The reference voltage is generated from a resistor divider of two internal 50kΩ resistors. This guarantees that V_{TT} will track VDDQ / 2 precisely. The optimal implementation of VDDQ is as a remote sense. This can be achieved by connecting VDDQ directly to the 2.5V rail at the DIMM instead of AVIN and PVIN. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-2 applications VDDQ will be a 2.5V signal, which will create a 1.25V termination voltage at V_{TT} (See Electrical Characteristics Table for exact values of V_{TT} over temperature).

V_{SENSE}

The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to V_{TT} in a long plane. If the output voltage was regulated only at the output of the LP2996 then the long trace will cause a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. The V_{SENSE} pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus. If remote load regulation is not used then the V_{SENSE} pin must still be connected to V_{TT}. Care should be taken when a long V_{SENSE} trace is implemented in close proximity to the memory. Noise pickup in the V_{SENSE} trace can cause problems with precise regulation of V_{TT}. A small 0.1uF ceramic capacitor placed next to the V_{SENSE} pin can help filter any high frequency signals and preventing errors.

V_{REF}

V_{REF} provides the buffered output of the internal reference voltage VDDQ / 2. This output should be used to provide the reference voltage for the Northbridge chipset and memory. Since these inputs are typically an extremely high impedance, there should be little current drawn from V_{REF}. For improved performance, an output bypass capacitor can be used, located close to the pin, to help with noise. A ceramic capacitor in the range of 0.1 µF to 0.01 µF is recommended. This output remains active during the shutdown state and thermal shutdown events for the suspend to RAM functionality.

V_{TT}

V_{TT} is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to VDDQ / 2. The LP2996 is designed to handle peak transient currents of up to ± 3A with a fast transient response. The maximum continuous current is a function of V_{IN} and can be viewed in the *TYPICAL PERFORMANCE CHARACTERISTICS* section. If a transient is expected to last above the maximum continuous current rating for a significant amount of time then the output capacitor should be sized large enough to prevent an excessive voltage drop. Despite the fact that the LP2996 is designed to handle large transient output currents it is not capable of handling these for long durations, under all conditions. The reason for this is the standard packages are not able to thermally dissipate the heat as a result of the internal power loss. If large currents are required for longer durations, then care should be taken to ensure that the maximum junction temperature is not exceeded. Proper thermal derating should always be used (please refer to the Thermal Dissipation section). If the junction temperature exceeds the thermal shutdown point than V_{TT} will tri-state until the part returns below the hysteretic trip-point.

Component Selection

INPUT CAPACITOR

The LP2996 does not require a capacitor for input stability, but it is recommended for improved performance during large load transients to prevent the input rail from dropping. The input capacitor should be located as close as possible to the PVIN pin. Several recommendations exist dependent on the application required. A typical value recommended for AL electrolytic capacitors is 50 µF. Ceramic capacitors can also be used, a value in the range of 10 µF with X5R or better would be an ideal choice. The input capacitance can be reduced if the LP2995 is placed close to the bulk capacitance from the output of the 2.5V DC-DC converter. If the two supply rails (AVIN and PVIN) are separated then the 47uF capacitor should be placed as close to possible to the PVIN rail. An additional 0.1uF ceramic capacitor can be placed on the AVIN rail to prevent excessive noise from coupling into the device.

OUTPUT CAPACITOR

The LP2996 has been designed to be insensitive of output capacitor size or ESR (Equivalent Series Resistance). This allows the flexibility to use any capacitor desired. The choice for output capacitor will be determined solely on the application and the requirements for load transient response of V_{TT}. As a general recommendation the output capacitor should be sized above 100 µF with a low ESR for SSTL applications with DDR-SDRAM. The value of ESR should be determined by the maximum current spikes expected and the extent at which the output voltage is allowed to droop. Several capacitor options are available on the market and a few of these are highlighted below:

AL - It should be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher

Component Selection (Continued)

frequency (between 20 kHz and 100 kHz) should be used for the LP2996. To improve the ESR several AL electrolytics can be combined in parallel for an overall reduction. An important note to be aware of is the extent at which the ESR will change over temperature. Aluminum electrolytic capacitors can have their ESR rapidly increase at cold temperatures.

Ceramic - Ceramic capacitors typically have a low capacitance, in the range of 10 to 100 µF range, but they have excellent AC performance for bypassing noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature. Because of the typically low value of capacitance it is recommended to use ceramic capacitors in parallel with another capacitor such as an aluminum electrolytic. A dielectric of X5R or better is recommended for all ceramic capacitors.

Hybrid - Several hybrid capacitors such as OS-CON and SP are available from several manufacturers. These offer a large capacitance while maintaining a low ESR. These are the best solution when size and performance are critical, although their cost is typically higher than any other capacitor.

THERMAL DISSIPATION

Since the LP2996 is a linear regulator any current flow from V_{TT} will result in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise (T_{Rmax}) can be calculated given the maximum ambient temperature (T_{Amax}) of the application and the maximum allowable junction temperature (T_{Jmax}).

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

From this equation, the maximum power dissipation (P_{Dmax}) of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA}$$

The θ_{JA} of the LP2995 will be dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow. For instance, the θ_{JA} of the SO-8 is 163˚C/W with the package mounted to a standard 8x4 2-layer board with 1oz. copper, no airflow, and 0.5W dissipation at room temperature. This value can be reduced to 151.2˚C/W by changing to a 3x4 board with 2 oz. copper that is the JEDEC standard. *Figure 2* shows how the θ_{JA} varies with airflow for the two boards mentioned.

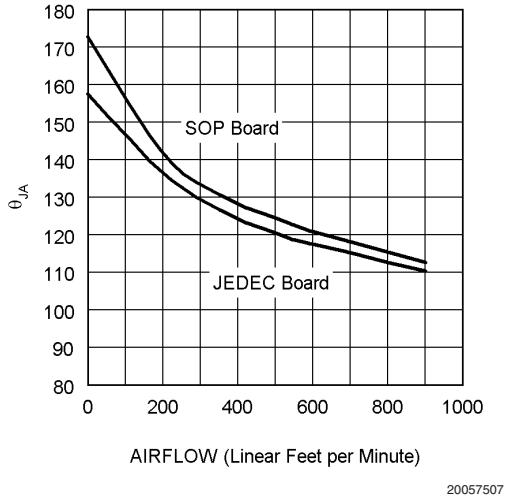


FIGURE 2. θ_{JA} vs Airflow (SO-8)

Additional improvements can be made by the judicious use of vias to connect the part and dissipate heat to an internal ground plane. Using larger traces and more copper on the top side of the board can also help. With careful layout it is possible to reduce the θ_{JA} further than the nominal values shown in *Figure 2*

Layout is also extremely critical to maximize the output current with the LLP package. By simply placing vias under the DAP the θ_{JA} can be lowered significantly. *Figure 3* shows the LLP thermal data when placed on a 4-layer JEDEC board with copper thickness of 0.5/1/1/0.5 oz. The number of vias, with a pitch of 1.27 mm, has been increased to the maximum of 4 where a θ_{JA} of 50.41˚C/W can be obtained. Via wall thickness for this calculation is 0.036 mm for 1oz. Copper.

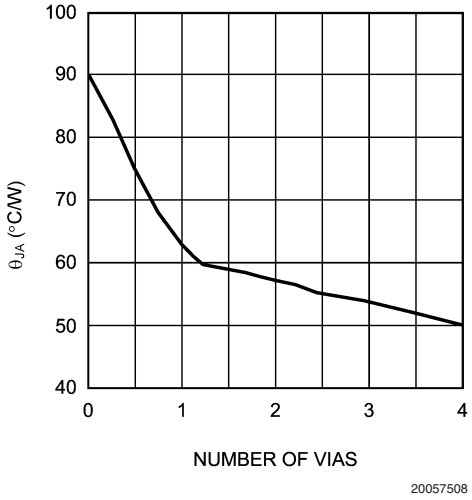


FIGURE 3. LLP-16 θ_{JA} vs # of Vias (4 Layer JEDEC Board))

Additional improvements in lowering the θ_{JA} can also be achieved with a constant airflow across the package. Maintaining the same conditions as above and utilizing the 2x2 via array, *Figure 4* shows how the θ_{JA} varies with airflow.

THERMAL DISSIPATION (Continued)

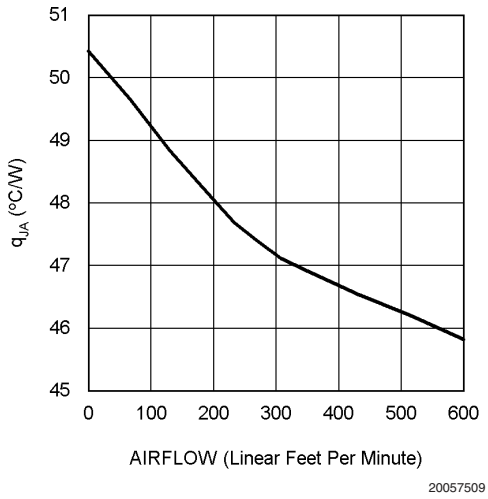


FIGURE 4. θ_{JA} vs Airflow Speed (JEDEC Board with 4 Vias)

Optimizing the θ_{JA} and placing the LP2996 in a section of a board exposed to lower ambient temperature allows the part to operate with higher power dissipation. The internal power dissipation can be calculated by summing the three main sources of loss: output current at V_{TT}, either sinking or sourcing, and quiescent current at AVIN and VDDQ. During the active state (when shutdown is not held low) the total internal power dissipation can be calculated from the following equations:

$$P_D = P_{AVIN} + P_{VDDQ} + P_{VTT}$$

Where,

$$P_{AVIN} = I_{AVIN} * V_{AVIN}$$

$$P_{VDDQ} = V_{VDDQ} * I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ}$$

To calculate the maximum power dissipation at V_{TT} both conditions at V_{TT} need to be examined, sinking and sourcing current. Although only one equation will add into the total, V_{TT} cannot source and sink current simultaneously.

$$P_{VTT} = V_{VTT} \times I_{LOAD} \text{ (Sinking) or}$$

$$P_{VTT} = (V_{PVIN} - V_{VTT}) \times I_{LOAD} \text{ (Sourcing}$$

The power dissipation of the LP2996 can also be calculated during the shutdown state. During this condition the output V_{TT} will tri-state, therefore that term in the power equation will disappear as it cannot sink or source any current (leakage is negligible). The only losses during shutdown will be the reduced quiescent current at AVIN and the constant impedance that is seen at the VDDQ pin.

$$P_D = P_{AVIN} + P_{VDDQ}$$

$$P_{AVIN} = I_{AVIN} \times V_{AVIN}$$

$$P_{VDDQ} = V_{VDDQ} * I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ}$$

Typical Application Circuits

Several different application circuits have been shown in *Figure 5* through *Figure 14* to illustrate some of the options that are possible in configuring the LP2996. Graphs of the individual circuit performance can be found in the *Typical Performance Characteristics* section in the beginning of the datasheet. These curves illustrate how the maximum output current is affected by changes in AVIN and PVIN.

SSTL-2 APPLICATIONS

For the majority of applications that implement the SSTL-2 termination scheme it is recommended to connect all the input rails to the 2.5V rail. This provides an optimal trade-off between power dissipation and component count and selection. An example of this circuit can be seen in *Figure 5*.

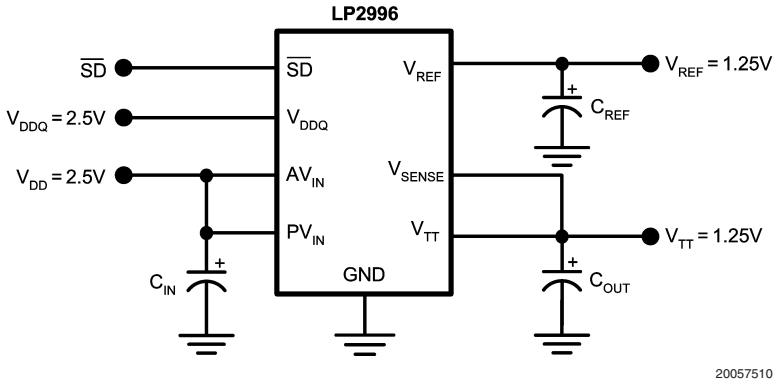


FIGURE 5. Recommended SSTL-2 Implementation

If power dissipation or efficiency is a major concern then the LP2996 has the ability to operate on split power rails. The output stage (PVIN) can be operated on a lower rail such as 1.8V and the analog circuitry (AVIN) can be connected to a higher rail such as 2.5V, 3.3V or 5V. This allows the internal power dissipation to be lowered when sourcing current from V_{TT}. The disadvantage of this circuit is that the maximum continuous current is reduced because of the lower rail voltage, although it is adequate for all motherboard SSTL-2 applications. Increasing the output capacitance can also help if periods of large load transients will be encountered.

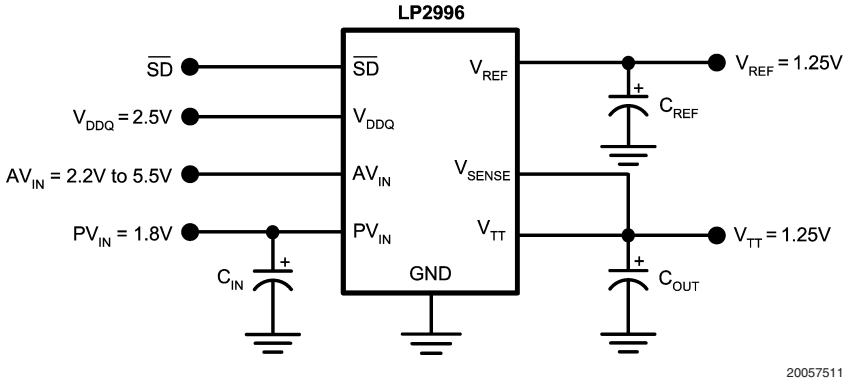


FIGURE 6. Lower Power Dissipation SSTL-2 Implementation

The third option for SSTL-2 applications in the situation that a 1.8V rail is not available and it is not desirable to use 2.5V, is to connect the LP2996 power rail to 3.3V. In this situation AVIN will be limited to operation on the 3.3V or 5V rail as PVIN can never exceed AVIN. This configuration has the ability to provide the maximum continuous output current at the downside of higher thermal dissipation. Care should be taken to prevent the LP2996 from experiencing large current levels which cause the junction temperature to exceed the maximum. Because of this risk it is not recommended to supply the output stage with a voltage higher than a nominal 3.3V rail.

Typical Application Circuits (Continued)

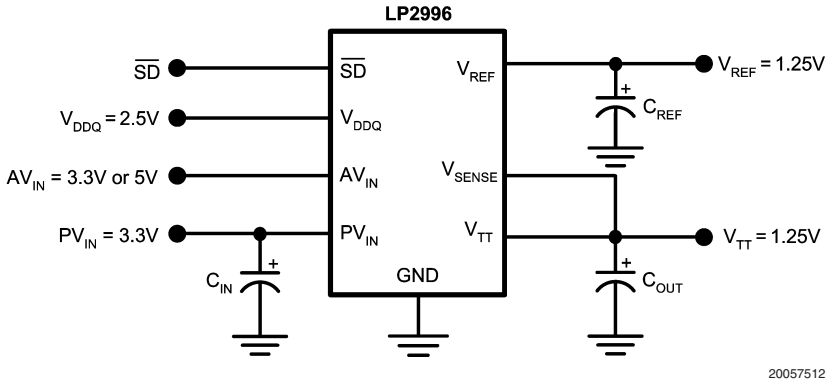


FIGURE 7. SSTL-2 Implementation with higher voltage rails

DDR-II APPLICATIONS

With the separate VDDQ pin and an internal resistor divider it is possible to use the LP2996 in applications utilizing DDR-II memory. *Figure 6* and *Figure 7* show several implementations of recommended circuits with output curves displayed in the *Typical Performance Characteristics*. *Figure 6* shows the recommended circuit configuration for DDR-II applications. The output stage is connected to the 1.8V rail and the AVIN pin can be connected to either a 3.3V or 5V rail.

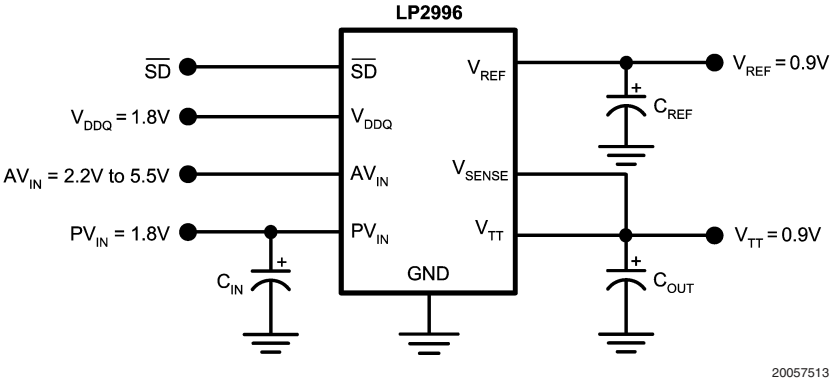


FIGURE 8. Recommended DDR-II Termination

If it is not desirable to use the 1.8V rail it is possible to connect the output stage to a 3.3V rail. Care should be taken to not exceed the maximum junction temperature as the thermal dissipation increases with lower V_{TT} output voltages. For this reason it is not recommended to power PVIN off a rail higher than the nominal 3.3V. The advantage of this configuration is that it has the ability to source and sink a higher maximum continuous current.

Typical Application Circuits (Continued)

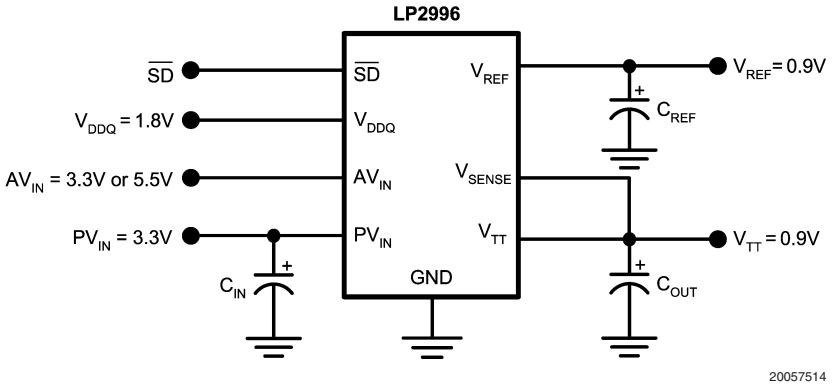


FIGURE 9. DDR-II Termination with higher voltage rails

LEVEL SHIFTING

If standards other than SSTL-2 are required, such as SSTL-3, it may be necessary to use a different scaling factor than 0.5 times V_{DDQ} for regulating the output voltage. Several options are available to scale the output to any voltage required. One method is to level shift the output by using feedback resistors from V_{TT} to the V_{SENSE} pin. This has been illustrated in Figures 10 and 11. Figure 10 shows how to use two resistors to level shift V_{TT} above the internal reference voltage of VDDQ/2. To calculate the exact voltage at V_{TT} the following equation can be used.

$$V_{TT} = VDDQ/2 \ (\ 1 + R1/R2)$$

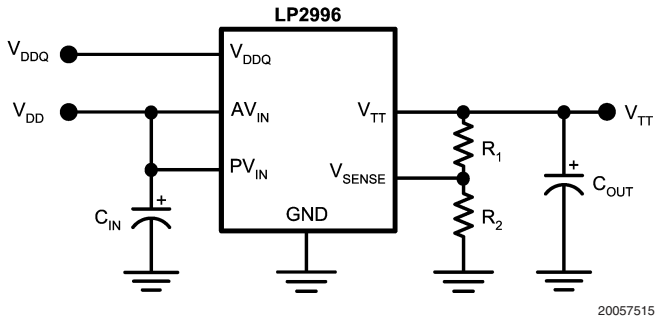


FIGURE 10. Increasing VTT by Level Shifting

Conversely, the R2 resistor can be placed between V_{SENSE} and V_{DDQ} to shift the V_{TT} output lower than the internal reference voltage of VDDQ/2. The equations relating VTT and the resistors can be seen below:

$$V_{TT} = VDDQ/2 \ (1 - R1/R2)$$

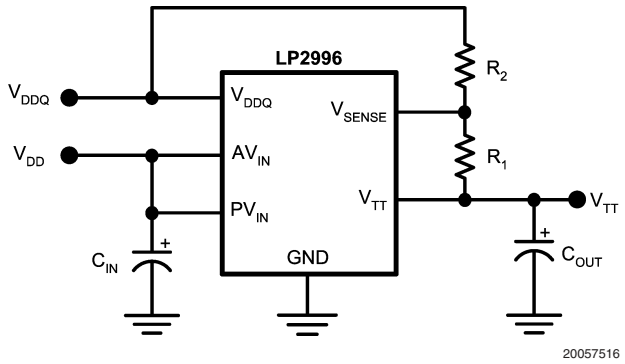


FIGURE 11. Decreasing VTT by Level Shifting

Typical Application Circuits (Continued)

HSTL APPLICATIONS

The LP2996 can be easily adapted for HSTL applications by connecting V_{DDQ} to the 1.5V rail. This will produce a V_{TT} and V_{REF} voltage of approximately 0.75V for the termination resistors. AVIN and PVIN should be connected to a 2.5V rail for optimal performance.

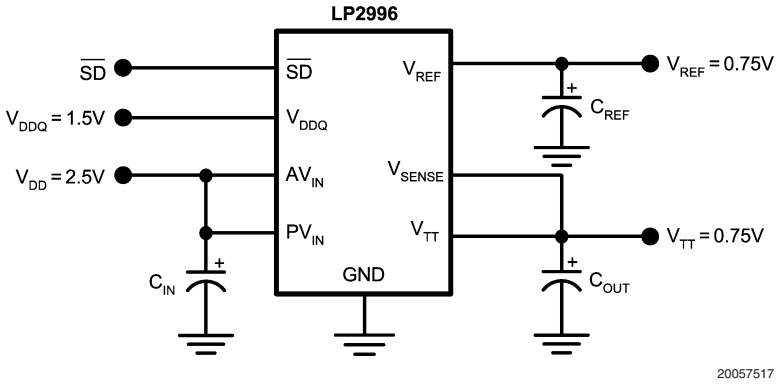


FIGURE 12. HSTL Application

QDR APPLICATIONS

Quad data rate (QDR) applications utilize multiple channels for improved memory performance. However, this increase in bus lines has the effect of increasing the current levels required for termination. The recommended approach in terminating multiple channels is to use a dedicated LP2996 for each channel. This simplifies layout and reduces the internal power dissipation for each regulator. Separate V_{REF} signals can be used for each DIMM bank from the corresponding regulator with the chipset reference provided by a local resistor divider or one of the LP2996 signals. Because V_{REF} and V_{TT} are expected to track and the part to part variations are minor, there should be little difference between the reference signals of each LP2996.

OUTPUT CAPACITOR SELECTION

For applications utilizing the LP2996 to terminate SSTL-2 I/O signals the typical application circuit shown in *Figure 11* can be implemented.

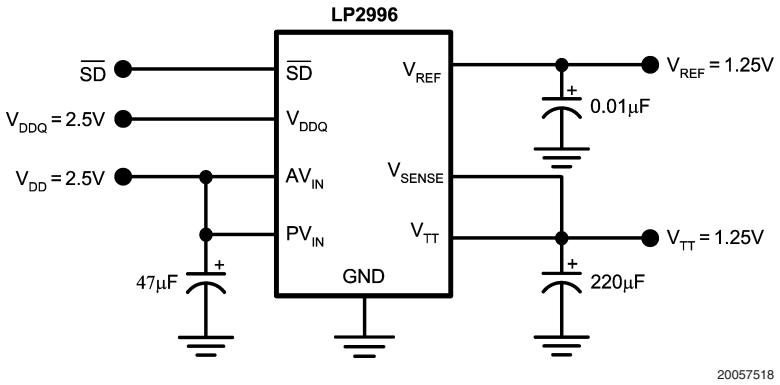


FIGURE 13. Typical SSTL-2 Application Circuit

This circuit permits termination in a minimum amount of board space and component count. Capacitor selection can be varied depending on the number of lines terminated and the maximum load transient. However, with motherboards and other applications where V_{TT} is distributed across a long plane it is advisable to use multiple bulk capacitors and addition to high frequency decoupling. *Figure 12* shown below depicts an example circuit where 2 bulk output capacitors could be situated at both ends of the V_{TT} plane for optimal placement. Large aluminum electrolytic capacitors are used for their low ESR and low cost.

Typical Application Circuits (Continued)

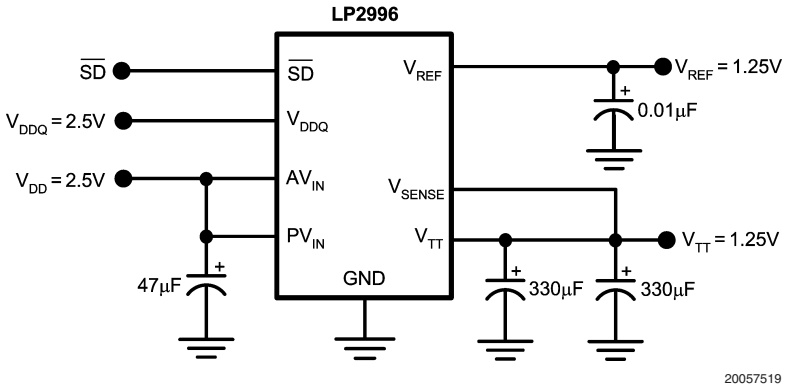


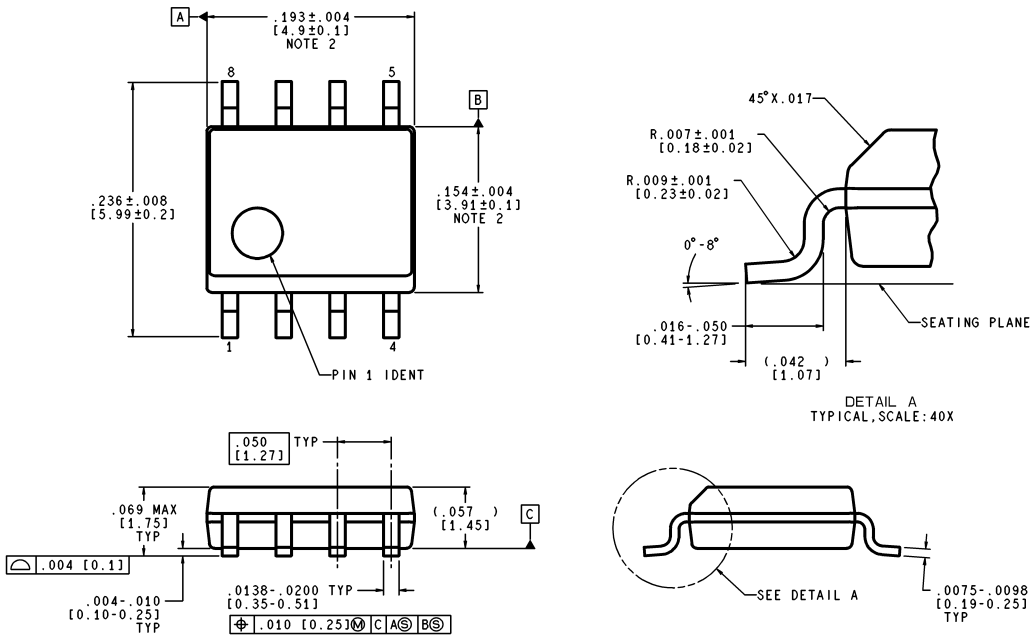
FIGURE 14. Typical SSTL-2 Application Circuit for Motherboards

In most PC applications an extensive amount of decoupling is required because of the long interconnects encountered with the DDR-SDRAM DIMMs mounted on modules. As a result bulk aluminum electrolytic capacitors in the range of 1000uF are typically used.

PCB Layout Considerations

1. The input capacitor for the power rail should be placed as close as possible to the PVIN pin.
2. V_{SENSE} should be connected to the V_{TT} termination bus at the point where regulation is required. For motherboard applications an ideal location would be at the center of the termination bus.
3. V_{DDQ} can be connected remotely to the V_{DDQ} rail input at either the DIMM or the Chipset. This provides the most accurate point for creating the reference voltage.
4. For improved thermal performance excessive top side copper should be used to dissipate heat from the package. Numerous vias from the ground connection to the internal ground plane will help. Additionally these can be located underneath the package if manufacturing standards permit.
5. Care should be taken when routing the V_{SENSE} trace to avoid noise pickup from switching I/O signals. A 0.1uF ceramic capacitor located close to the $_{SENSE}$ can also be used to filter any unwanted high frequency signal. This can be an issue especially if long $_{SENSE}$ traces are used.
6. V_{REF} should be bypassed with a 0.01 µF or 0.1 µF ceramic capacitor for improved performance. This capacitor should be located as close as possible to the V_{REF} pin.

Physical Dimensions inches (millimeters) unless otherwise noted

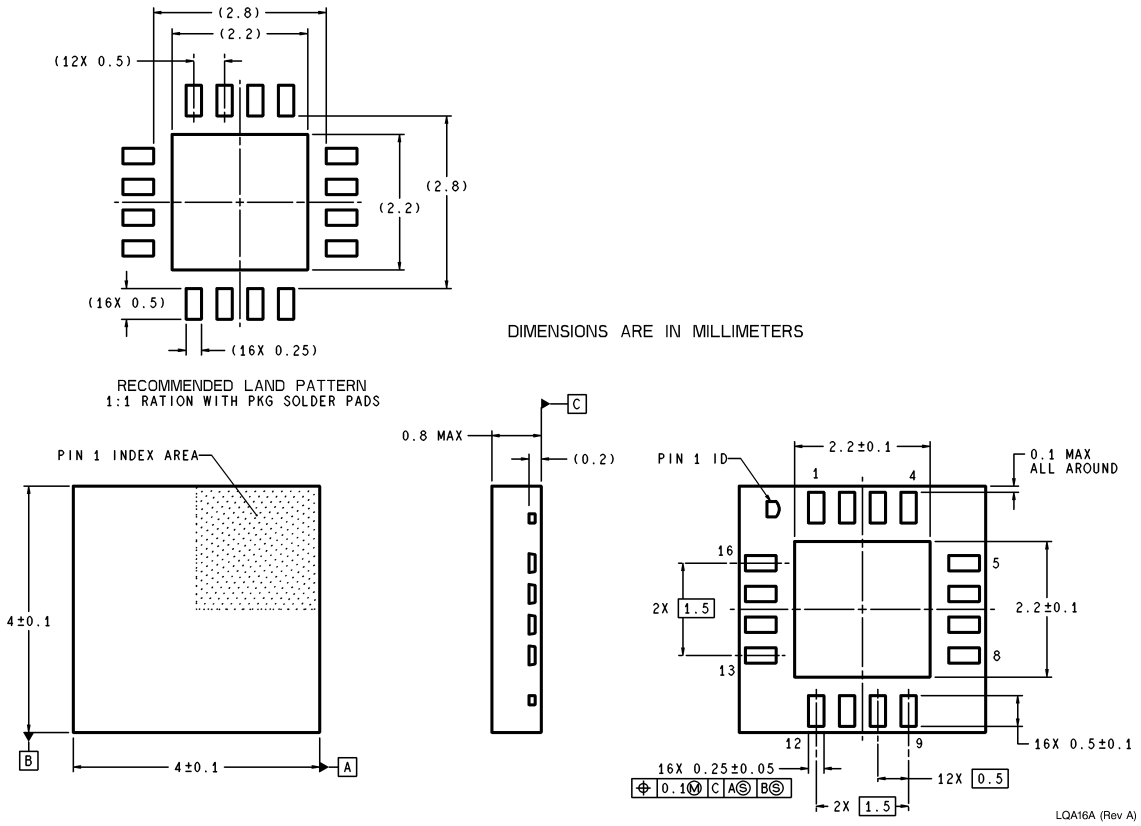


CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

M08A (Rev J)

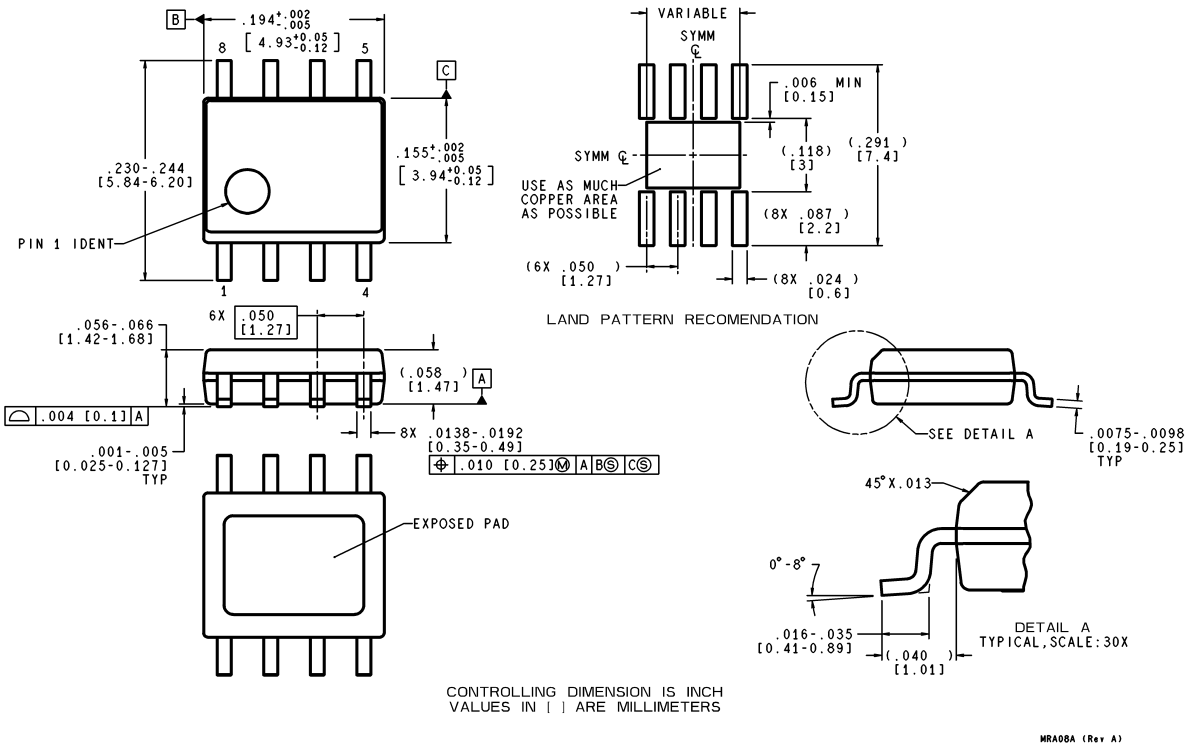
8-Lead Small Outline Package (M8)
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead LLP Package (LD)
NS Package Number LQA16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead PSOP Package (PSOP-8)
NS Package Number MRA08A

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