

SANYO Semiconductors DATA SHEET

An ON Semiconductor Company

LV56351HA — 1ch DC/DC boost converter

Overview

LV56351HA integrates 1ch DC/DC boost converter and 1ch LDO. It is suitable as the power supply for BS/CS antennas of LCD/PDP TV and BD recorders that require automatic recovery without IC destruction and malfunction when the output is short-circuited.

Functions

[DC/DC boost converter]

- Soft-start time: 2.8ms
- Frequency 425kHz operation
- Pulse by pulse over current limiter
- Short circuit protector (SCP)

[LDO]

• Over current limiter (Fold back)

[All

- Under voltage lockout
- Thermal shutdown protector
- Power good

Specifications

Maximum Ratings at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
V _{CC} maximum supply voltage		V _{CC} max		-0.3 to 25	V
LDOIN maximum input voltage		V _{LDOIN} max		-0.3 to 30	V
SW maximum voltage		V _{SW} max		-0.3 to 30	V
Allowable power dissipation		Pd max	*1	1.45	W
Operating temperature		Topr		-30 to +85	°C
Operating junction temperature		Tjopr		-30 to +125	°C
Storage temperature		Tstg		-40 to +150	°C
Allowable	V _{CC} , EN			25	V
pin voltage	SW, LDOIN, LDOOL	JT		30	V
	IN1, IN2, FB, SCP, PGOOD, DDCTL			6	V

^{*1} Mounted on a specified board : 32mm × 38mm × 1.6mm, glass epoxy, double side board.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

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Recommended Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
V _{CC} supply voltage	V _{CC}		8 to 23	V
LDOIN input voltage	V _{LDOIN}		8 to 28	V
SW voltage	V _{SW}		-0.3 to 28	V
EN voltage	VEN		0 to 23	V

$\textbf{Electrical Characteristics} \ at \ Ta = \underline{25^{\circ}C}, \ V_{CC} = 12V, \ V_{EN} = 2V, \ LDOIN = 16V, \ LDOOUT = 15V$

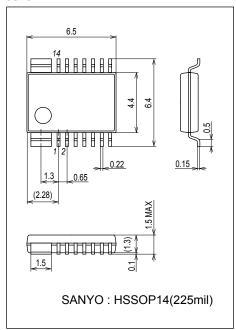
Parameter	Symbol	Conditions	Ratings			Unit
i arameter	Symbol	Conditions	min	typ	max	Offic
All						
Supply current1	Icc	Switching is turned off		1.8	3.5	mA
Supply current2	loff	EN = 0V			10	μΑ
Reference voltage	V _{REF}		1.2348	1.26	1.2852	>
Enable voltage	V _{EN}		2.0			>
Disable voltage	V _{DIS}				0.4	٧
EN input current	I _{EN}	V _{EN} = 2.0V			10	μΑ
PGOOD threshold	VPG	IN1 ≥ VREF×85% and IN2 ≥ VREF×85%		VREF×0.85		V
PGOOD sink current	IPG	V _{PGOOD} = 0.5V		1.0		mA
PGOOD leak current	IPGLK	V _{PGOOD} = 2V			10	μΑ
UVLO on voltage	V _{UVLO}			7.0		V
Thermal shutdown temperature	T _{TSD}	*2	130			°C
TSD hysteresis	T _{HYS}	*2		30		°C
DC/DC boost converter						
FB output voltage "Low"	FB _{Low}	IN1 = 2.0V, I _{FB} = -20μA (Sink)			0.2	V
FB output voltage "High"	FB _{High}	IN1 = 0.2V, I _{FB} = 20μA (Source)	1.8			V
Soft-start time	T _{SS}			2.8		ms
Oscillator frequency	Fosc			425		kHz
Max on duty	D _{MAX}		78	85	92	%
SW on resistance	R _{ON}			0.7		Ω
SW peak current	I _{PK}		1.5	1.8		Α
SCP source current	ISCP			4.8		μΑ
SCP threshold	V _{SCP}			VREF		V
DDCTL on voltage	VDDCTLON	DC/DC Off	2.0			V
DDCTL off voltage	VDDCTLOFF	DC/DC On			0.4	V
DDCTL input current	IDDCTL	V _{DDCTL} = 2V			20	μΑ
LDO						
Maximum output current	IOMAX		350	520	670	mA
Line regulation	R _{LN}	16V < LDOIN < 21V			20	mV
Load regulation	R _{LD}	10mA < I _O < 300mA			20	mV
Dropout voltage	V _{DROP}	I _O = 300mA		0.25	0.4	V
Short current	ISHORT	LDOOUT = GND			100	mA

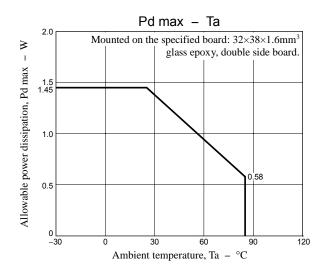
^{*2:} Design guarantee value.

Package Dimensions

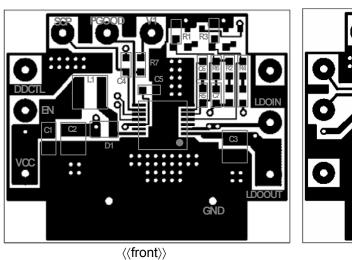
unit: mm (typ)

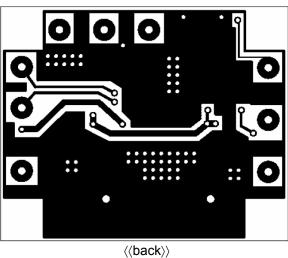
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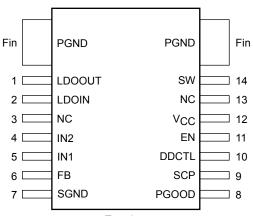


Specified board (32mm × 38mm × 1.6mm, glass epoxy, double side board)





Pin assignment



Top view

LV56351HA

Pin function

Pin fun			
Pin No.	Pin name	Function	Equivalent circuit
1	LDOOUT	LDO output	0.15011
2	LDOIN	LDO input	2 LDOIN
7	SGND	Signal ground (*3)	++
			1) LDOOUT
			1 220001
			T -
			7) SGND
			Ŭ
4	IN2	LDO feedback input	\downarrow
			iguplus
			10kΩ
			IN2 4 W
			★ ★
			SGND (7)
			OGIVE (1) TO TO T
5	IN1	DC/DC error amplifier input	
		20,20 direi ampinio impat	\bigcirc
			,
			10kΩ
			IN1 5 10KS2
			★ ★
			T \$ h \$\$
			SGND (7)
			\cup
6	FB	DC/DC error amplifier output	\downarrow
			Ω 1kΩ
			FB 6 + W + +
			SGND 7
8	PGOOD	Power good output	
	1 0005	1 ower good output	8 PGOOD
			500Ω≸
			→
			
			7 SGND
	COD	DO/DO CODit	
9	SCP	DC/DC SCP capacitor connect pin for timer setting	
			300Ω $2k\Omega$ 9 SCP
			9 SCP
			M# J+₹ ★
			7 SGND
10	DDCTL	DC/DC on and off control	_
10	DDCIL	DO/DO ON AND ON CONTROL	DDCTL (10) VREG
			₩ 6 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8
			SGND (7)
			33.13 ()
11	EN	Enable	Vac 12 -
12	Vcc	Power supply	V _{CC} ②
			EN (1) +
			T TG[55]
			SGND 7

^{*3:} When you use this IC, Please short-circuit all the pins of SGND and PGND on the IC mounting side.

Continued on next page.

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Continued from preceding page.

Pin No.	Pin name	Function	Equivalent circuit
14 Fin	SW	DC/DC open drain output	VREG 14 SW
Fin	PGND	Power ground (*3)	Fin PGND

^{*3:} When you use this IC, Please short-circuit all the pins of SGND and PGND on the IC mounting side.

Function overview

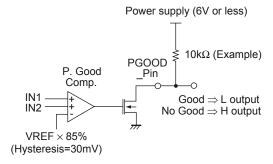
(1) UVLO (Under Voltage Lockout)

UVLO stops outputs of both DC/DC and LDO to prevent malfunction when V_{CC} decreases. UVLO operates when V_{CC} falls below the UVLO voltage. This function is a non-latch-type, and recovers these outputs automatically when V_{CC} exceeds the UVLO voltage.

(2) Power good

Power good notifies that the output voltages of DC/DC and LDO are within the range of the setting voltage. The two output voltages are monitored through the voltage of IN1 and IN2. The output is judged to be "power good" when both outputs are 85% or higher compared to the setting voltages. If either IN1 or IN2 voltage falls below VREF×85%, PGOOD output becomes $L \to H$ (No Good). When IN1 and IN2 voltages become (VREF×85%) + 30mV or higher, PGOOD output becomes $H \to L$ (Good). During soft start, the output is H (No Good).

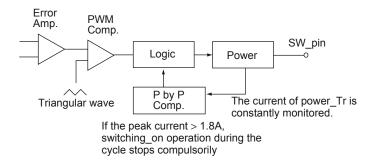
⟨⟨Power good circuit diagram⟩⟩



(3) Pulse-by-Pulse over current protection (P by P)

The P by P stops switch-on operation of a certain cycle by force when the current of power MOSFET reaches the maximum output peak current.

⟨⟨P by P circuit diagram⟩⟩



(4) Short Circuit Protector (SCP)

When output voltage of DC/DC decreases due to short-circuit; for example, SCP latches off the outputs of DC/DC and LDO by timer.

When output voltage of DC/DC decreases and FB turns to H, which is the error amplifier output, charge at $4.8\mu A$ constant current starts to SCP capacitor for timer setting. When SCP voltage exceeds the threshold voltage (=VREF), latch-off occurs. If the output voltage recovers until the time the SCP voltage reaches to the threshold voltage, SCP capacitor is discharged and timer is reset. To restart the output after latch-off, you need to input EN signal again. If you do not use the SCP function, make sure to short SCP and GND.

To define timer, you need to calculate a value of SCP capacitor using the following formula because timer (tSCP) depends on capacitance.

$$C_{SCP} = (I_{SCP} \times tSCP)/VREF$$

$$\langle \langle SCP \ circuit \ diagram \rangle \rangle \qquad \langle \langle Waveform \ of \ SCP_Pin \rangle \rangle$$

$$C_{SCP} = (I_{SCP} \times tSCP)/VREF$$

Voltage

Reset

(5) DC/DC on and off control

setting

This function controls on and off of DC/DC during the operation of IC.

VREF

Discharge Tr

⟨⟨Turning on DC/DC⟩⟩

Where DDCTL = Low or open, DC/DC and LDO operate at the same time.

⟨⟨Turning off DC/DC⟩⟩

Where DDCTL = High, DC/DC is compulsorily stopped and only LDO operates.

When DDCTL is switched from H to L (or open), LDO stops temporarily and DC/DC starts with soft start and then LDO restart. If you switch DDCTL during IC operation, make sure that the output waveforms of DC/DC and LDO are normal.

Time

Latch-OFF

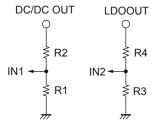
Output voltage setting

Output voltages are given by the following formulas.

DCDCOUT =
$$(1+R2/R1) \times VREF[V]$$

LDOOUT = $(1+R4/R3) \times VREF[V]$

 $\langle\langle Resistance \ for \ output \ setting\rangle\rangle$

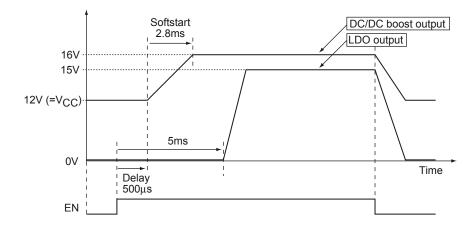


Start and stop

Start: Make sure to input EN signal (L \Rightarrow H) after supplying $V_{CC} = 12V$.

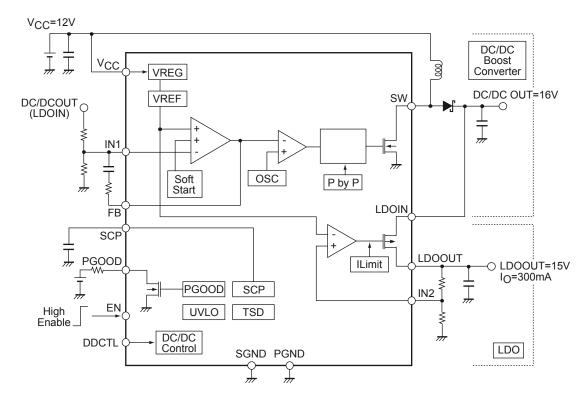
Stop: Reverse-operation of start.

 $\langle\langle Output\ waveform\ during\ start\ and\ stop \rangle\rangle$



Block diagram and Application circuit 1 (for BS antenna)

Condition: V_{CC} = 12V, DCDCOUT = 16V, LDOOUT = 15V

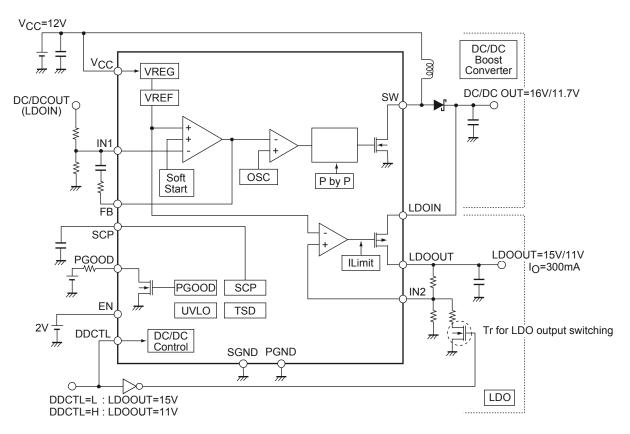


 $\langle\langle Note \rangle\rangle$

When LDOOUT is in the over current state or the short-circuit state, IC and external parts are protected by over current limiter of LDO. And when DC/DCOUT is short-circuited, IC stops by timer latch-off type SCP function.

Application circuit 2 (for BS/CS antenna)

BS condition: $V_{CC} = 12V$, DCDCOUT = 16V, LDOOUT = 15V CS condition: $V_{CC} = 12V$, DCDC = OFF, LDOOUT = 11V



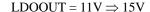
 $\langle\langle Addition\rangle\rangle$

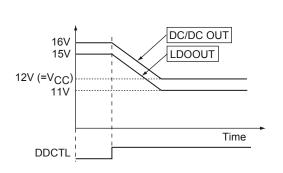
The above application circuit enables switching between 15V for BS and 11V for CS.

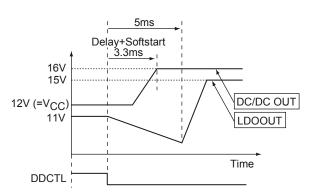
Where DDCTL=L, DC/DC booster is turned on and set as follows: DC/DCOUT=16V, LDOOUT=15V Where DDCTL=H, DC/DC booster is turned off and set as follows: DC/DCOUT=11.7V, LDOOUT=11V (because the resistance value of output setting of LDO is switched)

⟨⟨Output waveform at switching⟩⟩

 $LDOOUT = 15V \Rightarrow 11V$







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