

# QUADRUPLE BISTABLE LATCH

# S5475

# N7475

S5475-B • N7475-B

DIGITAL 54/74 TTL SERIES

## DESCRIPTION

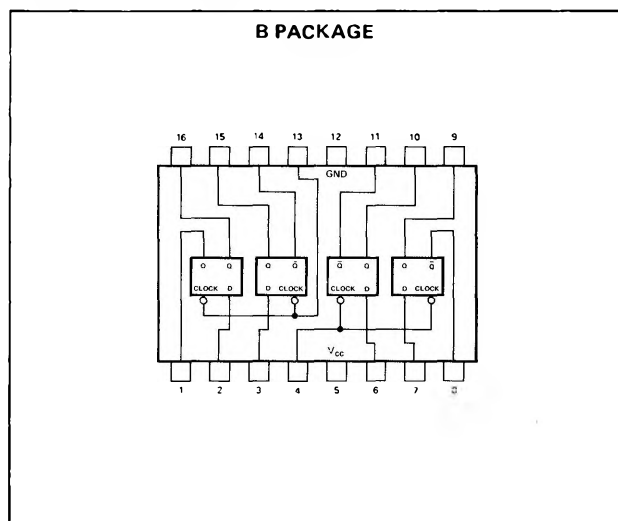
The S5475B/N7475B is a monolithic, quadruple, bistable latch with complementary Q and  $\bar{Q}$  outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

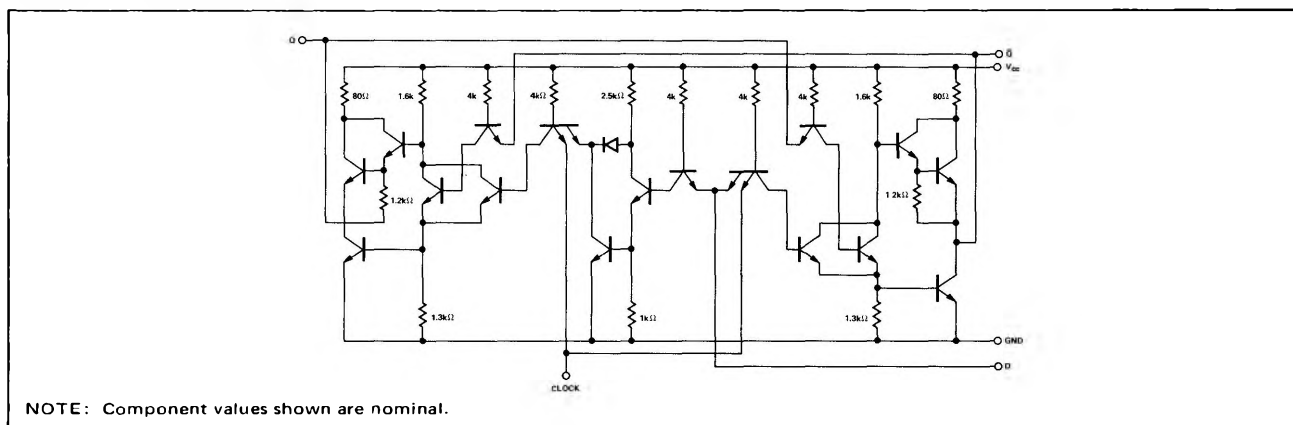
## TRUTH TABLE

LOGIC			NOTES:
(Each Latch)			
$t_n$	$t_{n+1}$		1. $t_n$ = bit time before clock pulse. 2. $t_{n+1}$ = bit time after clock pulse 3. These voltages are with respect to network ground terminal.
D	Q	$\bar{Q}$	
1	1	0	
0	0	1	

## PIN CONFIGURATIONS



## SCHEMATIC (each latch)



## RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ (See Note 3):	4.5	5	5.5	V
S5475 Circuits	4.75	5	5.25	V
N7475 Circuits			10	
Normalized Fan-Out from Outputs			10	
Operating Free-Air Temperature Range, $T_A$ :	-55	25	125	$^{\circ}C$
S5475 Circuits	0	25	70	$^{\circ}C$
N7475 Circuits				

## ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	$V_{CC} = \text{MIN}$	2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	$V_{CC} = \text{MIN}$		0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -400\mu A$	2.4		V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16mA$		0.4	V

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**ELECTRICAL CHARACTERISTICS (Cont'd)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current at D	$V_{CC} = \text{MAX}$ ,	$V_{in} = 0.4V$			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	$V_{CC} = \text{MAX}$ ,				-6.4	mA
$I_{in(1)}$	Logical 1 level input current at D	$V_{CC} = \text{MAX}$ ,	$V_{in} = 2.4V$			80	$\mu A$
$I_{in(1)}$	Logical 1 level input current at clock	$V_{CC} = \text{MAX}$ ,	$V_{in} = 5.5V$			1	mA
$I_{OS}$	Short circuit output current†	$V_{CC} = \text{MAX}$	$V_{in} = 2.4V$			160	$\mu A$
$I_{OS}$	Short circuit output current†	$V_{CC} = \text{MAX}$	$V_{in} = 5.5V$			1	mA
$I_{OS}$	Short circuit output current†	$V_{CC} = \text{MAX}$ ,	S5475	-20		-75	mA
$I_{OS}$	Short circuit output current†	$V_{out} = 0$	N7475	-18		-75	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ ,	S5475		32	46	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ ,	N7475		32	53	mA

**SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $N = 10$**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{setup1}$	Minimum logical 1 level input setup time at D input	$C_L = 15pF$ ,	$R_L = 400\Omega$		7	20	ns
$t_{setup0}$	Minimum logical 0 level input setup time at D input	$C_L = 15pF$ ,	$R_L = 400\Omega$		14	20	ns
$t_{hold1}$	Maximum logical 1 level input hold time required at D input	$C_L = 15pF$ ,	$R_L = 400\Omega$	0	15¶		ns
$t_{hold0}$	Maximum logical 0 level input hold time required at D input	$C_L = 15pF$ ,	$R_L = 400\Omega$	0	6¶		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	$C_L = 15pF$ ,	$R_L = 400\Omega$		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	$C_L = 15pF$ ,	$R_L = 400\Omega$		14	25	ns
$t_{pd1(D-\bar{Q})}$	Propagation delay time to logical 1 level from D input to $\bar{Q}$ output	$C_L = 15pF$ ,	$R_L = 400\Omega$		24	40	ns
$t_{pd0(D-\bar{Q})}$	Propagation delay time to logical 0 level from D input to $\bar{Q}$ output	$C_L = 15pF$ ,	$R_L = 400\Omega$		7	15	ns
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	$C_L = 15pF$ ,	$R_L = 400\Omega$		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	$C_L = 15pF$ ,	$R_L = 400\Omega$		7	15	ns
$t_{pd1(C-\bar{Q})}$	Propagation delay time to logical 1 level from clock input to $\bar{Q}$ output	$C_L = 15pF$ ,	$R_L = 400\Omega$		16	30	ns
$t_{pd0(C-\bar{Q})}$	Propagation delay time to logical 0 level from clock input to $\bar{Q}$ output	$C_L = 15pF$ ,	$R_L = 400\Omega$		7	15	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.  
 \*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .  
 † Not more than one output should be shorted at a time.  
 ¶ These typical times indicate that period occurring prior to the fall of clock pulse ( $t_0$ ) below 1.5V when data at the D input will still be recognized and stored.